Hi3521A/Hi3520D V300 H.264 CODEC Processor

Data Sheet

Issue 00B07

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Contents

About This Document

Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module of the Hi3521A/Hi3520D V300. This document also describes the interface timings and related parameter in diagrams. In addition, this document details the pins, pin usages, performance parameters, and package of the Hi3521A/Hi3520D V300.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3521A	V100
Hi3520D	V300

Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.
 WARNING	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
 CAUTION	Indicates a potentially hazardous situation, which if not avoided, could result in equipment damage, data loss, performance degradation, or unexpected results.
 TIP	Indicates a tip that may help you solve a problem or save time.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

General Conventions

The general conventions that may be found in this document are defined as follows.

Convention	Description
Times New Roman	Normal paragraphs are in Times New Roman.
Boldface	Names of files, directories, folders, and users are in **boldface**. For example, log in as user **root**.
Italic	Book titles are in *italics*.
`Courier New`	Examples of information displayed on the screen are in `Courier New`.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Content	Description
–	The cell is blank.
*	The content in this cell is configurable.

Notes

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)

Symbol	Example	Description
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues is changed.

Issue 00B07 (2015-12-10)

Chapter 2 Hardware_Hi3521A_BGA

Sections 2.1.2, 2.8.2, 2.8.3, and 2.8.4 are modified.

In section 2.10.4, table 2-83 is modified.

In section 2.10.7, the description of the SPI Timings is modified.

Chapter 2 Hardware_Hi3520DV300_QFP

Sections 2.8.2, 2.8.3, and 2.8.4 are modified.

In section 2.1.2, table 2-3 is modified.

In section 2.2.2, table 2-26 is modified.

In section 2.8, table 2-66 is modified.

In section 2.10.4, table 2-83 is modified.

In section 2.10.7, the description of the SPI Timings is modified.

Chapter 3 System

Section 3.10 is modified.

Issue 00B06 (2015-10-30)

This issue is the sixth draft release.

Chapter 1 Product Description

In section 1.2.1, table 1-3 is modified.

Section 1.2.2 is modified.

Chapter 2 Hardware Hi3520DV300

In section 2.8.1 table 2-64 is modified.

In section 2.8.3 table 2-66 is modified.

Chapter 3 System

Section 3.3 is modified.

Issue 00B05 (2015-09-20)

This issue is the fifth draft release.

Chapter 1 Product Description

In section 1.2.10, the 2x720p TDM inputs for Hi3520D V300 implemented through 148.5 MHz dual-edge sampling for each 8-bit interface is changed to 4x720p TDM inputs.

Chapter 2 Hardware Hi3520DV300

In section 2.8.1 table 2-64 is modified.

In section 2.8.3 table 2-66 is modified.

In section 2.10.3 table 2-76, table 2-77, table 2-78 , and table 2-79 are modified.

Chapter 2 Hardware Hi3521A_BGA

In section 2.8.1 table 2-66 and table 2-67 are modified.

In section 2.8.3 table 2-68 is modified.

In section 2.10.3 table 2-78, table 2-79, table 2-80 , and table 2-81 are modified.

Chapter 3 System

In section 3.2.7, PERI_CRG11 bit[30:29], PERI_CRG13 bit[5:4], PERI_CRG15 bit[3:2], PERI_CRG16 bit[3:2], PERI_CRG17 bit[3:2] and PERI_CRG19 bit[2] are modified.

Section 3.12.5 is deleted.

Chapter 8 Motion Detect Unit

In Section 8.2 is modified.

Issue 00B04 (2015-07-15)

Chapter 1 Product Description

In section 1.2.4, the H.264 multi-frame encoding and decoding performance of the Hi3520DV300 is modified.

Chapter 6 Video Codec

In section 6.1.2, the maximum picture resolution is changed.

The H.264 multi-frame encoding and decoding performance is modified.

Appendix A Ordering Information

The contents related to Hi3520DV300 mark is added.

Issue 00B03 (2015-06-27)

This issue is the third draft release. Ordering Information is added.

Issue 00B02 (2015-06-09)

This issue is the second draft release.

Issue 00B01 (2015-05-11)

This issue is the first draft release.

Contents

Figures

Tables

1 Product Description

1.1 Application Scenarios

The Hi3521A/Hi3520D V300 is a professional SoC targeted for the multi-channel HD (1080p/720p) or SD (D1/960H) DVR. The Hi3521A/Hi3520D V300 provides an ARM A7 processor, a high-performance H.264 video encoding/decoding engine, a high-performance video/graphics processing engine with various complicated graphics processing algorithms, HDMI/VGA HD outputs, and various peripheral interfaces. These features enable the Hi3521A /Hi3520D V300 to provide high-performance, high-picture-quality, and low-cost analog HD/SDI solutions for customers' products while reducing the eBOM cost.

CAUTION

Unless otherwise specified, this document applies to the Hi3521A and Hi3520D V300. The descriptions are provided using the Hi3521A as an example.

Figure 1-1 shows the typical application scenario of the Hi3521A.

Figure 1-1 Application block diagram of the Hi3521A

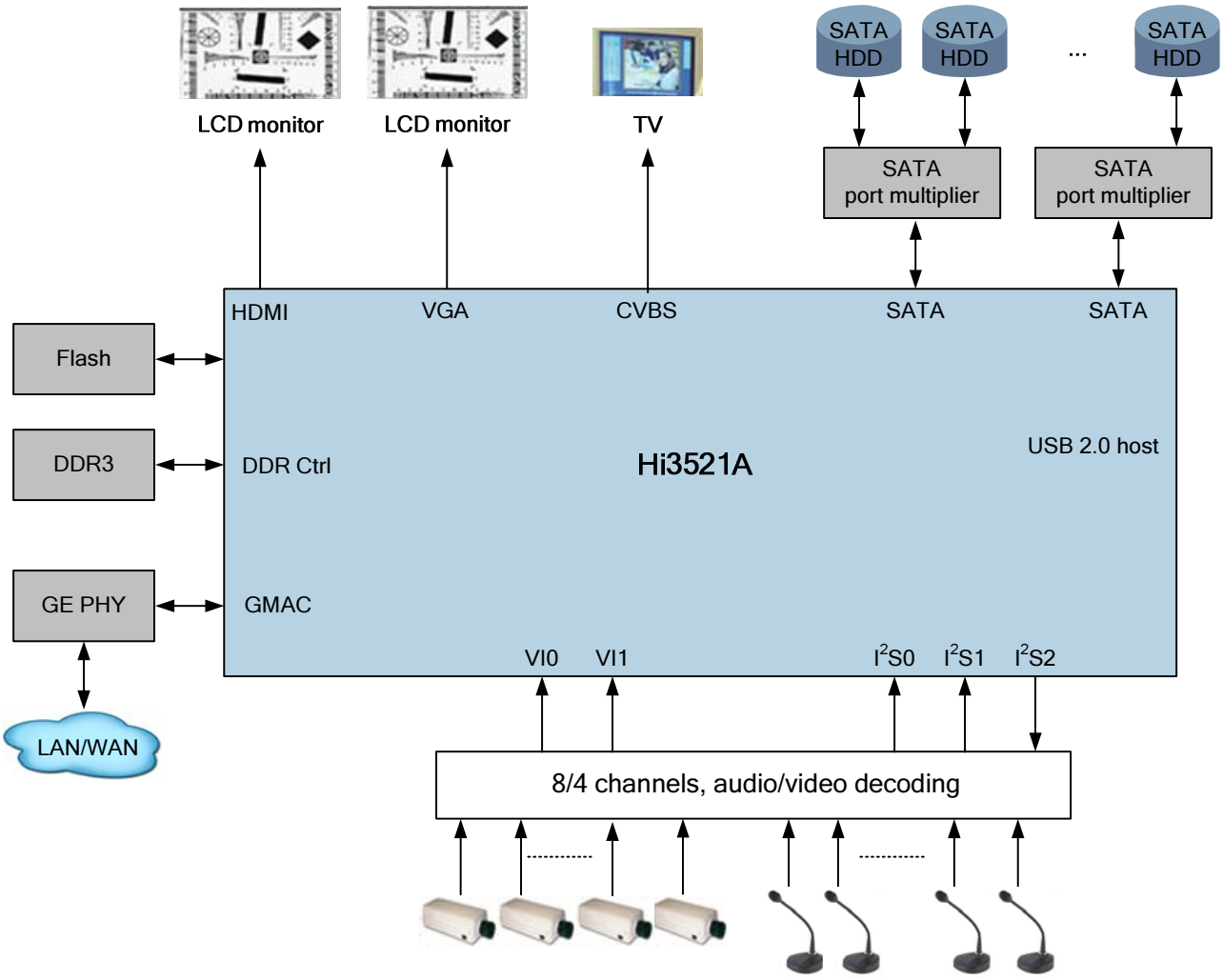
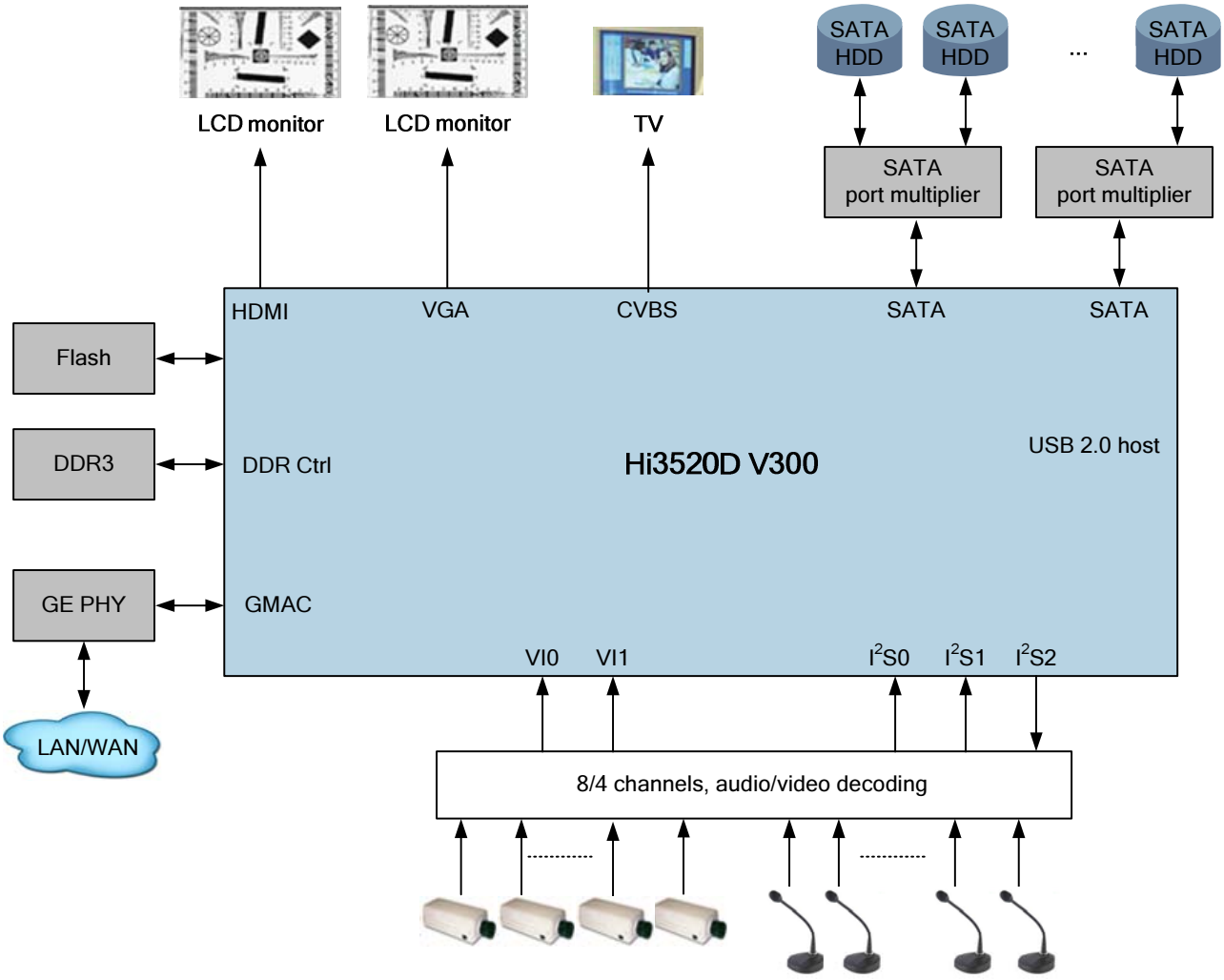


Figure 1-2shows the typical application scenario of the Hi3520D V300.

Figure 1-2 Application block diagram of the Hi3520D V300



1.2 Architecture

1.2.1 Overview

Figure 1-3 shows the logic block diagram of the Hi3521A.

Figure 1-3 Logic block diagram of the Hi3521A

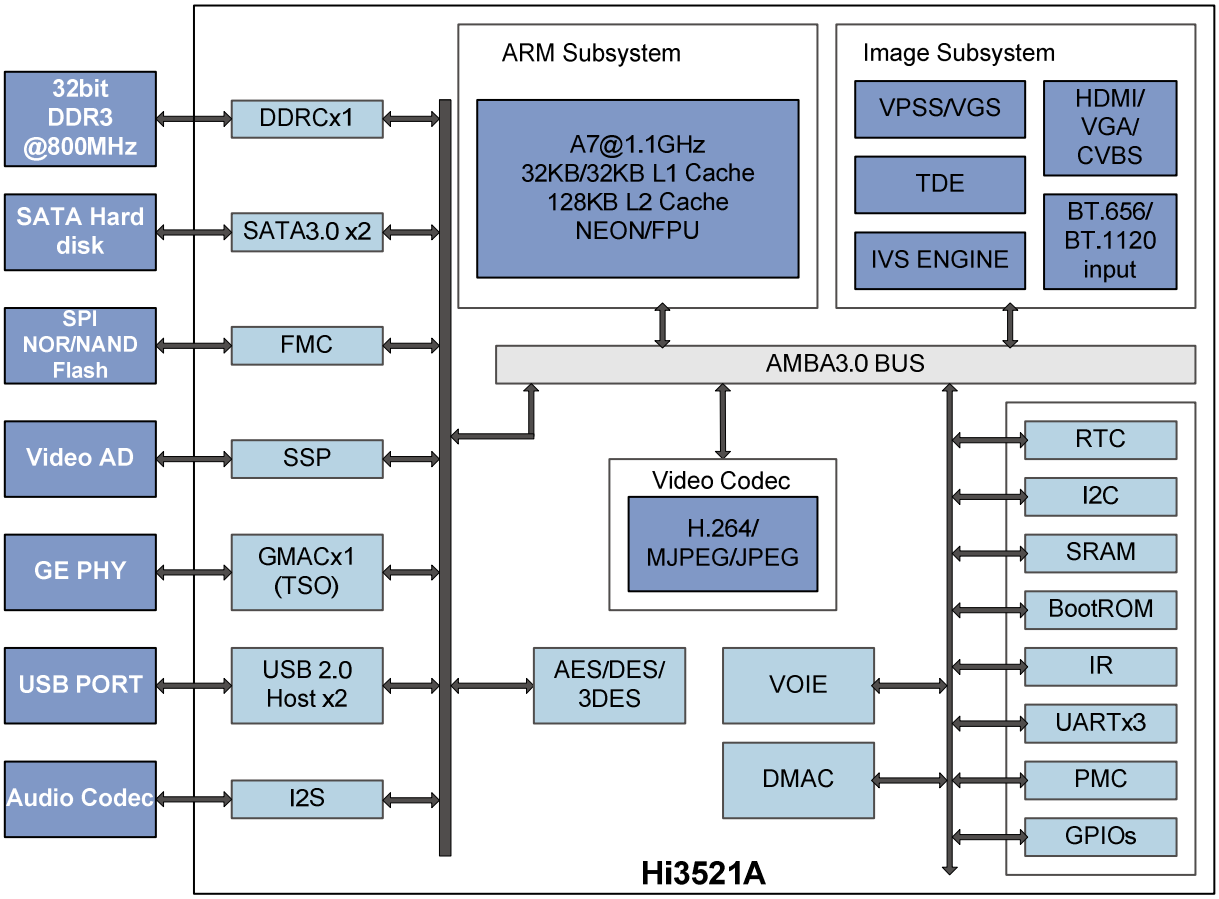
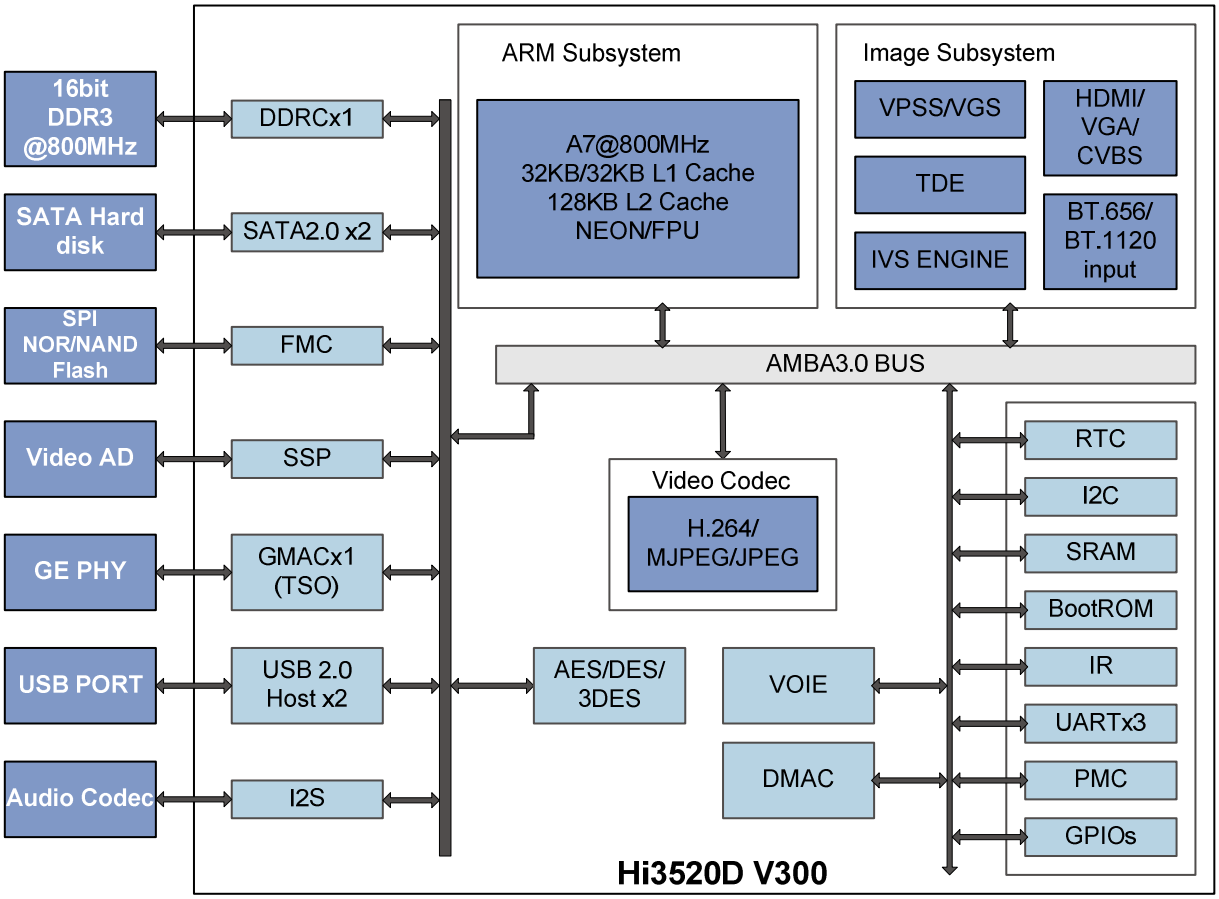


Figure 1-4 shows the logic block diagram of the Hi3520D V300.

Figure 1-4 Logic block diagram of the Hi3520D V300



1.2.2 Processor Core

- ARM Cortex A7@maximum 1.1 GHz (Hi3521A)
  - 32 KB L1 I-cache, 32 KB L1 D-cache
  - 128 KB L2 cache
  - NEON and FPU
- ARM Cortex A7@maximum 800 MHz (Hi3520D V300)
  - 32 KB L1 I-cache, 32 KB L1 D-cache
  - 128 KB L2 cache
  - NEON and FPU

1.2.3 Video Decoding Standards

- H.264 baseline/main/high profile L4.2
- MJPEG/JPEG baseline

1.2.4 Video Encoding Standards

- H.264 Baseline/Main/High profile L5.1
- MJPEG/JPEG baseline

1.2.5 Video Encoding/Decoding

- H.264&JPEG encoding and decoding of multiple streams (Hi3521A)
  - 4x1080p@30 fps H.264 encoding+4xCIF@30 fps H.264 encoding+1x1080p@30 fps H.264 decoding+4x1080p@2 fps JPEG encoding
  - 8x720p@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4x720p@30 fps H.264 decoding+8x720p@2 fps JPEG encoding
  - 16x960H@30 fps H.264 encoding+16xCIF@30 fps H.264 encoding+4x960H@30 fps H.264 decoding+16x960H@2 fps JPEG encoding
  - 16xD1@30 fps H.264 encoding+16xCIF@30 fps H.264 encoding+8xD1@30 fps H.264 decoding+16xD1@2 fps JPEG encoding
  - 5x1080p@30 fps H.264 decoding
  - 10x720p@30 fps H.264 decoding
  - 4x720p@30 fps JPEG decoding
- H.264&JPEG encoding and decoding of multiple streams (Hi3520D V300)
  - 4x720p@30 fps H.264 encoding+4xCIF@30 fps H.264 encoding+4x720p@30 fps H.264 decoding+4x720p@2 fps JPEG encoding
  - 8x960H@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+1x960H@30 fps H.264 decoding+8x960H@2 fps JPEG encoding
  - 8xD1@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4xD1@30 fps H.264 decoding+8xD1@2 fps JPEG encoding
  - 2x1080p@30 fps H.264 decoding
  - 4x720p@30 fps H.264 decoding
  - 4x720p@30 fps JPEG decoding
- CBR or VBR, ranging from 16 kbit/s to 40 Mbit/s
- Fixed QP
- Encoding frame rate ranging from 1/16 fps to full frame rate
- ROI encoding
- Color-to-gray encoding

1.2.6 Intelligent Video Analysis

Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

1.2.7 Video and Graphic Processing

- Deinterlacing, sharpening, 3D denoising, dynamic contrast improvement, and demosaic
- Anti-flicker for output videos and graphics
- 1/8x to 16x video scaling
- 1/2x to 2x graphics scaling
- Four Cover regions
- OSD overlaying of eight regions

1.2.8 Audio Encoding/Decoding

- ADPCM, G.711, and G.726 hardware audio encoding

- Software audio encoding and decoding complying with multiple protocols

1.2.9 Security Engine

AES, DES, and 3DES algorithms implemented by hardware

1.2.10 Video Interfaces

- VI interfaces (Hi3521A)
  - Four 8-bit interfaces or two 16-bit interfaces
  - 108 MHz/144 MHz 4xD1/960H TDM inputs for each 8-bit interface (16xD1/16x960H real-time video inputs in total)
  - 144 MHz/148.5 MHz 2x720p TDM inputs for each 8-bit interface (8x720p@30 fps real-time video inputs in total)
  - 4x720p TDM inputs through 144 MHz/148.5 MHz dual-edge sampling for each 8-bit interface (16x720p@30 fps real-time video inputs in total)
  - 148.5 MHz BT.1120 Y/C interleaved mode for each 8-bit interface (4x1080p@30 fps real-time video inputs in total)
  - 2x1080p TDM inputs through 148.5 MHz dual-edge sampling for each 8-bit interface (8x1080p@30 fps real-time video inputs in total)
  - 148.5 MHz BT.1120 standard mode for the 16-bit interface (1x1080p@60 fps real-time video inputs in total)
- VI interfaces (Hi3520D V300)
  - Two 8-bit interfaces or one 16-bit interface
  - 108 MHz/144 MHz 4xD1/960H TDM inputs for each 8- bit interface (8xD1/8x960H real-time video inputs in total)
  - 144 MHz/148.5 MHz 2x720p TDM inputs for each 8-bit interface (4x720p@30 fps real-time video inputs in total)
  - 4x720p TDM inputs through 148.5 MHz dual-edge sampling for each 8-bit interface (8x720p@30 fps real-time video inputs in total)
  - 2x1080p TDM inputs through 148.5 MHz dual-edge sampling for each 8-bit interface (4x1080p@30 fps real-time video inputs in total)
  - 148.5 MHz BT.1120 Y/C interleaved mode for each 8-bit interface (2x1080p@30 fps real-time video inputs in total)
  - 148.5 MHz BT.1120 standard mode for the 16-bit interface (1x1080p@60 fps real-time video inputs in total)
- VO interfaces
  - HDMI 1.4+VGA+CVBS video outputs
  - HDMI and VGA outputs from the same source
  - Maximum 1080p@60 fps resolution for HDMI or VGA
  - One HD graphics layer and one SD graphics layer in ARGB1555 or ARGB8888 format
  - One hardware cursor layer in ARGB1555 or ARGB8888 format, with the maximum resolution of 128 x 128
  - Alpha blending of the video layer, graphics layer, and cursor layer

1.2.11 Audio Interfaces

- One integrated audio CODEC
- Three unidirectional I2S/PCM interfaces
  - One input, supporting 16 multiplexed inputs
  - Two outputs
- 16-bit audio input and output

1.2.12 Ethernet Ports

- One gigabit Ethernet port
  - RGMII, RMII, and MII modes
  - 10/100 Mbit/s half-duplex or full-duplex
  - 1000 Mbit/s full-duplex
  - TSO for reducing the CPU usage

1.2.13 Peripheral Interfaces

- Two SATA 3.0 interfaces (Hi3521A)
  - PM
  - eSATA
- Two SATA 2.0 interfaces (Hi3520D V300)
  - PM
  - eSATA
- Two USB 2.0 host ports, supporting the hub
- Three UART interfaces, one of which supporting four wires
- One SPI, supporting two CSs
- One IR interface
- One I2C interface
- Multiple GPIO interfaces

1.2.14 Memory Interfaces

- One 32-bit DDR3/DDR3L SDRAM interface (Hi3521A)
  - Maximum frequency of 800 MHz
  - ODT
  - Maximum capacity of 1 GB
  - Automatic power consumption control
- One 16-bit DDR3/DDR3L SDRAM interface (Hi3520D V300)
  - Maximum frequency of 800 MHz
  - ODT
  - Maximum capacity of 512 MB
  - Automatic power consumption control
- SPI NOR/NAND flash interface
  - 1-/2-/4-bit SPI NOR/NAND flash

  - Two CSs, connected to different flash memories
  - Maximum capacity of 32 MB for each CS (only for the NOR flash)
  - Maximum capacity of 4GBits for each CS (only for the SPI NAND flash)
  - 2 KB/4 KB page size (only for the SPI NAND flash)
  - 8-bit/24-bit/1 KB ECC (only for the SPI NAND flash)
- Embedded 4 KB BOOTROM and 16 KB SRAM

1.2.15 RTC with an Independent Power Supply

Independent battery for supplying power to the RTC

1.2.16 Boot Modes

- Booting from the BOOTROM
- Booting from the SPI NOR flash
- Booting from the SPI NAND flash

1.2.17 SDK

- Linux 3.10-based SDK
- Audio encoding and decoding libraries complying with various protocols
- High-performance H.264 PC decoding library

1.2.18 Physical Specifications

- Power consumption (Hi3521A)
  - Typical power consumption of 3 W
  - Multi-level power consumption control
- Power consumption (Hi3520D V300)
  - Typical power consumption of 2.5 W
  - Multi-level power consumption control
- Operating voltages (Hi3521A)
  - 1.1 V core voltage
  - 1.25 V CPU voltage
  - 3.3 V I/O voltage
  - 1.5 V DDR3 SDRAM interface voltage
- Operating voltages (Hi3520D V300)
  - 1.15 V core (including the CPU) voltage
  - 3.3 V I/O voltage
  - 1.5 V DDR3 SDRAM interface voltage
- Package (Hi3521A)
  - RoHS, TFBGA
  - Lead pitch of 0.8 mm (0.03 in.)
  - Body size of 19 mm x 19 mm (0.75 in. x 0.75 in.)
- Package (Hi3520D V300)

  - RoHS, Epad-LQFP256
  - Lead pitch of 0.4 mm (0.02 in.)
  - Body size of 28 mm x 28 mm (1.10 in. x 1.10 in.)
- Operating temperature ranging from 0°C (32°F) to 70°C (158°F)

1.3 Boot Modes

The Hi3521A can boot from:

- BOOTROM
- External SPI NOR flash
- External SPI NAND flash

During power-on reset (POR), the boot mode of the Hi3521A depends on the values of the BOOTROM_SEL signal. Table 1-1 describes the mapping between the signal values and boot modes.

Table 1-1 Mapping between signal values and boot modes

BOOTROM_SEL	Boot Mode
1	Booting from the BOOTROM
0	Booting from the external SPI NOR/NAND flash

NOTE

The BOOTROM_SEL signal is multiplexed with the external pin MDCK.

When the Hi3521A boots from the BOOTROM, the serial port communication mechanism starts, the communication between the serial port and the related software running on the PC is set up, and then the boot program is downloaded. For details, see the *HiTool Burning Tool Application Notes*. If the serial port communication times out, the Hi3521A will boot from the external SPI NAND/NOR flash.

Table 1-2 describes the address space mapping.

Table 1-2 Address space mapping

Start Address	End Address	Function	Capacity	Remarks
0x8000_0000	0xFFFF_FFFF	DDR storage address space	2 GB	-
0x1500_0000	0x7FFF_FFFF	Reserved	-	-
0x1400_0000	0x14FF_FFFF	Address space of the SFC NAND/NOR memory	16 MB	-
0x1316_0000	0x131F_FFFF	Reserved	-	-
0x1315_0000	0x1315_FFFF	MDU register	64 KB	-

Start Address	End Address	Function	Capacity	Remarks
0x1314_0000	0x1314_FFFF	AIAO register	64 KB	-
0x1313_0000	0x1313_FFFF	JPGE register	64 KB	-
0x1312_0000	0x1312_FFFF	VOIE register	64 KB	-
0x1311_0000	0x1311_FFFF	VPSS register	64 KB	-
0x1310_0000	0x1310_FFFF	AVC1 register	64 KB	-
0x130C_0000	0x130F_FFFF	VICAP register	256 KB	-
0x1309_0000	0x130E_FFFF	Reserved	-	-
0x1308_0000	0x1308_FFFF	VGS register	64 KB	-
0x1307_0000	0x1307_FFFF	JPGD register	64 KB	-
0x1306_0000	0x1306_FFFF	IVE register	64 KB	-
0x1305_0000	0x1305_FFFF	TDE register	64 KB	-
0x1304_0000	0x1304_FFFF	AVC0 register	64 KB	-
0x1303_0000	0x1303_FFFF	Reserved	-	-
0x1302_0000	0x1302_FFFF	VDP register	64 KB	-
0x1301_0000	0x1301_FFFF	HDMI register	64 KB	-
0x1300_0000	0x1300_FFFF	Reserved	-	-
0x1223_0000	0x12FF_FFFF	Reserved	-	-
0x1222_0000	0x1222_FFFF	GPIO13 register	64 KB	-
0x1221_0000	0x1221_FFFF	GPIO12 register	64 KB	-
0x1220_0000	0x1220_FFFF	GPIO11 register	64 KB	-
0x121F_0000	0x121F_FFFF	GPIO10 register	64 KB	-
0x121E_0000	0x121E_FFFF	GPIO9 register	64 KB	-
0x121D_0000	0x121D_FFFF	GPIO8 register	64 KB	-
0x121C_0000	0x121C_FFFF	GPIO7 register	64 KB	-
0x121B_0000	0x121B_FFFF	GPIO6 register	64 KB	-
0x121A_0000	0x121A_FFFF	GPIO5 register	64 KB	-
0x1219_0000	0x1219_FFFF	GPIO4 register	64 KB	-
0x1218_0000	0x1218_FFFF	GPIO3 register	64 KB	-
0x1217_0000	0x1217_FFFF	GPIO2 register	64 KB	-
0x1216_0000	0x1216_FFFF	GPIO1 register	64 KB	-

Start Address	End Address	Function	Capacity	Remarks
0x1215_0000	0x1215_FFFF	GPIO0 register	64 KB	-
0x1214_0000	0x1214_FFFF	IR register	64 KB	-
0x1213_0000	0x1213_FFFF	Reserved	-	-
0x1212_0000	0x1212_FFFF	Peripheral control register	64 KB	-
0x1211_0000	0x1211_FFFF	DDRC register	64 KB	-
0x1210_0000	0x1210_0FFF	DDRT0 register	64 KB	-
0x120F_0800	0x120F_FFFF	Pin control register	32 KB	-
0x120F_0000	0x120F_7FFF	Pin multiplexing register	32 KB	-
0x120E_0000	0x120E_FFFF	PMC register	64 KB	-
0x120D_0000	0x120D_FFFF	SSP register	64 KB	-
0x120C_0000	0x120C_FFFF	I^2C register	64 KB	-
0x120B_0000	0x120B_FFFF	RTC register	64 KB	-
0x120A_0000	0x120A_FFFF	UART2 register	64 KB	-
0x1209_0000	0x1209_FFFF	UART1 register	64 KB	-
0x1208_0000	0x1208_FFFF	UART0 register	64 KB	-
0x1207_0000	0x1207_FFFF	WDG register	64 KB	-
0x1206_0000	0x1206_FFFF	Reserved	-	-
0x1205_0000	0x1205_FFFF	System control register	64 KB	-
0x1204_0000	0x1204_FFFF	CRG register	64 KB	-
0x1203_0000	0x1203_FFFF	Timer6/Timer7 register	64 KB	-
0x1202_0000	0x1202_FFFF	Timer4/Timer5 register	64 KB	
0x1201_0000	0x1201_FFFF	Timer2/Timer3 register	64 KB	-
0x1200_0000	0x1200_FFFF	Timer0/Timer1 register	64 KB	-
0x1102_0000	0x11FF_FFFF	Reserved	-	
0x1101_0000	0x1101_FFFF	SATA 3.0 register	64 KB	
0x1100_0000	0x1100_FFFF	Reserved	-	
0x100B_0000	0x10FF_FFFF	Reserved	-	
0x100A_0000	0x100A_FFFF	GSF register	64 KB	
0x1009_0000	0x1009_FFFF	Reserved	-	
0x1008_0000	0x1008_FFFF	SCD register	64 KB	

Start Address	End Address	Function	Capacity	Remarks
0x1007_0000	0x1007_FFFF	Cipher register	64 KB	-
0x1006_0000	0x1006_FFFF	DMAC register	64 KB	-
0x1005_0000	0x1005_FFFF	Reserved	-	-
0x1004_0000	0x1004_FFFF	USB 2.0 host EHCI register	64 KB	-
0x1003_0000	0x1003_FFFF	USB 2.0 host OHCI register	64 KB	-
0x1001_0000	0x1002_FFFF	Reserved	-	-
0x1000_0000	0x1000_FFFF	FMC register	64 KB	-
0x0402_0000	0x0FFF_FFFF	Reserved	-	-
0x0401_0000	0x0401_FFFF	Address space of the on-chip RAM	64 KB	The actual RAM capacity is only 16 KB.
0x0400_0000	0x0400_FFFF	BOOTROM address space	64 KB	The actual ROM capacity is only 4 KB.
0x0000_0000	0x03FF_FFFF	During address remapping, the address space points to the boot address space. After address remapping is cleared, the address space points to the on-chip RAM.	64 MB	-

Contents

Figures

Tables

2 Hardware

2.1 Package and Pinout

2.1.1 Package

Hi3520D V300 uses the exposed pad (Epad) low-profile quad flat (LQFP) package. It has 256 pins, its body size is 28 mm x 28 mm (1.10 in. x 1.10 in.), and its lead pitch is 0.8 mm (0.03 in.). Figure 2-1 to Figure 2-3 show the package of Hi3520D V300. Table 2-1 shows the package specifications.

Figure 2-1 Top view

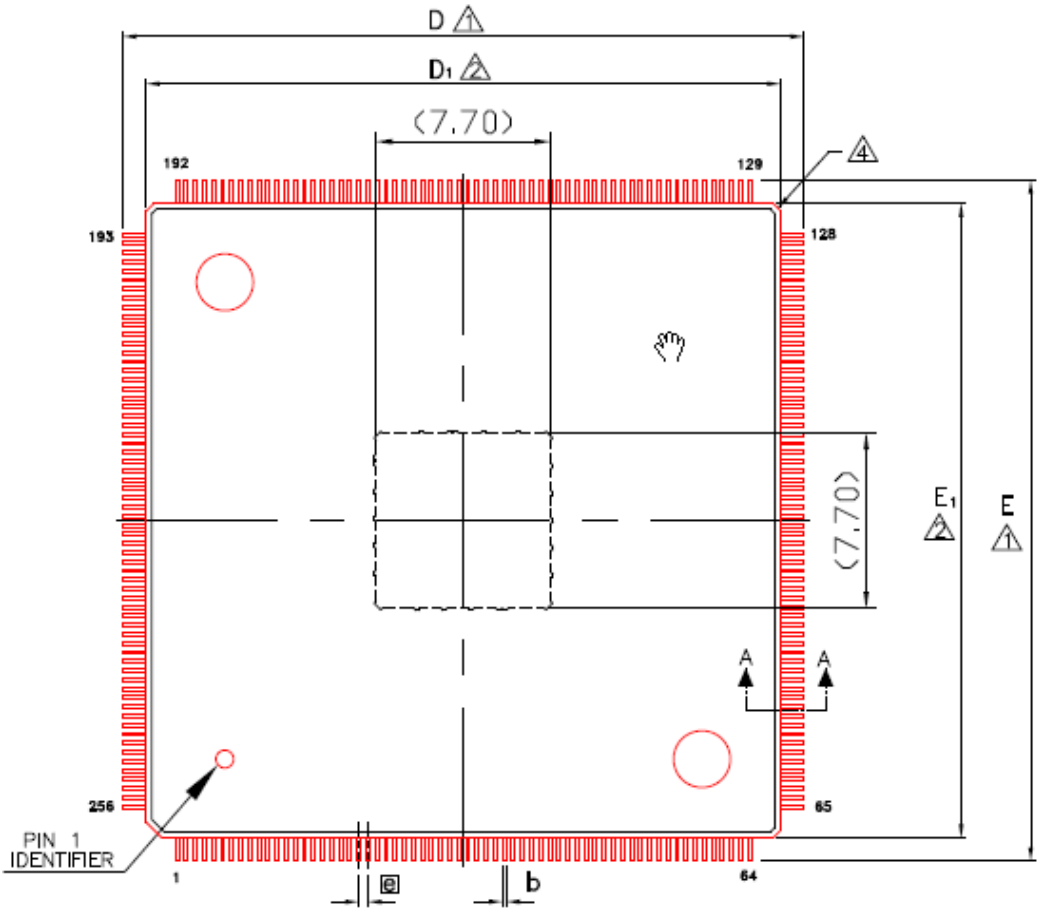


Figure 2-2 Side view

Figure 2-3 Enlarged view of detail "A"

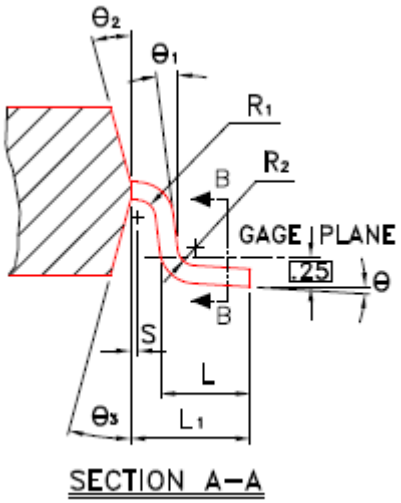


Figure 2-4 Enlarged view of detail "B"

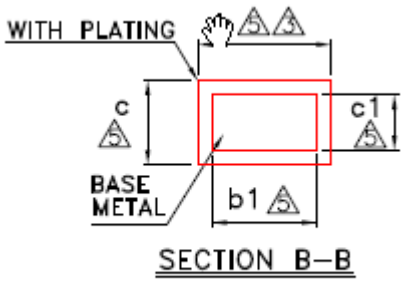


Table 2-1 Package dimensions

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.025	—	0.127	0.001	—	0.005
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.12	—	0.20	0.005	—	0.008
c_1	0.13 REF			0.005 REF		
D	29.85	30.00	30.15	1.175	1.181	1.187
D_1	27.90	28.00	28.10	1.098	1.102	1.106
E	29.85	30.00	30.15	1.175	1.181	1.187
E_1	27.90	28.00	28.10	1.098	1.102	1.106
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.15 REF			0.006 REF		
R_2	0.15 REF			0.006 REF		
S	0.21 REF			0.008 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	7° REF			7° REF		
$θ_2$	12° REF			12° REF		
$θ_3$	12° REF			12° REF		
ccc	0.08			0.003		

2.1.2 Pinout

Table 2-2 lists the pin quantity of Hi3520D V300 by type.

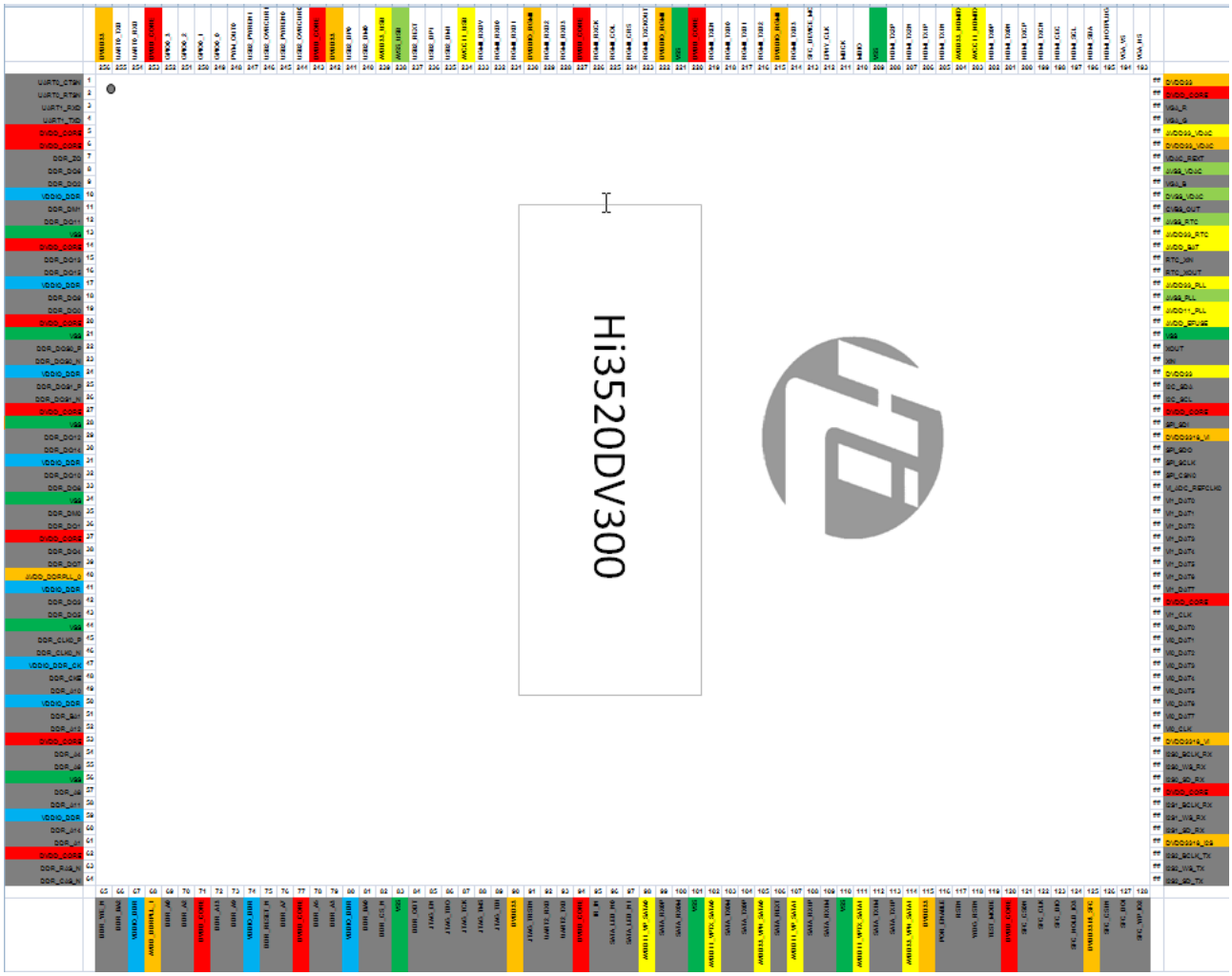
Table 2-2 Pin quantity

Pin Type	Quantity
I/O	176
Digital power	46
Digital GND	12
Others/Analog power	17
Others/Analog GND	0
DDR reference power	5
Total	256

Pin Map

Figure 2-5 shows pin maps.

Figure 2-5 Pin map (top view)



Pin Arrangement

Table 2-3 lists the pins of Hi3520D V300 based on their positions.

Table 2-3 Pin arrangement

Position	Pin Name	Position	Pin Name
1	UART0_CTSN	129	I2S2_SD_TX
2	UART0_RTSN	130	I2S2_WS_TX
3	UART1_RXD	131	I2S2_BCLK_TX
4	UART1_TXD	132	DVDD3318_I2S

Position	Pin Name	Position	Pin Name
5	DVDD_CORE	133	I2S1_SD_RX
6	DVDD_CORE	134	I2S1_WS_RX
7	DDR_ZQ	135	I2S1_BCLK_RX
8	DDR_DQ6	136	DVDD_CORE
9	DDR_DQ2	137	I2S0_SD_RX
10	VDDIO_DDR	138	I2S0_WS_RX
11	DDR_DM1	139	I2S0_BCLK_RX
12	DDR_DQ11	140	DVDD3318_VI
13	VSS	141	VI0_CLK
14	DVDD_CORE	142	VI0_DAT7
15	DDR_DQ13	143	VI0_DAT6
16	DDR_DQ15	144	VI0_DAT5
17	VDDIO_DDR	145	VI0_DAT4
18	DDR_DQ9	146	VI0_DAT3
19	DDR_DQ0	147	VI0_DAT2
20	DVDD_CORE	148	VI0_DAT1
21	VSS	149	VI0_DAT0
22	DDR_DQS0_P	150	VI1_CLK
23	DDR_DQS0_N	151	DVDD_CORE
24	VDDIO_DDR	152	VI1_DAT7
25	DDR_DQS1_P	153	VI1_DAT6
26	DDR_DQS1_N	154	VI1_DAT5
27	DVDD_CORE	155	VI1_DAT4
28	VSS	156	VI1_DAT3
29	DDR_DQ12	157	VI1_DAT2
30	DDR_DQ14	158	VI1_DAT1
31	VDDIO_DDR	159	VI1_DAT0
32	DDR_DQ10	160	VI_ADC_REFCLK0
33	DDR_DQ8	161	SPI_CSN0
34	VSS	162	SPI_SCLK
35	DDR_DM0	163	SPI_SDO

Position	Pin Name	Position	Pin Name
36	DDR_DQ1	164	DVDD3318_VI
37	DVDD_CORE	165	SPI_SDI
38	DDR_DQ4	166	DVDD_CORE
39	DDR_DQ7	167	I2C_SCL
40	AVDD_DDRPLL_0	168	I2C_SDA
41	VDDIO_DDR	169	DVDD33
42	DDR_DQ3	170	XIN
43	DDR_DQ5	171	XOUT
44	VSS	172	VSS
45	DDR_CLK0_P	173	AVDD_EFUSE
46	DDR_CLK0_N	174	AVDD_PLL
47	VDDIO_DDR_CK	175	AVSS_PLL
48	DDR_CKE	176	AVDD33_PLL
49	DDR_A10	177	RTC_XOUT
50	VDDIO_DDR	178	RTC_XIN
51	DDR_BA1	179	AVDD_BAT
52	DDR_A12	180	AVDD33_RTC
53	DVDD_CORE	181	AVSS_RTC
54	DDR_A4	182	CVBS_OUT
55	DDR_A6	183	DVSS_VDAC
56	VSS	184	VGA_B
57	DDR_A8	185	AVSS_VDAC
58	DDR_A11	186	VDAC_REXT
59	VDDIO_DDR	187	DVDD33_VDAC
60	DDR_A14	188	AVDD33_VDAC
61	DDR_A1	189	VGA_G
62	DVDD_CORE	190	VGA_R
63	DDR_RAS_N	191	DVDD_CORE
64	DDR_CAS_N	192	DVDD33
65	DDR_WE_N	193	VGA_HS
66	DDR_BA2	194	VGA_VS

Position	Pin Name	Position	Pin Name
67	VDDIO_DDR	195	HDMI_HOTPLUG
68	AVDD_DDRPLL_1	196	HDMI_SDA
69	DDR_A0	197	HDMI_SCL
70	DDR_A2	198	HDMI_CEC
71	DVDD_CORE	199	HDMI_TXCN
72	DDR_A13	200	HDMI_TXCP
73	DDR_A9	201	HDMI_TX0N
74	VDDIO_DDR	202	HDMI_TX0P
75	DDR_RESET_N	203	AVCC_HDMITX
76	DDR_A7	204	AVDD33_HDMITX
77	DVDD_CORE	205	HDMI_TX1N
78	DDR_A5	206	HDMI_TX1P
79	DDR_A3	207	HDMI_TX2N
80	VDDIO_DDR	208	HDMI_TX2P
81	DDR_BA0	209	VSS
82	DDR_CS_N	210	MDIO
83	VSS	211	MDCK
84	DDR_ODT	212	EPHY_CLK
85	JTAG_EN	213	SFC_DEVICE_MODE
86	JTAG_TDO	214	RGMII_TXD3
87	JTAG_TCK	215	DVDDIO_RGMII
88	JTAG_TMS	216	RGMII_TXD2
89	JTAG_TDI	217	RGMII_TXD1
90	DVDD33	218	RGMII_TXD0
91	JTAG_TRSTN	219	RGMII_TXEN
92	UART2_RXD	220	DVDD_CORE
93	UART2_TXD	221	VSS
94	DVDD_CORE	222	DVDDIO_RGMII
95	IR_IN	223	RGMII_TXCKOUT
96	SATA_LED_N0	224	RGMII_CRS
97	SATA_LED_N1	225	RGMII_COL

Position	Pin Name	Position	Pin Name
98	AVDD_VP_SATA0	226	RGMII_RXCK
99	SATA_RX0P	227	DVDD_CORE
100	SATA_RX0M	228	RGMII_RXD3
101	VSS	229	RGMII_RXD2
102	AVDD_VPTX_SATA0	230	DVDDIO_RGMII
103	SATA_TX0M	231	RGMII_RXD1
104	SATA_TX0P	232	RGMII_RXD0
105	AVDD33_VPH_SATA0	233	RGMII_RXDV
106	SATA_REXT	234	AVCC_USB
107	AVDD_VP_SATA1	235	USB2_DM1
108	SATA_RX1P	236	USB2_DP1
109	SATA_RX1M	237	USB2_REXT
110	VSS	238	AVSS_USB
111	AVDD_VPTX_SATA1	239	AVDD33_USB
112	SATA_TX1M	240	USB2_DM0
113	SATA_TX1P	241	USB2_DP0
114	AVDD33_VPH_SATA1	242	DVDD33
115	DVDD33	243	DVDD_CORE
116	POR_ENABLE	244	USB2_OVRCUR0
117	RSTN	245	USB2_PWREN0
118	WDG_RSTN	246	USB2_OVRCUR1
119	TEST_MODE	247	USB2_PWREN1
120	DVDD_CORE	248	PWM_OUT0
121	SFC_CS0N	249	GPIO0_0
122	SFC_CLK	250	GPIO0_1
123	SFC_DIO	251	GPIO0_2
124	SFC_HOLD_IO3	252	GPIO0_3
125	DVDD3318_SFC	253	DVDD_CORE
126	SFC_CS1N	254	UART0_RXD
127	SFC_DOI	255	UART0_TXD
128	SFC_WP_IO2	256	DVDD33

2.2 Pin Description

2.2.1 Pin Types

Table 2-4 describes the I/O pin types.

Table 2-4 I/O types

I/O	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with a Schmitt trigger
I_{SPD}	Input signal with a Schmitt trigger, internal pull-down
I_{SPU}	Input signal with a Schmitt trigger, internal pull-up
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (input/output) signal
I_{PD}/O	Bidirectional signal, input pull-down
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPU}/O	Bidirectional signal with a Schmitt trigger, input pull-up
I_{SPD}/O	Bidirectional signal with Schmitt trigger, input pull-down
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD
I_S/O	Bidirectional signal, input with a Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with a Schmitt trigger and output OD
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground (GND)

2.2.2 Pin Details

NOTE

- The drive current of pins with the symbol of "CFG" in the **Drive Current (mV)** column can be configured in the pin drive capability register. When the CFG pin is used as the output pin, the default drive current is determined by the default value of the pin drive capability register.
- Pins with the symbol of "5 V tol" in the **Voltage (V)** column support the 5 V tolerance.

VDAC Pins

Table 2-5 describes video digital-to-analog converter (VDAC) pins.

Table 2-5 VDAC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
182	CVBS_OUT	O	-	-	CVBS channel output
186	VDAC_REXT	I/O	-	-	VDAC reference current. A 12 kΩ resistor is recommended.
184	VGA_B	O	-	-	B channel output of the VGA
189	VGA_G	O	-	-	G channel output of the VGA
190	VGA_R	O	-	-	R channel output of the VGA
193	VGA_HS	I/O	CFG	3.3	Function 0: GPIO11_6 General-purpose input/output (GPIO) Function 1: VGA_HS VGA row sync output
194	VGA_VS	I/O	CFG	3.3	Function 0: GPIO11_3 GPIO Function 1: VGA_VS VGA field sync output

HDMI Pins

Table 2-6 describes high definition multimedia interface (HDMI) pins.

Table 2-6 HDMI pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
198	HDMI_CEC	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO13_5 GPIO Function 1: HDMI_CEC Consumer electronics control (CEC) channel signal of the HDMI
195	HDMI_HOTPLUG	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO13_4 GPIO Function 1: HDMI_HOTPLUG Hot plug detection signal of the HDMI
197	HDMI_SCL	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO13_7 GPIO Function 1: HDMI_SCL Display data channel (DDC) clock signal of the HDMI
196	HDMI_SDA	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO13_6 GPIO Function 1: HDMI_SDA DDC data/address signal of the HDMI
201	HDMI_TX0N	O	-	-	Negative terminal of the serial differential signal of HDMI TX channel 0
202	HDMI_TX0P	O	-	-	Positive terminal of the serial differential signal of HDMI TX channel 0
205	HDMI_TX1N	O	-	-	Negative terminal of the serial differential signal of HDMI TX channel 1
206	HDMI_TX1P	O	-	-	Positive terminal of the serial differential signal of HDMI TX channel 1

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
207	HDMI_TX2N	O	-	-	Negative terminal of the serial differential signal of HDMI TX channel 2
208	HDMI_TX2P	O	-	-	Positive terminal of the serial differential signal of HDMI TX channel 2
199	HDMI_TXCN	O	-	-	Negative terminal of the HDMI TX differential pixel clock
200	HDMI_TXCP	O	-	-	Positive terminal of the HDMI TX differential pixel clock

DDR Pins

Table 2-7 describes double data rate (DDR) pins.

Table 2-7 DDR pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
69	DDR_A0	O	-	1.5/1.35	DDR SDRAM address 0
61	DDR_A1	O	-	1.5/1.35	DDR SDRAM address 1
70	DDR_A2	O	-	1.5/1.35	DDR SDRAM address 2
79	DDR_A3	O	-	1.5/1.35	DDR SDRAM address 3
54	DDR_A4	O	-	1.5/1.35	DDR SDRAM address 4
78	DDR_A5	O	-	1.5/1.35	DDR SDRAM address 5
55	DDR_A6	O	-	1.5/1.35	DDR SDRAM address 6
76	DDR_A7	O	-	1.5/1.35	DDR SDRAM address 7
57	DDR_A8	O	-	1.5/1.35	DDR SDRAM address 8
73	DDR_A9	O	-	1.5/1.35	DDR SDRAM address 9
49	DDR_A10	O	-	1.5/1.35	DDR SDRAM address 10

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
58	DDR_A11	O	-	1.5/1.35	DDR SDRAM address 11
52	DDR_A12	O	-	1.5/1.35	DDR SDRAM address 12
72	DDR_A13	O	-	1.5/1.35	DDR SDRAM address 13
60	DDR_A14	O	-	1.5/1.35	DDR SDRAM address 14
81	DDR_BA0	O	-	1.5/1.35	Bank address signal 0 of the DDR SDRAM
51	DDR_BA1	O	-	1.5/1.35	Bank address signal 1 of the DDR SDRAM
66	DDR_BA2	O	-	1.5/1.35	Bank address signal 2 of the DDR SDRAM
64	DDR_CAS_N	O	-	1.5/1.35	Column address select signal of the DDR SDRAM
48	DDR_CKE	O	-	1.5/1.35	Clock enable signal of the DDR SDRAM
46	DDR_CLK0_N	O	-	1.5/1.35	(Negative) differential clock of the DDR SDRAM
45	DDR_CLK0_P	O	-	1.5/1.35	(Positive) differential clock of the DDR SDRAM
82	DDR_CS_N	O	-	1.5/1.35	Chip select (CS) signal of the DDR SDRAM
35	DDR_DM0	I/O	-	1.5/1.35	Data mask signal 0 of the DDR SDRAM
11	DDR_DM1	I/O	-	1.5/1.35	Data mask signal 1 of the DDR SDRAM
19	DDR_DQ0	I/O	-	1.5/1.35	DDR SDRAM data 0
36	DDR_DQ1	I/O	-	1.5/1.35	DDR SDRAM data 1
9	DDR_DQ2	I/O	-	1.5/1.35	DDR SDRAM data 2
42	DDR_DQ3	I/O	-	1.5/1.35	DDR SDRAM data 3
38	DDR_DQ4	I/O	-	1.5/1.35	DDR SDRAM data 4
43	DDR_DQ5	I/O	-	1.5/1.35	DDR SDRAM data 5
8	DDR_DQ6	I/O	-	1.5/1.35	DDR SDRAM data 6

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
39	DDR_DQ7	I/O	-	1.5/1.35	DDR SDRAM data 7
33	DDR_DQ8	I/O	-	1.5/1.35	DDR SDRAM data 8
18	DDR_DQ9	I/O	-	1.5/1.35	DDR SDRAM data 9
32	DDR_DQ10	I/O	-	1.5/1.35	DDR SDRAM data 10
12	DDR_DQ11	I/O	-	1.5/1.35	DDR SDRAM data 11
29	DDR_DQ12	I/O	-	1.5/1.35	DDR SDRAM data 12
15	DDR_DQ13	I/O	-	1.5/1.35	DDR SDRAM data 13
30	DDR_DQ14	I/O	-	1.5/1.35	DDR SDRAM data 14
16	DDR_DQ15	I/O	-	1.5/1.35	DDR SDRAM data 15
23	DDR_DQS0_N	I/O	-	1.5/1.35	(Negative) data strobe (DQS) signal 0 of the DDR SDRAM, corresponding to DDR_DQ0−DDR_DQ7
22	DDR_DQS0_P	I/O	-	1.5/1.35	(Positive) data strobe (DQS) signal 0 of the DDR SDRAM, corresponding to DDR_DQ0−DDR_DQ7
26	DDR_DQS1_N	I/O	-	1.5/1.35	(Negative) data strobe (DQS) signal 1 of the DDR SDRAM, corresponding to DDR_DQ8−DDR_DQ15
25	DDR_DQS1_P	I/O	-	1.5/1.35	(Positive) data strobe (DQS) signal 1 of the DDR SDRAM, corresponding to DDR_DQ8−DDR_DQ15
84	DDR_ODT	I/O	-	1.5/1.35	Matched termination resistor of the DDR SDRAM
63	DDR_RAS_N	O	-	1.5/1.35	Row address select signal of the DDR SDRAM
75	DDR_RESET_N	O	-	1.5/1.35	Reset signal of the DDR SDRAM
65	DDR_WE_N	O	-	1.5/1.35	Write enable signal of the DDR SDRAM

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
7	DDR_ZQ	I/O	-	1.5/1.35	ZQ calibration signal of the DDR SDRAM

RGMII Pins

Hi3520D V300 Ethernet port supports the reduced gigabit media independent interface (RGMII), reduced media independent interface (RMII), and media independent interface (MII) modes. Table 2-8 describes the functions of RGMII pins in each mode.

Table 2-8 Functions of RGMII pins in three modes

Pin Name	RGMII Mode	MII Mode	RMII Mode
RGMII_COL	-	Conflict detection	-
RGMII_CRS	-	Carrier detection	-
RGMII_RXCK	RX clock	RX clock	-
RGMII_RXD0	RX data 0	RX data 0	RX data 0
RGMII_RXD1	RX data 1	RX data 1	RX data 1
RGMII_RXD2	RX data 2	RX data 2	-
RGMII_RXD3	RX data 3	RX data 3	-
RGMII_RXDV	RX data validity	RX data validity	RX data validity/carrier detection
RGMII_TXCKOUT	TX clock	TX clock	Reference clock
RGMII_TXD0	TX data 0	TX data 0	TX data 0
RGMII_TXD1	TX data 1	TX data 1	TX data 1
RGMII_TXD2	TX data 2	TX data 2	-
RGMII_TXD3	TX data 3	TX data 3	-
RGMII_TXEN	TX data enable	TX data enable	TX data enable

Table 2-9 describes RGMII pins.

Table 2-9 RGMII pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
212	EPHY_CLK	I/O	CFG	3.3	Function 0: GPIO6_6 GPIO Function 1: EPHY_CLK Working clock of the Ethernet PHY
225	RGMII_COL	I_{PD}/O	CFG	3.3	Function 0: GPIO8_5 GPIO Function 1: RGMII_COL Conflict detection signal in MII mode
224	RGMII_CRS	I_{PD}/O	CFG	3.3	Function 0: GPIO8_4 GPIO Function 1: RGMII_CRS Carrier sense signal in MII mode
226	RGMII_RXCK	I/O	CFG	3.3	Function 0: GPIO7_5 GPIO Function 1: RGMII_RXCK RX clock in RGMII or MII mode
232	RGMII_RXD0	I/O	CFG	3.3	Function 0: GPIO7_4 GPIO Function 1: RGMII_RXD0 RX data 0 in RGMII, MII, or RMII mode
231	RGMII_RXD1	I/O	CFG	3.3	Function 0: GPIO7_3 GPIO Function 1: RGMII_RXD1 RX data 1 in RGMII, MII, or RMII mode
229	RGMII_RXD2	I/O	CFG	3.3	Function 0: GPIO7_2 GPIO Function 1: RGMII_RXD2 RX data 2 in RGMII or MII mode
228	RGMII_RXD	I/O	CFG	3.3	Function 0: GPIO7_1 GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
	3				Function 1: RGMII_RXD3 RX data 3 in RGMII or MII mode
233	RGMII_RXDV	I/O	CFG	3.3	Function 0: GPIO7_0 GPIO Function 1: RGMII_RXDV RX data validity signal in RGMII or MII mode RX data validity and carrier detection signals in RMII mode
223	RGMII_TXCKOUT	I/O	CFG	3.3	Function 0: GPIO8_3 GPIO Function 1: RGMII_TXCKOUT TX clock (active on both edges) in RGMII gigabit mode Function 2: MII_TXCK TX clock in MII mode Function 3: RMII_CLK Reference clock in RMII mode
218	RGMII_TXD0	I/O	CFG	3.3	Function 0: GPIO8_2 GPIO Function 1: RGMII_TXD0 TX data 0 in RGMII, MII, or RMII mode
217	RGMII_TXD1	I/O	CFG	3.3	Function 0: GPIO8_1 GPIO Function 1: RGMII_TXD1 TX data 1 in RGMII, MII, or RMII mode
216	RGMII_TXD2	I/O	CFG	3.3	Function 0: GPIO8_0 GPIO Function 1: RGMII_TXD2 TX data 2 in RGMII or MII mode
214	RGMII_TXD3	I/O	CFG	3.3	Function 0: GPIO7_7 GPIO Function 1: RGMII_TXD3

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					TX data 3 in RGMII or MII mode
219	RGMII_TXEN	I/O	CFG	3.3	Function 0: GPIO7_6 GPIO Function 1: RGMII_TXEN TX data validity signal in RGMII, MII, or RMII mode

MDIO Pins

Table 2-10 describes management data input/output (MDIO) pins.

Table 2-10 MDIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
211	MDCK	I_{PD}/O	CFG	3.3	Function 0: GPIO10_0 GPIO Function 1: MDCK MIDO interface clock output Function 2: BOOTROM_SEL BOOTROM boot 0: boot from the SPI flash 1: boot from the BOOTROM
210	MDIO	I/O	CFG	3.3	Function 0: GPIO10_1 GPIO Function 1: MDIO Input/Output signal of the MDIO interface

I2C Pins

Table 2-11 describes inter-integrated circuit (I^2C) pins.

Table 2-11 I^2C pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
167	I2C_SCL	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO12_7 GPIO Function 1: I2C_SCL I^2C bus clock
168	I2C_SDA	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO12_6 GPIO Function 1: I2C_SDA I^2C bus data/address

IR Pins

Table 2-12 describes the infrared (IR) pin.

Table 2-12 IR pin

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
95	IR_IN	I_{PU} /O	CFG	3.3 (5 V tol)	Function 0: GPIO10_2 GPIO Function 1: IR_IN IR input signal

PWM Pins

Table 2-13 describes pulse-width modulation (PWM) pins.

Table 2-13 PWM pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
248	PWM_OUT0	I/O	CFG	DVDDIO_33	Function 0: PWM_OUT0 PWM output 0 Function 1: GPIO5_5 GPIO

SFC Pins

Table 2-14 describes SFC pins.

Table 2-14 SFC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
122	SFC_CLK	I_{PD}/O	CFG	3.3/1.8	Function 0: SFC_CLK Clock of the SPI NAND/NOR flash Function 1: SFC_BOOT_MODE Boot address mode of the SPI NOR flash when SFC_DEVICE_MODE is 0 0: 3-byte address mode 1: 4-byte address mode Boot mode of the SPI NAND flash when SFC_DEVICE_MODE is 1 0: 1-wire boot mode 1: 4-wire boot mode
121	SFC_CS0N	I/O	CFG	3.3/1.8	CS0 signal of the SPI NAND/NOR flash, active low
126	SFC_CS1N	I/O	CFG	3.3/1.8	CS1 signal of the SPI NAND/NOR flash, active low
123	SFC_DIO	I/O	CFG	3.3/1.8	Function 0: SFC_DIO Data output signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode Function 1: GPIO11_0 GPIO
127	SFC_DOI	I/O	CFG	3.3/1.8	Function 0: SFC_DOI Data input signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: GPIO11_2 GPIO
124	SFC_HOLD_IO3	I/O	CFG	3.3/1.8	Hold function in standard SPI mode, active low Hold function in dual-SPI mode, active low Data I/O signal in quad-SPI mode
128	SFC_WP_IO2	I/O	CFG	3.3/1.8	Function 0: SFC_WP_IO2 Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal in quad-SPI mode Function 1: GPIO11_1 GPIO

UART Pins

Table 2-15 describes universal asynchronous receiver transmitter (UART) pins.

Table 2-15 UART pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
1	UART0_CTSN	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: UART0_CTSN UART0 clear-to-send (CTS) signal, active low Function 1: GPIO6_2 GPIO
2	UART0_RTSN	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: UART0_RTSN UART0 request to send (RTS) signal, active low Function 1: GPIO6_3 GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
254	UART0_RXD	I_{PU} /O	CFG	DVDDIO_33 (5 V tol)	Function 0: UART0_RXD UART0 RX data Function 1: GPIO10_7 GPIO
255	UART0_TXD	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: UART0_TXD UART0 TX data Function 1: GPIO12_5 GPIO
3	UART1_RXD	I_{PU} /O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO6_5 GPIO Function 1: UART1_RXD UART1 RX data
4	UART1_TXD	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO6_7 GPIO Function 1: UART1_TXD UART1 TX data
92	UART2_RXD	I_{PU} /O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO11_4 GPIO Function 1: UART2_RXD UART2 RX data
93	UART2_TXD	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO11_5 GPIO Function 1: UART2_TXD UART2 TX data

SATA Pins

Table 2-16 describes serial advanced technology attachment (SATA) pins.

Table 2-16 SATA pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
96	SATA_LED_N0	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO10_3 GPIO Function 1: SATA_LED_N0 Light emitting diode (LED) indicator of SATA port 0, active low
97	SATA_LED_N1	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO10_4 GPIO Function 1: SATA_LED_N1 LED indicator of SATA port 1, active low
100	SATA_RX0M	I	-	-	Negative terminal of the RX differential signal of SATA port 0
99	SATA_RX0P	I	-	-	Positive terminal of the RX differential signal of SATA port 0
103	SATA_TX0M	O	-	-	Negative terminal of the TX differential signal of SATA port 0
104	SATA_TX0P	O	-	-	Positive terminal of the TX differential signal of SATA port 0
109	SATA_RX1M	I	-	-	Negative terminal of the RX differential signal of SATA port 1
108	SATA_RX1P	I	-	-	Positive terminal of the RX differential signal of SATA port 1
112	SATA_TX1M	O	-	-	Negative terminal of the TX differential signal of SATA port 1
113	SATA_TX1P	O	-	-	Positive terminal of the TX differential signal of SATA port 1
106	SATA_REXT	I/O			External resistor of the SATA port. A 200±1% resistor is recommended.

USB2 Pins

Table 2-17 describes USB 2.0 pins.

Table 2-17 USB 2.0 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
240	USB2_DM0	I/O	-	-	Negative terminal of the data signal of USB 2.0 port 0
235	USB2_DM1	I/O	-	-	Negative terminal of the data signal of USB 2.0 port 1
241	USB2_DP0	I/O	-	-	Positive terminal of the data signal of USB 2.0 port 0
236	USB2_DP1	I/O	-	-	Positive terminal of the data signal of USB 2.0 port 1
244	USB2_OVRCUR0	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO13_0 GPIO Function 1: SB2_OVRCUR0 Overcurrent indicator of USB port 0, configurable level, and active high by default
246	USB2_OVRCUR1	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO13_2 GPIO Function 1: USB2_OVRCUR1 Overcurrent indicator of USB port 1, configurable level, and active high by default
245	USB2_PWREN0	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO13_1 GPIO Function 1:

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					USB2_PWREN0 Power control output signal of USB port 0, configurable level, and active low by default
247	USB2_PWREN1	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO13_3 GPIO Function 1: USB2_PWREN1 Power control output signal of USB port 1, configurable level, and active low by default
237	USB2_REXT	I/O	-	3.3	External reference resistor of USB 2.0 port. A 135±1% resistor is recommended.

VI Pins

Table 2-18 describes video input (VI) pins.

Table 2-18 VI pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
160	VI_ADC_REFCLK0	I/O	CFG	3.3/1.8	Function 0: GPIO6_0 GPIO Function 1: VI_ADC_REFCLK0 Video analog-to-digital converter (VADC) working clock 0 Function 2: VI1_CLK VI1 clock signal
141	VI0_CLK	I/O	CFG	3.3/1.8	Function 0: GPIO5_7

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO Function 1: VI0_CLK VI0 clock signal Function 2: VI_ADC_REFCLK0 VADC working clock 0
149	VI0_DAT0	I/O	CFG	3.3/1.8	Function 0: GPIO1_7 GPIO Function 1: VI0_DAT0 VI0 data input
148	VI0_DAT1	I/O	CFG	3.3/1.8	Function 0: GPIO1_6 GPIO Function 1: VI0_DAT1 VI0 data input
147	VI0_DAT2	I/O	CFG	3.3/1.8	Function 0: GPIO1_5 GPIO Function 1: VI0_DAT2 VI0 data input
146	VI0_DAT3	I/O	CFG	3.3/1.8	Function 0: GPIO1_4 GPIO Function 1: VI0_DAT3 VI0 data input
145	VI0_DAT4	I/O	CFG	3.3/1.8	Function 0: GPIO1_3 GPIO Function 1: VI0_DAT4 VI0 data input
144	VI0_DAT5	I/O	CFG	3.3/1.8	Function 0: GPIO1_2 GPIO Function 1: VI0_DAT5 VI0 data input
143	VI0_DAT6	I/O	CFG	3.3/1.8	Function 0: GPIO1_1

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO Function 1: VI0_DAT6 VI0 data input
142	VI0_DAT7	I/O	CFG	3.3/1.8	Function 0: GPIO1_0 GPIO Function 1: VI0_DAT7 VI0 data input
150	VI1_CLK	I/O	CFG	3.3/1.8	Function 0: GPIO10_6 GPIO Function 1: VI1_CLK VI1 clock signal Function 2: VI0_CLK VI0 clock signal
159	VI1_DAT0	I/O	CFG	3.3/1.8	Function 0: GPIO2_7 GPIO Function 1: VI1_DAT0 VI1 data input
158	VI1_DAT1	I/O	CFG	3.3/1.8	Function 0: GPIO2_6 GPIO Function 1: VI1_DAT1 VI1 data input
157	VI1_DAT2	I/O	CFG	3.3/1.8	Function 0: GPIO2_5 GPIO Function 1: VI1_DAT2 VI1 data input
156	VI1_DAT3	I/O	CFG	3.3/1.8	Function 0: GPIO2_4 GPIO Function 1: VI1_DAT3 VI1 data input
155	VI1_DAT4	I/O	CFG	3.3/1.8	Function 0: GPIO2_3 GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: VI1_DAT4 VI1 data input
154	VI1_DAT5	I/O	CFG	3.3/1.8	Function 0: GPIO2_2 GPIO Function 1: VI1_DAT5 VI1 data input
153	VI1_DAT6	I/O	CFG	3.3/1.8	Function 0: GPIO2_1 GPIO Function 1: VI1_DAT6 VI1 data input
152	VI1_DAT7	I/O	CFG	3.3/1.8	Function 0: GPIO2_0 GPIO Function 1: VI1_DAT7 VI1 data input

I2S Pins

Table 2-19 describes inter-IC sound (I^2S) pins.

Table 2-19 I^2S pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
139	I2S0_BCLK_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_0 GPIO Function 1: I2S0_BCLK_RX RX clock of the I^2S0/PCM0 interface
137	I2S0_SD_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_2 GPIO Function 1: I2S0_SD_RX Data input of the I^2S0/PCM0 interface
138	I2S0_WS_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_1

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO Function 1: I2S0_WS_RX I^2S0 RX audio channel select signal or PCM0 RX frame sync signal
135	I2S1_BCLK_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_3 GPIO Function 1: I2S1_BCLK_RX RX clock of the I2S1/PCM1 interface Function 2: I2S2_MCLK Main clock of the I^2S2 or PCM2 interface. It can act as the working clock of the audio CODEC.
133	I2S1_SD_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_5 GPIO Function 1: I2S1_SD_RX Data input of the I^2S1 or PCM1 interface
134	I2S1_WS_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_4 GPIO Function 1: I2S1_WS_RX I^2S1 RX audio channel select signal or PCM1 RX frame sync signal
131	I2S2_BCLK_TX	I/O	CFG	3.3/1.8	Function 0: GPIO9_6 GPIO Function 1: I2S2_BCLK_TX TX clock of the I^2S2/PCM2 interface
129	I2S2_SD_TX	I/O	CFG	3.3/1.8	Function 0: GPIO5_4 GPIO Function 1: I2S2_SD_TX TX data output of the I^2S2 or PCM2 interface
130	I2S2_WS_TX	I/O	CFG	3.3/1.8	Function 0: GPIO9_7 GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: I2S2_WS_TX I^2S2 TX audio channel select signal or PCM2 TX frame sync signal

SPI Pins

Table 2-20 describes SPI pins.

Table 2-20 SPI pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
161	SPI_CSN0	I/O	CFG	3.3/1.8	Function 0: GPIO5_3 GPIO Function1: SPI_CSN0 SPI CS 0 output
162	SPI_SCLK	I/O	CFG	3.3/1.8	Function 0: TEST_CLK Output of the main test clock Function 1: SPI_SCLK SPI clock signal Function 2: GPIO5_0 GPIO
165	SPI_SDI	I/O	CFG	3.3/1.8	Function 0: GPIO5_2 GPIO Function 1: SPI_SDI SPI data input
163	SPI_SDO	I/O	CFG	3.3/1.8	Function 0: GPIO5_1 GPIO Function 1: SPI_SDO SPI data output

OSC Pins

Table 2-21 describes oscillator (OSC) pins.

Table 2-21 OSC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
170	XIN	CIN	-	3.3	24 MHz crystal input
171	XOUT	COUT	-	3.3	24 MHz crystal drive output

RTC Pins

Table 2-22 describes real-time clock (RTC) pins.

Table 2-22 RTC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
178	RTC_XIN	CIN	-	3.3	RTC crystal input
177	RTC_XOUT	COUT	-	3.3	RTC crystal drive output

SYS Pins

Table 2-23 describes system (SYS) pins.

Table 2-23 SYS pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
116	POR_ENABLE	IPD/O	CFG	DVDDIO_33	Power-on reset (POR) enable 0: The internal POR is disabled. 1: The internal POR is enabled.
117	RSTN	IPU /O	CFG	DVDDIO_33	System POR signal input, active low
119	TEST_MODE	IPD/O	CFG	DVDDIO_33	Mode select 0: function mode 1: test mode
118	WDG_RST	I/O	CFG	DVDDIO_3	Function 0:

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
	N			3	WDG_RSTN Watchdog reset output signal, active low and OD output Function 1: SYS_RSTN_OUT System reset output signal, active low
213	SFC_DEVICE_MODE	I_{PD}/O	CFG	3.3/2.5/1.8	SFC_DEVICE_MODE SPI flash type select (hardware multiplexing, valid during reset) 0: SPI NOR flash 1: SPI NAND flash

JTAG Pins

Table 2-24 describes Joint Test Action Group (JTAG) pins.

Table 2-24 JTAG pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
85	JTAG_EN	I_{PD}/O	CFG	3.3 (5 V tol)	JTAG function enable
87	JTAG_TCK	I_{PD}/O	CFG	3.3 (5 V tol)	JTAG function enable
89	JTAG_TDI	I_{PU} /O	CFG	3.3 (5 V tol)	Function 0: JTAG_TCK JTAG clock input Function 1: GPIO12_1 GPIO
86	JTAG_TDO	I/O	CFG	3.3 (5 V tol)	Function 0: JTAG_TDI JTAG data input Function 1: GPIO12_4 GPIO
88	JTAG_TMS	I_{PU} /O	CFG	3.3 (5 V tol)	Function 0: JTAG_TMS JTAG mode select input or data output for software trace, controlled

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					by using the CPU Function 1: GPIO12_2 GPIO
91	JTAG_TRSTN	I_{PD}/O	CFG	3.3 (5 V tol)	Function 0: JTAG_TRSTN JTAG reset input Function 1: GPIO12_0 GPIO

GPIO Pins

Table 2-25 describes GPIO pins.

Table 2-25 GPIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
249	GPIO0_0	I/O	CFG	3.3 (5 V tol)	GPIO
250	GPIO0_1	I/O	CFG	3.3 (5 V tol)	GPIO
251	GPIO0_2	I/O	CFG	3.3 (5 V tol)	GPIO
252	GPIO0_3	I/O	CFG	3.3 (5 V tol)	GPIO

Power and GND Pins

Table 2-26 describes power and GND pins.

Table 2-26 Power and GND pins

Pin Position	Pin Name	Type	Voltage (V)	Description
203	AVCC_HDMITX	P	1.2	HDMI TX core analog power
234	AVCC_USB	P	1.2	USB core analog power
179	AVDD_BAT	P	3.3	RTC batter power pin
40	AVDD_DDRPLL_0	P	3.3	3.3 V DDR3 PLL

Pin Position	Pin Name	Type	Voltage (V)	Description
				analog power
68	AVDD_DDRPLL_1	P	3.3	3.3 V DDR3 PLL analog power
173	AVDD_EFUSE	P	2.5	2.5 V eFUSE analog power
174	AVDD_PLL	P	1.2	PLL core analog power
98	AVDD_VP_SATA0	P	1.2	SATA core analog power
107	AVDD_VP_SATA1	P	1.2	SATA core analog power
102	AVDD_VPTX_SATA0	P	1.2	SATA core analog power
111	AVDD_VPTX_SATA1	P	1.2	SATA core analog power
204	AVDD33_HDMITX	P	3.3	3.3 V HDMI TX analog power
176	AVDD33_PLL	P	3.3	3.3 V PLL analog power
180	AVDD33_RTC	P	3.3	RTC analog power
239	AVDD33_USB	P	3.3	3.3 V USB analog power
188	AVDD33_VDAC	P	3.3	3.3 V VDAC RGB analog power
105	AVDD33_VPH_SATA0	P	3.3	3.3 V SATA analog power
114	AVDD33_VPH_SATA1	P	3.3	3.3 V SATA analog power
5, 6, 14, 20, 27, 37, 53, 62, 71, 77, 94, 120, 136, 151, 166, 191, 220, 227, 243, 253	DVDD_CORE	P	1.2	Core power
90, 115, 169, 192, 242, 256	DVDD33	P	3.3	I/O power
187	DVDD33_VDAC	P	3.3	3.3 V VDAC digital power

Pin Position	Pin Name	Type	Voltage (V)	Description
132	DVDD3318_I2S	P	3.3/1.8	I^2S1/I^2S2 I/O power
125	DVDD3318_SFC	P	3.3/1.8	SFC I/O power
140, 164	DVDD3318_VI	P	3.3/1.8	I^2S0/VI/SPI I/O power
215, 222, 230	DVDDIO_RGMII	P	3.3/2.5	RGMII power
47	VDDIO_DDR_CK	P	1.5	DDR3 clock interface power
10, 17, 24, 31, 41, 50, 59, 67, 74, 80	VDDIO_DDR	P	1.5	DDR3 interface power
175	AVSS_PLL	G	-	PLL analog GND
181	AVSS_RTC	G	-	RTC analog GND
238	AVSS_USB	G	-	USB analog GND
185	AVSS_VDAC	G	-	VDAC analog GND
183	DVSS_VDAC	G	-	VDAC digital GND
13, 21, 28, 34, 44, 56, 83, 101, 110, 172, 209, 221	VSS	P	-	Digital GND

2.3 Default Reset Status of Digital Pins

Table 2-27 describes the default reset status of digital pins.

Table 2-27 Default reset status of digital pins

Position	Pin Name	Default Status	Remarks
212	EPHY_CLK	Input	-
249	GPIO0_0	Input	-
250	GPIO0_1	Input	-
251	GPIO0_2	Input	-

Position	Pin Name	Default Status	Remarks
252	GPIO0_3	Input	-
198	HDMI_CEC	Input	-
195	HDMI_HOTPLUG	Input	-
197	HDMI_SCL	Input	-
196	HDMI_SDA	Input	-
167	I2C_SCL	Input	-
168	I2C_SDA	Input	-
139	I2S0_BCLK_RX	Input	-
137	I2S0_SD_RX	Input	-
138	I2S0_WS_RX	Input	-
135	I2S1_BCLK_RX	Input	-
133	I2S1_SD_RX	Input	-
134	I2S1_WS_RX	Input	-
131	I2S2_BCLK_TX	Input	-
129	I2S2_SD_TX	Input	-
130	I2S2_WS_TX	Input	-
95	IR_IN	Input	Internal pull-up
85	JTAG_EN	Input	Internal pull-down
87	JTAG_TCK	Input	Internal pull-down
89	JTAG_TDI	Input	Internal pull-up
86	JTAG_TDO	Output when JTAG_EN is high, and input when JTAG_EN is low	-

Position	Pin Name	Default Status	Remarks
88	JTAG_TMS	Input	Internal pull-up
91	JTAG_TRSTN	Input	Internal pull-down
211	MDCK	Input	Internal pull-down
210	MDIO	Input	-
116	POR_ENABLE	Input	Internal pull-down
248	PWM_OUT0	Low-level output	-
225	RGMII_COL	Input	Internal pull-down
224	RGMII_CRS	Input	Internal pull-down
226	RGMII_RXCK	Input	-
232	RGMII_RXD0	Input	-
231	RGMII_RXD1	Input	-
229	RGMII_RXD2	Input	-
228	RGMII_RXD3	Input	-
233	RGMII_RXDV	Input	-
223	RGMII_TXCKOUT	Input	-
218	RGMII_TXD0	Input	-
217	RGMII_TXD1	Input	-
216	RGMII_TXD2	Input	-
214	RGMII_TXD3	Input	-
219	RGMII_TXEN	Input	-
213	SFC_DEVICE_MODE	Low-level output	-
117	RSTN	Input	Internal pull-up
96	SATA_LED_N0	Input	-
97	SATA_LED_N1	Input	-

Position	Pin Name	Default Status	Remarks
122	SFC_CLK	Low-level output	-
121	SFC_CS0N	High-level output	-
126	SFC_CS1N	High-level output	-
123	SFC_DIO	Input	-
127	SFC_DOI	Input	-
124	SFC_HOLD_IO3	Input	-
128	SFC_WP_IO2	Input	-
161	SPI_CSN0	Input	-
162	SPI_SCLK	Low-level output	-
165	SPI_SDI	Input	-
163	SPI_SDO	Input	-
119	TEST_MODE	Input	Internal pull-down
1	UART0_CTSN	Input	-
2	UART0_RTSN	High-level output	-
254	UART0_RXD	Input	Internal pull-up
255	UART0_TXD	High-level output	-
3	UART1_RXD	Input	Internal pull-up
4	UART1_TXD	Input	-
92	UART2_RXD	Input	Internal pull-up
93	UART2_TXD	Input	-
244	USB2_OVRCUR0	Input	-
246	USB2_OVRCUR1	Input	-
245	USB2_PWREN0	Input	-

Position	Pin Name	Default Status	Remarks
247	USB2_PWREN1	Input	-
193	VGA_HS	Input	-
194	VGA_VS	Input	-
160	VI_ADC_REFCLK0	Input	-
141	VI0_CLK	Input	-
149	VI0_DAT0	Input	-
148	VI0_DAT1	Input	-
147	VI0_DAT2	Input	-
146	VI0_DAT3	Input	-
145	VI0_DAT4	Input	-
144	VI0_DAT5	Input	-
143	VI0_DAT6	Input	-
142	VI0_DAT7	Input	-
150	VI1_CLK	Input	-
159	VI1_DAT0	Input	-
158	VI1_DAT1	Input	-
157	VI1_DAT2	Input	-
156	VI1_DAT3	Input	-
155	VI1_DAT4	Input	-
154	VI1_DAT5	Input	-
153	VI1_DAT6	Input	-
152	VI1_DAT7	Input	-
118	WDG_RSTN	OD output	-

2.4 Pin Multiplexing Control Registers

2.4.1 Register Summary

Table 2-28 describes pin multiplexing control registers.

Table 2-28 Summary of pin multiplexing control registers (base address: 0x120F_0000)

Offset Address	Register	Description	Page
0x000	muxctrl_reg0	Multiplexing control register for the VI0_CLK pin	2-46
0x004	muxctrl_reg1	Multiplexing control register for the VI0_DAT7 pin	2-46
0x008	muxctrl_reg2	Multiplexing control register for the VI0_DAT6 pin	2-47
0x00C	muxctrl_reg3	Multiplexing control register for the VI0_DAT5 pin	2-47
0x010	muxctrl_reg4	Multiplexing control register for the VI0_DAT4 pin	2-47
0x014	muxctrl_reg5	Multiplexing control register for the VI0_DAT3 pin	2-48
0x018	muxctrl_reg6	Multiplexing control register for the VI0_DAT2 pin	2-48
0x01C	muxctrl_reg7	Multiplexing control register for the VI0_DAT1 pin	2-49
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Offset Address	Register	Description	Page
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Offset Address	Register	Description	Page
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0x128	muxctrl_reg74	Multiplexing control register for the RGMII_TXD2 pin	2-81
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Offset Address	Register	Description	Page
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0x158	muxctrl_reg86	Multiplexing control register for the SFC_DIO pin	2-86
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2.4.2 Register Description

muxctrl_reg0

muxctrl_reg0 is a multiplexing control register for the VI0_CLK pin.

Offset Address	Register Name	Total Reset Value
0x000	muxctrl_reg0	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg0	Multiplexing control for the VI0_CLK pin 00: GPIO5_7 01: VI0_CLK 10: VI_ADC_REFCLK0 Other values: Reserved

muxctrl_reg1

muxctrl_reg1 is a multiplexing control register for the VI0_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x004	muxctrl_reg1	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg1	Multiplexing control for the VI0_DAT7 pin 0: GPIO1_0 1: VI0_DAT7

muxctrl_reg2

muxctrl_reg2 is a multiplexing control register for the VI0_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x008	muxctrl_reg2	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg2	Multiplexing control for the VI0_DAT6 pin 0: GPIO1_1 1: VI0_DAT6

muxctrl_reg3

muxctrl_reg3 is a multiplexing control register for the VI0_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x00C	muxctrl_reg3	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg3
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg3	Multiplexing control for the VI0_DAT5 pin 0: GPIO1_2 1: VI0_DAT5

muxctrl_reg4

muxctrl_reg4 is a multiplexing control register for the VI0_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x010	muxctrl_reg4	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg4
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg4	Multiplexing control for the VI0_DAT4 pin 0: GPIO1_3 1: VI0_DAT4

muxctrl_reg5

muxctrl_reg5 is a multiplexing control register for the VI0_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x014	muxctrl_reg5	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg5
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg5	Multiplexing control for the VI0_DAT3 pin 0: GPIO1_4 1: VI0_DAT3

muxctrl_reg6

muxctrl_reg6 is a multiplexing control register for the VI0_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x018	muxctrl_reg6	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg6	Multiplexing control for the VI0_DAT2 pin 0: GPIO1_5 1: VI0_DAT2

muxctrl_reg7

muxctrl_reg7 is a multiplexing control register for the VI0_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x01C	muxctrl_reg7	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg7
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg7	Multiplexing control for the VI0_DAT1 pin 0: GPIO1_6 1: VI0_DAT1

muxctrl_reg8

muxctrl_reg8 is a multiplexing control register for the VI0_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x020	muxctrl_reg8	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg8
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg8	Multiplexing control for the VI0_DAT0 pin 0: GPIO1_7 1: VI0_DAT0

muxctrl_reg9

muxctrl_reg9 is a multiplexing control register for the VI1_CLK pin.

Offset Address	Register Name	Total Reset Value
0x024	muxctrl_reg9	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg9
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg9	Multiplexing control for the VI1_CLK pin 00: GPIO10_6 01: VI1_CLK 10: VI0_CLK Other values: reserved

muxctrl_reg10

muxctrl_reg10 is a multiplexing control register for the VI1_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x028	muxctrl_reg10	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg10
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg10	Multiplexing control for the VI1_DAT7 pin 0: GPIO2_0 1: VI1_DAT7

muxctrl_reg11

muxctrl_reg11 is a multiplexing control register for the VI1_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x02C	muxctrl_reg11	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg11
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg11	Multiplexing control for the VI1_DAT6 pin 0: GPIO2_1 1: VI1_DAT6

muxctrl_reg12

muxctrl_reg12 is a multiplexing control register for the VI1_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x030	muxctrl_reg12	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg12
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg12	Multiplexing control for the VI1_DAT5 pin 0: GPIO2_2 1: VI1_DAT5

muxctrl_reg13

muxctrl_reg13 is a multiplexing control register for the VI1_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x034	muxctrl_reg13	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg13
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg13	Multiplexing control for the VI1_DAT4 pin 0: GPIO2_3 1: VI1_DAT4

muxctrl_reg14

muxctrl_reg14 is a multiplexing control register for the VI1_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x038	muxctrl_reg14	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg14
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg14	Multiplexing control for the VI1_DAT3 pin 0: GPIO2_4 1: VI1_DAT3

muxctrl_reg15

muxctrl_reg15 is a multiplexing control register for the VI1_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x03C	muxctrl_reg15	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg15
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg15	Multiplexing control for the VI1_DAT2 pin 0: GPIO2_5 1: VI1_DAT2

muxctrl_reg16

muxctrl_reg16 is a multiplexing control register for the VI1_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x040	muxctrl_reg16	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg16
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg16	Multiplexing control for the VI1_DAT1 pin 0: GPIO2_6 1: VI1_DAT1

muxctrl_reg17

muxctrl_reg17 is a multiplexing control register for the VI1_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x044	muxctrl_reg17	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								muxctrl_reg17
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg17	Multiplexing control for the VI1_DAT0 pin 0: GPIO2_7 1: VI1_DAT0

muxctrl_reg18

muxctrl_reg18 is a multiplexing control register for the VI_ADC_REFCLK0 pin.

Offset Address	Register Name	Total Reset Value
0x048	muxctrl_reg18	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 18	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg18	Multiplexing control for the VI_ADC_REFCLK0 pin 00: GPIO6_0 01: VI_ADC_REFCLK0 10: VI1_CLK Other values: reserved

muxctrl_reg19

muxctrl_reg19 is a multiplexing control register for the VI2_CLK pin.

Offset Address	Register Name	Total Reset Value
0x04C	muxctrl_reg19	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg19	Multiplexing control for the VI2_CLK pin 00: GPIO11_7 01: VI2_CLK 10: VI_ADC_REFCLK1 Other values: reserved

muxctrl_reg20

muxctrl_reg20 is a multiplexing control register for the VI2_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x050	muxctrl_reg20	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg20
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg20	Multiplexing control for the VI2_DAT7 pin 0: GPIO3_0 1: VI2_DAT7

muxctrl_reg21

muxctrl_reg21 is a multiplexing control register for the VI2_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x054	muxctrl_reg21	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg21
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg21	Multiplexing control for the VI2_DAT6 pin 0: GPIO3_1 1: VI2_DAT6

muxctrl_reg22

muxctrl_reg22 is a multiplexing control register for the VI2_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x058	muxctrl_reg22	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg22
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg22	Multiplexing control for the VI2_DAT5 pin 0: GPIO3_2 1: VI2_DAT5

muxctrl_reg23

muxctrl_reg23 is a multiplexing control register for the VI2_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x05C	muxctrl_reg23	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg23
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg23	Multiplexing control for the VI2_DAT4 pin 0: GPIO3_3 1: VI2_DAT4

muxctrl_reg24

muxctrl_reg24 is a multiplexing control register for the VI2_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x060	muxctrl_reg24	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg24
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg24	Multiplexing control for the VI2_DAT3 pin 0: GPIO3_4 1: VI2_DAT3

muxctrl_reg25

muxctrl_reg25 is a multiplexing control register for the VI2_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x064	muxctrl_reg25	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg25
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg25	Multiplexing control for the VI2_DAT2 pin 0: GPIO3_5 1: VI2_DAT2

muxctrl_reg26

muxctrl_reg26 is a multiplexing control register for the VI2_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x068	muxctrl_reg26	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg26
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg26	Multiplexing control for the VI2_DAT1 pin 0: GPIO3_6 1: VI2_DAT1

muxctrl_reg27

muxctrl_reg27 is a multiplexing control register for the VI2_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x06C	muxctrl_reg27	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg27
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg27	Multiplexing control for the VI2_DAT0 pin 0: GPIO3_7 1: VI2_DAT0

muxctrl_reg28

muxctrl_reg28 is a multiplexing control register for the VI3_CLK pin.

Offset Address	Register Name	Total Reset Value
0x070	muxctrl_reg28	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg28	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg28	Multiplexing control for the VI3_CLK pin 00: GPIO10_5 01: VI3_CLK 10: VI2_CLK Other values: reserved

muxctrl_reg29

muxctrl_reg29 is a multiplexing control register for the VI3_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x074	muxctrl_reg29	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg29	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg29	Multiplexing control for the VI3_DAT7 pin 0: GPIO4_0 1: VI3_DAT7

muxctrl_reg30

muxctrl_reg30 is a multiplexing control register for the VI3_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x078	muxctrl_reg30	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg 30
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg30	Multiplexing control for the VI3_DAT6 pin 0: GPIO4_1 1: VI3_DAT6

muxctrl_reg31

muxctrl_reg31 is a multiplexing control register for the VI3_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x07C	muxctrl_reg31	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg 31
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg31	Multiplexing control for the VI3_DAT5 pin 0: GPIO4_2 1: VI3_DAT5

muxctrl_reg32

muxctrl_reg32 is a multiplexing control register for the VI3_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x080	muxctrl_reg32	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg32	Multiplexing control for the VI3_DAT4 pin 0: GPIO4_3 1: VI3_DAT4

muxctrl_reg33

muxctrl_reg33 is a multiplexing control register for the VI3_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x084	muxctrl_reg33	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg33
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg33	Multiplexing control for the VI3_DAT3 pin 0: GPIO4_4 1: VI3_DAT3

muxctrl_reg34

muxctrl_reg34 is a multiplexing control register for the VI3_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x088	muxctrl_reg34	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg34
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg34	Multiplexing control for the VI3_DAT2 pin 0: GPIO4_5 1: VI3_DAT2

muxctrl_reg35

muxctrl_reg35 is a multiplexing control register for the VI3_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x08C	muxctrl_reg35	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg35
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg35	Multiplexing control for the VI3_DAT1 pin 0: GPIO4_6 1: VI3_DAT1

muxctrl_reg36

muxctrl_reg36 is a multiplexing control register for the VI3_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x090	muxctrl_reg36	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg36	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg36	Multiplexing control for the VI3_DAT0 pin 0: GPIO4_7 1: VI3_DAT0

muxctrl_reg37

muxctrl_reg37 is a multiplexing control register for the VI_ADC_REFCLK1 pin.

Offset Address	Register Name	Total Reset Value
0x094	muxctrl_reg37	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg37	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg37	Multiplexing control for the VI_ADC_REFCLK1 pin 00: GPIO6_1 01: VI_ADC_REFCLK1 10: VI3_CLK Other values: reserved

muxctrl_reg38

muxctrl_reg38 is a multiplexing control register for the VGA_HS pin.

Offset Address	Register Name	Total Reset Value
0x098	muxctrl_reg38	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg38
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg38	Multiplexing control for the VGA_HS pin 0: GPIO11_6 1: VGA_HS

muxctrl_reg39

muxctrl_reg39 is a multiplexing control register for the VGA_VS pin.

Offset Address	Register Name	Total Reset Value
0x09C	muxctrl_reg39	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg39
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg39	Multiplexing control for the VGA_VS pin 0: GPIO11_3 1: VGA_VS

muxctrl_reg40

muxctrl_reg40 is a multiplexing control register for the I2S0_BCLK_RX pin.

Offset Address	Register Name	Total Reset Value
0x0A0	muxctrl_reg40	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg40
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg40	Multiplexing control for the I2S0_BCLK_RX pin 0: GPIO9_0 1: I2S0_BCLK_RX

muxctrl_reg41

muxctrl_reg41 is a multiplexing control register for the I2S0_WS_RX pin.

Offset Address	Register Name	Total Reset Value
0x0A4	muxctrl_reg41	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg41
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg41	Multiplexing control for the I2S0_WS_RX pin 0: GPIO9_1 1: I2S0_WS_RX

muxctrl_reg42

muxctrl_reg42 is a multiplexing control register for the I2S0_SD_RX pin.

Offset Address	Register Name	Total Reset Value
0x0A8	muxctrl_reg42	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg42
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg42	Multiplexing control for the I2S0_SD_RX pin 0: GPIO9_2 1: I2S0_SD_RX

muxctrl_reg43

muxctrl_reg43 is a multiplexing control register for the I2S1_BCLK_RX pin.

Offset Address	Register Name	Total Reset Value
0x0AC	muxctrl_reg43	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg43
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg43	Multiplexing control for the I2S1_BCLK_RX pin 00: GPIO9_3 01: I2S1_BCLK_RX 10: I2S2_MCLK Other values: reserved

muxctrl_reg44

muxctrl_reg44 is a multiplexing control register for the I2S1_WS_RX pin.

Offset Address	Register Name	Total Reset Value
0x0B0	muxctrl_reg44	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg44
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg44	Multiplexing control for the I2S1_WS_RX pin 0: GPIO9_4 1: I2S1_WS_RX

muxctrl_reg45

muxctrl_reg45 is a multiplexing control register for the I2S1_SD_RX pin.

Offset Address	Register Name	Total Reset Value
0x0B4	muxctrl_reg45	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg45
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg45	Multiplexing control for the I2S1_SD_RX pin 0: GPIO9_5 1: I2S1_SD_RX

muxctrl_reg46

muxctrl_reg46 is a multiplexing control register for the I2S2_BCLK_TX pin.

Offset Address	Register Name	Total Reset Value
0x0B8	muxctrl_reg46	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg46
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg46	Multiplexing control for the I2S2_BCLK_TX pin 0: GPIO9_6 1: I2S2_BCLK_TX

muxctrl_reg47

muxctrl_reg47 is a multiplexing control register for the I2S2_WS_TX pin.

Offset Address	Register Name	Total Reset Value
0x0BC	muxctrl_reg47	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg47
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg47	Multiplexing control for the I2S2_WS_TX pin 0: GPIO9_7 1: I2S2_WS_TX

muxctrl_reg48

muxctrl_reg48 is a multiplexing control register for the I2S2_SD_TX pin.

Offset Address	Register Name	Total Reset Value
0x0C0	muxctrl_reg48	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg48	Multiplexing control for the I2S2_SD_TX pin 0: GPIO5_4 1: I2S2_SD_TX

muxctrl_reg49

muxctrl_reg49 is a multiplexing control register for the SPI_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x0C4	muxctrl_reg49	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg49
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg49	Multiplexing control for the SPI_SCLK pin 00: TEST_CLK 01: SPI_SCLK 10: GPIO5_0 Other values: reserved

muxctrl_reg50

muxctrl_reg50 is a multiplexing control register for the SPI_SDO pin.

Offset Address	Register Name	Total Reset Value
0x0C8	muxctrl_reg50	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg50
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg50	Multiplexing control for the SPI_SDO pin 0: GPIO5_1 1: SPI_SDO

muxctrl_reg51

muxctrl_reg51 is a multiplexing control register for the SPI_SDI pin.

Offset Address	Register Name	Total Reset Value
0x0CC	muxctrl_reg51	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg51
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg51	Multiplexing control for the SPI_SDI pin 0: GPIO5_2 1: SPI_SDI

muxctrl_reg52

muxctrl_reg52 is a multiplexing control register for the SPI_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x0D0	muxctrl_reg52	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg52
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg52	Multiplexing control for the SPI_CSN0 pin 0: GPIO5_3 1: SPI_CSN0

muxctrl_reg54

muxctrl_reg54 is a multiplexing control register for the PWM_OUT0 pin.

Offset Address	Register Name	Total Reset Value
0x0D8	muxctrl_reg54	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg54
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg54	Multiplexing control for the PWM_OUT0 pin 0: PWM_OUT0 1: GPIO5_5

muxctrl_reg56

muxctrl_reg56 is a multiplexing control register for the I2C_SDA pin.

Offset Address	Register Name	Total Reset Value
0x0E0	muxctrl_reg56	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg56
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg56	Multiplexing control for the I2C_SDA pin 0: GPIO12_6 1: I2C_SDA

muxctrl_reg57

muxctrl_reg57 is a multiplexing control register for the I2C_SCL pin.

Offset Address	Register Name	Total Reset Value
0x0E4	muxctrl_reg57	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg57
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg57	Multiplexing control for the I2C_SCL pin 0: GPIO12_7 1: I2C_SCL

muxctrl_reg58

muxctrl_reg58 is a multiplexing control register for the UART0_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0E8	muxctrl_reg58	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg58
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg58	Multiplexing control for the UART0_RXD pin 0: UART0_RXD 1: GPIO10_7

muxctrl_reg59

muxctrl_reg59 is a multiplexing control register for the UART0_TXD pin.

Offset Address	Register Name	Total Reset Value
0x0EC	muxctrl_reg59	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg59
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg59	Multiplexing control for the UART0_TXD pin 0: UART0_TXD 1: GPIO12_5

muxctrl_reg60

muxctrl_reg60 is a multiplexing control register for the UART0_CTSN pin.

Offset Address	Register Name	Total Reset Value
0x0F0	muxctrl_reg60	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg60
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg60	Multiplexing control for the UART0_CTSN pin 0: UART0_CTSN 1: GPIO6_2

muxctrl_reg61

muxctrl_reg61 is a multiplexing control register for the UART0_RTSN pin.

Offset Address	Register Name	Total Reset Value
0x0F4	muxctrl_reg61	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg61
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg61	Multiplexing control for the UART0_RTSN pin 0: UART0_RTSN 1: GPIO6_3

muxctrl_reg62

muxctrl_reg62 is a multiplexing control register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0F8	muxctrl_reg62	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg62
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg62	Multiplexing control for the UART1_RXD pin 0: GPIO6_5 1: UART1_RXD

muxctrl_reg63

muxctrl_reg63 is a multiplexing control register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x0FC	muxctrl_reg63	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg63
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg63	Multiplexing control for the UART1_TXD pin 0: GPIO6_7 1: UART1_TXD

muxctrl_reg64

muxctrl_reg64 is a multiplexing control register for the UART2_RXD pin.

Offset Address	Register Name	Total Reset Value
0x100	muxctrl_reg64	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg64
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg64	Multiplexing control for the UART2_RXD pin 0: GPIO11_4 1: UART2_RXD

muxctrl_reg65

muxctrl_reg65 is a multiplexing control register for the UART2_TXD pin.

Offset Address	Register Name	Total Reset Value
0x104	muxctrl_reg65	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg65
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg65	Multiplexing control for the UART2_TXD pin 0: GPIO11_5 1: UART2_TXD

muxctrl_reg66

muxctrl_reg66 is a multiplexing control register for the RGMII_RXDV pin.

Offset Address	Register Name	Total Reset Value
0x108	muxctrl_reg66	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg66
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg66	Multiplexing control for the RGMII_RXDV pin 0: GPIO7_0 1: RGMII_RXDV

muxctrl_reg67

muxctrl_reg67 is a multiplexing control register for the RGMII_RXD3 pin.

Offset Address	Register Name	Total Reset Value
0x10C	muxctrl_reg67	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg67
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg67	Multiplexing control for the RGMII_RXD3 pin 0: GPIO7_1 1: RGMII_RXD3

muxctrl_reg68

muxctrl_reg68 is a multiplexing control register for the RGMII_RXD2 pin.

Offset Address	Register Name	Total Reset Value
0x110	muxctrl_reg68	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg68
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg68	Multiplexing control for the RGMII_RXD2 pin 0: GPIO7_2 1: RGMII_RXD2

muxctrl_reg69

muxctrl_reg69 is a multiplexing control register for the RGMII_RXD1 pin.

Offset Address	Register Name	Total Reset Value
0x114	muxctrl_reg69	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg69
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg69	Multiplexing control for the RGMII_RXD1 pin 0: GPIO7_3 1: RGMII_RXD1

muxctrl_reg70

muxctrl_reg70 is a multiplexing control register for the RGMII_RXD0 pin.

Offset Address	Register Name	Total Reset Value
0x118	muxctrl_reg70	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg70
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg70	Multiplexing control for the RGMII_RXD0 pin 0: GPIO7_4 1: RGMII_RXD0

muxctrl_reg71

muxctrl_reg71 is a multiplexing control register for the RGMII_RXCK pin.

Offset Address	Register Name	Total Reset Value
0x11C	muxctrl_reg71	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg71
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg71	Multiplexing control for the RGMII_RXCK pin 0: GPIO7_5 1: RGMII_RXCK

muxctrl_reg72

muxctrl_reg72 is a multiplexing control register for the RGMII_TXEN pin.

Offset Address	Register Name	Total Reset Value
0x120	muxctrl_reg72	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg72
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg72	Multiplexing control for the RGMII_TXEN pin 0: GPIO7_6 1: RGMII_TXEN

muxctrl_reg73

muxctrl_reg73 is a multiplexing control register for the RGMII_TXD3 pin.

Offset Address	Register Name	Total Reset Value
0x124	muxctrl_reg73	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg73
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg73	Multiplexing control for the RGMII_TXD3 pin 0: GPIO7_7 1: RGMII_TXD3

muxctrl_reg74

muxctrl_reg74 is a multiplexing control register for the RGMII_TXD2 pin.

Offset Address	Register Name	Total Reset Value
0x128	muxctrl_reg74	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg74
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg74	Multiplexing control for the RGMII_TXD2 pin 0: GPIO8_0 1: RGMII_TXD2

muxctrl_reg75

muxctrl_reg75 is a multiplexing control register for the RGMII_TXD1 pin.

Offset Address	Register Name	Total Reset Value
0x12C	muxctrl_reg75	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg75
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg75	Multiplexing control for the RGMII_TXD1 pin 0: GPIO8_1 1: RGMII_TXD1

muxctrl_reg76

muxctrl_reg76 is a multiplexing control register for the RGMII_TXD0 pin.

Offset Address	Register Name	Total Reset Value
0x130	muxctrl_reg76	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 76	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg76	Multiplexing control for the RGMII_TXD0 pin 0: GPIO8_2 1: RGMII_TXD0

muxctrl_reg77

muxctrl_reg77 is a multiplexing control register for the RGMII_TXCKOUT pin.

Offset Address	Register Name	Total Reset Value
0x134	muxctrl_reg77	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 77	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg77	Multiplexing control for the RGMII_TXCKOUT pin 00: GPIO8_3 01: RGMII_TXCKOUT 10: MII_TXCK 11: RMII_CLK

muxctrl_reg78

muxctrl_reg78 is a multiplexing control register for the RGMII_CRS pin.

Offset Address	Register Name	Total Reset Value
0x138	muxctrl_reg78	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg78
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg78	Multiplexing control for the RGMII_CRS pin 0: GPIO8_4 1: RGMII_CRS

muxctrl_reg79

muxctrl_reg79 is a multiplexing control register for the RGMII_COL pin.

Offset Address	Register Name	Total Reset Value
0x13C	muxctrl_reg79	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg79
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg79	Multiplexing control for the RGMII_COL pin 0: GPIO8_5 1: RGMII_COL

muxctrl_reg81

muxctrl_reg81 is a multiplexing control register for the EPHY_CLK pin.

Offset Address	Register Name	Total Reset Value
0x144	muxctrl_reg81	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg81	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg81	Multiplexing control for the EPHY_CLK pin 0: GPIO6_6 1: EPHY_CLK

muxctrl_reg83

muxctrl_reg83 is a multiplexing control register for the MDCK pin.

Offset Address	Register Name	Total Reset Value
0x14C	muxctrl_reg83	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg83	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg83	Multiplexing control for the MDCK pin 00: GPIO10_0 01: MDCK 10: BOOTROM_SEL Other values: reserved

muxctrl_reg84

muxctrl_reg84 is a multiplexing control register for the MDIO pin.

Offset Address	Register Name	Total Reset Value
0x150	muxctrl_reg84	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg84
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg84	Multiplexing control for the MDIO pin 0: GPIO10_1 1: MDIO

muxctrl_reg85

muxctrl_reg85 is a multiplexing control register for the IR_IN pin.

Offset Address	Register Name	Total Reset Value
0x154	muxctrl_reg85	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg85
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg85	Multiplexing control for the IR_IN pin 0: GPIO10_2 1: IR_IN

muxctrl_reg86

muxctrl_reg86 is a multiplexing control register for the SFC_DIO pin.

Offset Address	Register Name	Total Reset Value
0x158	muxctrl_reg86	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg86
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg86	Multiplexing control for the SFC_DIO pin 0: SFC_DIO 1: GPIO11_0

muxctrl_reg87

muxctrl_reg87 is a multiplexing control register for the SFC_WP_IO2 pin.

Offset Address	Register Name	Total Reset Value
0x15C	muxctrl_reg87	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg87
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg87	Multiplexing control for the SFC_WP_IO2 pin 0: SFC_WP_IO2 1: GPIO11_1

muxctrl_reg88

muxctrl_reg88 is a multiplexing control register for the SFC_DOI pin.

Offset Address	Register Name	Total Reset Value
0x160	muxctrl_reg88	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg88
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg88	Multiplexing control for the SFC_DOI pin 0: SFC_DOI 1: GPIO11_2

muxctrl_reg89

muxctrl_reg89 is a multiplexing control register for the USB2_OVRCUR0 pin.

Offset Address	Register Name	Total Reset Value
0x164	muxctrl_reg89	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg89
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg89	Multiplexing control for the USB2_OVRCUR0 pin 0: GPIO13_0 1: USB2_OVRCUR0

muxctrl_reg90

muxctrl_reg90 is a multiplexing control register for the USB2_PWREN0 pin.

Offset Address	Register Name	Total Reset Value
0x168	muxctrl_reg90	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg90
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg90	Multiplexing control for the USB2_PWREN0 pin 0: GPIO13_1 1: USB2_PWREN0

muxctrl_reg91

muxctrl_reg91 is a multiplexing control register for the USB2_OVRCUR1 pin.

Offset Address	Register Name	Total Reset Value
0x16C	muxctrl_reg91	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg91
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg91	Multiplexing control for the USB2_OVRCUR1 pin 0: GPIO13_2 1: USB2_OVRCUR1

muxctrl_reg92

muxctrl_reg92 is a multiplexing control register for the USB2_PWREN1 pin.

Offset Address	Register Name	Total Reset Value
0x170	muxctrl_reg92	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg92
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg92	Multiplexing control for the USB2_PWREN1 pin 0: GPIO13_3 1: USB2_PWREN1

muxctrl_reg93

muxctrl_reg93 is a multiplexing control register for the HDMI_HOTPLUG pin.

Offset Address	Register Name	Total Reset Value
0x174	muxctrl_reg93	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg93
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg93	Multiplexing control for the HDMI_HOTPLUG pin 0: GPIO13_4 1: HDMI_HOTPLUG

muxctrl_reg94

muxctrl_reg94 is a multiplexing control register for the HDMI_CEC pin.

Offset Address	Register Name	Total Reset Value
0x178	muxctrl_reg94	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg94
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg94	Multiplexing control for the HDMI_CEC pin 0: GPIO13_5 1: HDMI_CEC

muxctrl_reg95

muxctrl_reg95 is a multiplexing control register for the HDMI_SDA pin.

Offset Address	Register Name	Total Reset Value
0x17C	muxctrl_reg95	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg95
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg95	Multiplexing control for the HDMI_SDA pin 0: GPIO13_6 1: HDMI_SDA

muxctrl_reg96

muxctrl_reg96 is a multiplexing control register for the HDMI_SCL pin.

Offset Address	Register Name	Total Reset Value
0x180	muxctrl_reg96	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg96
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg96	Multiplexing control for the HDMI_SCL pin 0: GPIO13_7 1: HDMI_SCL

muxctrl_reg97

muxctrl_reg97 is a multiplexing control register for the SATA_LED_N0 pin.

Offset Address	Register Name	Total Reset Value
0x184	muxctrl_reg97	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg97
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg97	Multiplexing control for the SATA_LED_N0 pin 0: GPIO10_3 1: SATA_LED_N0

muxctrl_reg98

muxctrl_reg98 is a multiplexing control register for the SATA_LED_N1 pin.

Offset Address	Register Name	Total Reset Value
0x188	muxctrl_reg98	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg98
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg98	Multiplexing control for the SATA_LED_N1 pin 0: GPIO10_4 1: SATA_LED_N1

2.5 Pin Drive Capability Registers

2.5.1 Register Summary

Table 2-29 describes pin drive capability registers.

Table 2-29 Summary of pad_ctrl registers (base address: 0x120F_0800)

Offset Address	Register	Description	Page
0x0000	PADCTRL_REG0	Drive capability register for the VI0_CLK pin	2-99
0x0004	PADCTRL_REG1	Drive capability register for the VI0_DAT7 pin	2-100
0x0008	PADCTRL_REG2	Drive capability register for the VI0_DAT6 pin	2-101
0x000C	PADCTRL_REG3	Drive capability register for the VI0_DAT5 pin	2-101
0x0010	PADCTRL_REG4	Drive capability register for the VI0_DAT4 pin	2-102
0x0014	PADCTRL_REG5	Drive capability register for the VI0_DAT3 pin	2-102
0x0018	PADCTRL_REG6	Drive capability register for the VI0_DAT2 pin	2-103
0x001C	PADCTRL_REG7	Drive capability register for the VI0_DAT1 pin	2-104

Offset Address	Register	Description	Page
0x0020	PADCTRL_REG8	Drive capability register for the VI0_DAT0 pin	2-104
0x0024	PADCTRL_REG9	Drive capability register for the VI1_CLK pin	2-105
0x0028	PADCTRL_REG10	Drive capability register for the VI1_DAT7 pin	2-106
0x002C	PADCTRL_REG11	Drive capability register for the VI1_DAT6 pin	2-106
0x0030	PADCTRL_REG12	Drive capability register for the VI1_DAT5 pin	2-107
0x0034	PADCTRL_REG13	Drive capability register for the VI1_DAT4 pin	2-108
0x0038	PADCTRL_REG14	Drive capability register for the VI1_DAT3 pin	2-108
0x003C	PADCTRL_REG15	Drive capability register for the VI1_DAT2 pin	2-109
0x0040	PADCTRL_REG16	Drive capability register for the VI1_DAT1 pin	2-110
0x0044	PADCTRL_REG17	Drive capability register for the VI1_DAT0 pin	2-110
0x0048	PADCTRL_REG18	Drive capability register for the VI_ADC_REFCLK0 pin	2-111
0x004C	PADCTRL_REG19	Drive capability register for the VI2_CLK pin	2-112
0x0050	PADCTRL_REG20	Drive capability register for the VI2_DAT7 pin	2-113
0x0054	PADCTRL_REG21	Drive capability register for the VI2_DAT6 pin	2-113
0x0058	PADCTRL_REG22	Drive capability register for the VI2_DAT5 pin	2-114
0x005C	PADCTRL_REG23	Drive capability register for the VI2_DAT4 pin	2-115
0x0060	PADCTRL_REG24	Drive capability register for the VI2_DAT3 pin	2-115
0x0064	PADCTRL_REG25	Drive capability register for the VI2_DAT2 pin	2-116
0x0068	PADCTRL_REG26	Drive capability register for the VI2_DAT1 pin	2-117
0x006C	PADCTRL_REG2	Drive capability register for the VI2_DAT0	2-117

Offset Address	Register	Description	Page
	7	pin	
0x0070	PADCTRL_REG28	Drive capability register for the VI3_CLK pin	2-118
0x0074	PADCTRL_REG29	Drive capability register for the VI3_DAT7 pin	2-119
0x0078	PADCTRL_REG30	Drive capability register for the VI3_DAT6 pin	2-119
0x007C	PADCTRL_REG31	Drive capability register for the VI3_DAT5 pin	2-120
0x0080	PADCTRL_REG32	Drive capability register for the VI3_DAT4 pin	2-121
0x0084	PADCTRL_REG33	Drive capability register for the VI3_DAT3 pin	2-121
0x0088	PADCTRL_REG34	Drive capability register for the VI3_DAT2 pin	2-122
0x008C	PADCTRL_REG35	Drive capability register for the VI3_DAT1 pin	2-123
0x0090	PADCTRL_REG36	Drive capability register for the VI3_DAT0 pin	2-123
0x0094	PADCTRL_REG37	Drive capability register for the VI_ADC_REFCLK1 pin	2-124
0x0098	PADCTRL_REG38	Drive capability register for the VGA_HS pin	2-125
0x009C	PADCTRL_REG39	Drive capability register for the VGA_VS pin	2-126
0x00A0	PADCTRL_REG40	Drive capability register for the I2S0_BCLK_RX pin	2-126
0x00A4	PADCTRL_REG41	Drive capability register for the I2S0_WS_RX pin	2-127
0x00A8	PADCTRL_REG42	Drive capability register for the I2S0_SD_RX pin	2-128
0x00AC	PADCTRL_REG43	Drive capability register for the I2S1_BCLK_RX pin	2-128
0x00B0	PADCTRL_REG44	Drive capability register for the I2S1_WS_RX pin	2-129
0x00B4	PADCTRL_REG45	Drive capability register for the I2S1_SD_RX pin	2-130
0x00B8	PADCTRL_REG4	Drive capability register for the	2-130

Offset Address	Register	Description	Page
	6	I2S2_BCLK_TX pin	
0x00BC	PADCTRL_REG47	Drive capability register for the I2S2_WS_TX pin	2-131
0x00C0	PADCTRL_REG48	Drive capability register for the I2S2_SD_TX pin	2-132
0x00C4	PADCTRL_REG49	Drive capability register for the SPI_SCLK pin	2-132
0x00C8	PADCTRL_REG50	Drive capability register for the SPI_SDO pin	2-133
0x00CC	PADCTRL_REG51	Drive capability register for the SPI_SDI pin	2-134
0x00D0	PADCTRL_REG52	Drive capability register for the SPI_CSN0 pin	2-134
0x00D8	PADCTRL_REG54	Drive capability register for the PWM_OUT0 pin	2-135
0x00E0	PADCTRL_REG56	Drive capability register for the I2C_SDA pin	2-136
0x00E4	PADCTRL_REG57	Drive capability register for the I2C_SCL pin	2-136
0x00E8	PADCTRL_REG58	Drive capability register for the UART0_RXD pin	2-137
0x00EC	PADCTRL_REG59	Drive capability register for the UART0_TXD pin	2-138
0x00F0	PADCTRL_REG60	Drive capability register for the UART0_CTSN pin	2-138
0x00F4	PADCTRL_REG61	Drive capability register for the UART0_RTSN pin	2-139
0x00F8	PADCTRL_REG62	Drive capability register for the UART1_RXD pin	2-140
0x00FC	PADCTRL_REG63	Drive capability register for the UART1_TXD pin	2-140
0x0100	PADCTRL_REG64	Drive capability register for the UART2_RXD pin	2-141
0x0104	PADCTRL_REG65	Drive capability register for the UART2_TXD pin	2-142
0x0108	PADCTRL_REG66	Drive capability register for the RGMII_RXDV pin	2-142
0x010C	PADCTRL_REG6	Drive capability register for the	2-143

Offset Address	Register	Description	Page
	7	RGMII_RXD3 pin	
0x0110	PADCTRL_REG68	Drive capability register for the RGMII_RXD2 pin	2-144
0x0114	PADCTRL_REG69	Drive capability register for the RGMII_RXD1 pin	2-144
0x0118	PADCTRL_REG70	Drive capability register for the RGMII_RXD0 pin	2-145
0x011C	PADCTRL_REG71	Drive capability register for the RGMII_RXCK pin	2-146
0x0120	PADCTRL_REG72	Drive capability register for the RGMII_TXEN pin	2-146
0x0124	PADCTRL_REG73	Drive capability register for the RGMII_TXD3 pin	2-147
0x0128	PADCTRL_REG74	Drive capability register for the RGMII_TXD2 pin	2-148
0x012C	PADCTRL_REG75	Drive capability register for the RGMII_TXD1 pin	2-149
0x0130	PADCTRL_REG76	Drive capability register for the RGMII_TXD0 pin	2-149
0x0134	PADCTRL_REG77	Drive capability register for the RGMII_TXCKOUT pin	2-150
0x0138	PADCTRL_REG78	Drive capability register for the RGMII_CRS pin	2-151
0x013C	PADCTRL_REG79	Drive capability register for the RGMII_COL pin	2-152
0x0148	PADCTRL_REG82	Drive capability register for the EPHY_CLK pin	2-152
0x0150	PADCTRL_REG84	Drive capability register for the MDCK pin	2-153
0x0154	PADCTRL_REG85	Drive capability register for the MDIO pin	2-154
0x0158	PADCTRL_REG86	Drive capability register for the IR_IN pin	2-154
0x015C	PADCTRL_REG87	Drive capability register for the SFC_CLK pin	2-155
0x0160	PADCTRL_REG88	Drive capability register for the SFC_DIO pin	2-156
0x0164	PADCTRL_REG8	Drive capability register for the SFC_WP_IO2	2-156

Offset Address	Register	Description	Page
	9	pin	
0x0168	PADCTRL_REG90	Drive capability register for the SFC_DOI pin	2-157
0x016C	PADCTRL_REG91	Drive capability register for the SFC_HOLD_IO3 pin	2-157
0x0170	PADCTRL_REG92	Drive capability register for the SFC_CS0N pin	2-158
0x0174	PADCTRL_REG93	Drive capability register for the SFC_CS1N pin	2-159
0x0178	PADCTRL_REG94	Drive capability register for the JTAG_EN pin	2-159
0x017C	PADCTRL_REG95	Drive capability register for the JTAG_TRSTN pin	2-160
0x0180	PADCTRL_REG96	Drive capability register for the JTAG_TCK pin	2-161
0x0184	PADCTRL_REG97	Drive capability register for the JTAG_TMS pin	2-161
0x0188	PADCTRL_REG98	Drive capability register for the JTAG_TDO pin	2-162
0x018C	PADCTRL_REG99	Drive capability register for the JTAG_TDI pin	2-163
0x0190	PADCTRL_REG100	Drive capability register for the POR_ENABLE pin	2-163
0x0194	PADCTRL_REG101	Drive capability register for the RSTN pin	2-164
0x0198	PADCTRL_REG102	Drive capability register for the WDG_RSTN pin	2-165
0x019C	PADCTRL_REG103	Drive capability register for the TEST_MODE pin	2-165
0x01A0	PADCTRL_REG104	Drive capability register for the USB2_OVRCUR0 pin	2-166
0x01A4	PADCTRL_REG105	Drive capability register for the USB2_PWREN0 pin	2-167
0x01A8	PADCTRL_REG106	Drive capability register for the USB2_OVRCUR1 pin	2-167
0x01AC	PADCTRL_REG107	Drive capability register for the USB2_PWREN1 pin	2-168
0x01B0	PADCTRL_REG1	Drive capability register for the	2-169

Offset Address	Register	Description	Page
	08	HDMI_HOTPLUG pin	
0x01B4	PADCTRL_REG109	Drive capability register for the HDMI_CEC pin	2-169
0x01B8	PADCTRL_REG110	Drive capability register for the HDMI_SDA pin	2-170
0x01BC	PADCTRL_REG111	Drive capability register for the HDMI_SCL pin	2-171
0x01C0	PADCTRL_REG112	Drive capability register for the SATA_LED_N0 pin	2-171
0x01C4	PADCTRL_REG113	Drive capability register for the SATA_LED_N1 pin	2-172
0x01C8	PADCTRL_REG114	Drive capability register for the GPIO0_0 pin	2-173
0x01CC	PADCTRL_REG115	Drive capability register for the GPIO0_1 pin	2-173
0x01D0	PADCTRL_REG116	Drive capability register for the GPIO0_2 pin	2-174
0x01D4	PADCTRL_REG117	Drive capability register for the GPIO0_3 pin	2-175

2.5.2 Register Description

PADCTRL_REG0

PADCTRL_REG0 is a drive capability register for the VI0_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0000	PADCTRL_REG0	0x0000_0078

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2 1 0
Name	reserved						ds	sl	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 1	1	0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the VI0_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG1

PADCTRL_REG1 is a drive capability register for the VI0_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0004	PADCTRL_REG1	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG2

PADCTRL_REG2 is a drive capability register for the VI0_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x0008	PADCTRL_REG2	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG3

PADCTRL_REG3 is a drive capability register for the VI0_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x000C	PADCTRL_REG3	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI0_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG4

PADCTRL_REG4 is a drive capability register for the VI0_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x0010	PADCTRL_REG4	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG5

PADCTRL_REG5 is a drive capability register for the VI0_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0014	PADCTRL_REG5	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG6

PADCTRL_REG6 is a drive capability register for the VI0_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x0018	PADCTRL_REG6	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI0_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG7

PADCTRL_REG7 is a drive capability register for the VI0_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x001C	PADCTRL_REG7	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG8

PADCTRL_REG8 is a drive capability register for the VI0_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x0020	PADCTRL_REG8	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG9

PADCTRL_REG9 is a drive capability register for the VI1_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0024	PADCTRL_REG9	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI1_CLK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG10

PADCTRL_REG10 is a drive capability register for the VI1_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0028	PADCTRL_REG10	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG11

PADCTRL_REG11 is a drive capability register for the VI1_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x002C	PADCTRL_REG11	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG12

PADCTRL_REG12 is a drive capability register for the VI1_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x0030	PADCTRL_REG12	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI1_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG13

PADCTRL_REG13 is a drive capability register for the VI1_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x0034	PADCTRL_REG13	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG14

PADCTRL_REG14 is a drive capability register for the VI1_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0038	PADCTRL_REG14	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG15

PADCTRL_REG15 is a drive capability register for the VI1_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x003C	PADCTRL_REG15	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI1_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG16

PADCTRL_REG16 is a drive capability register for the VI1_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x0040	PADCTRL_REG16	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG17

PADCTRL_REG17 is a drive capability register for the VI1_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x0044	PADCTRL_REG17	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG18

PADCTRL_REG18 is a drive capability register for the VI_ADC_REFCLK0 pin.

Offset Address	Register Name	Total Reset Value
0x0048	PADCTRL_REG18	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the VI_ADC_REFCLK0 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the VI_ADC_REFCLK0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG19

PADCTRL_REG19 is a drive capability register for the VI2_CLK pin.

Offset Address	Register Name	Total Reset Value
0x004C	PADCTRL_REG19	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ds				sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the VI2_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA

[3]	RW	sl	Level conversion rate of the VI2_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG20

PADCTRL_REG20 is a drive capability register for the VI2_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0050	PADCTRL_REG20	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG21

PADCTRL_REG21 is a drive capability register for the VI2_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x0054	PADCTRL_REG21	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG22

PADCTRL_REG22 is a drive capability register for the VI2_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x0058	PADCTRL_REG22	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI2_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG23

PADCTRL_REG23 is a drive capability register for the VI2_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x005C	PADCTRL_REG23	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG24

PADCTRL_REG24 is a drive capability register for the VI2_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0060	PADCTRL_REG24	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG25

PADCTRL_REG25 is a drive capability register for the VI2_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x0064	PADCTRL_REG25	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI2_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG26

PADCTRL_REG26 is a drive capability register for the VI2_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x0068	PADCTRL_REG26	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG27

PADCTRL_REG27 is a drive capability register for the VI2_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x006C	PADCTRL_REG27	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG28

PADCTRL_REG28 is a drive capability register for the VI3_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0070	PADCTRL_REG28	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI3_CLK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG29

PADCTRL_REG29 is a drive capability register for the VI3_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0074	PADCTRL_REG29	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG30

PADCTRL_REG30 is a drive capability register for the VI3_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x0078	PADCTRL_REG30	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG31

PADCTRL_REG31 is a drive capability register for the VI3_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x007C	PADCTRL_REG31	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI3_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG32

PADCTRL_REG32 is a drive capability register for the VI3_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x0080	PADCTRL_REG32	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG33

PADCTRL_REG33 is a drive capability register for the VI3_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0084	PADCTRL_REG33	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG34

PADCTRL_REG34 is a drive capability register for the VI3_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x0088	PADCTRL_REG34	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI3_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG35

PADCTRL_REG35 is a drive capability register for the VI3_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x008C	PADCTRL_REG35	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG36

PADCTRL_REG36 is a drive capability register for the VI3_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x0090	PADCTRL_REG36	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG37

PADCTRL_REG37 is a drive capability register for the VI_ADC_REFCLK1 pin.

Offset Address	Register Name	Total Reset Value
0x0094	PADCTRL_REG37	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the VI_ADC_REFCLK1 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the VI_ADC_REFCLK1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG38

PADCTRL_REG38 is a drive capability register for the VGA_HS pin.

Offset Address	Register Name	Total Reset Value
0x0098	PADCTRL_REG38	0x0000_0078

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2 1 0
Name	reserved						ds	sl	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 1	1	0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the VGA_HS pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA

[3]	RW	sl	Level conversion rate of the VGA_HS pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG39

PADCTRL_REG39 is a drive capability register for the VGA_VS pin.

Offset Address	Register Name	Total Reset Value
0x009C	PADCTRL_REG39	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the VGA_VS pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the VGA_VS pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG40

PADCTRL_REG40 is a drive capability register for the I2S0_BCLK_RX pin.

Offset Address	Register Name	Total Reset Value
0x00A0	PADCTRL_REG40	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S0_BCLK_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S0_BCLK_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG41

PADCTRL_REG41 is a drive capability register for the I2S0_WS_RX pin.

Offset Address	Register Name	Total Reset Value
0x00A4	PADCTRL_REG41	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the I2S0_WS_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S0_WS_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG42

PADCTRL_REG42 is a drive capability register for the I2S0_SD_RX pin.

Offset Address	Register Name	Total Reset Value
0x00A8	PADCTRL_REG42	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S0_SD_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S0_SD_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG43

PADCTRL_REG43 is a drive capability register for the I2S1_BCLK_RX pin.

Offset Address	Register Name	Total Reset Value
0x00AC	PADCTRL_REG43	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S1_BCLK_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S1_BCLK_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG44

PADCTRL_REG44 is a drive capability register for the I2S1_WS_RX pin.

Offset Address	Register Name	Total Reset Value
0x00B0	PADCTRL_REG44	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the I2S1_WS_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S1_WS_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG45

PADCTRL_REG45 is a drive capability register for the I2S1_SD_RX pin.

Offset Address	Register Name	Total Reset Value
0x00B4	PADCTRL_REG45	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S1_SD_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S1_SD_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG46

PADCTRL_REG46 is a drive capability register for the I2S2_BCLK_TX pin.

Offset Address	Register Name	Total Reset Value
0x00B8	PADCTRL_REG46	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S2_BCLK_TX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S2_BCLK_TX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG47

PADCTRL_REG47 is a drive capability register for the I2S2_WS_TX pin.

Offset Address	Register Name	Total Reset Value
0x00BC	PADCTRL_REG47	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the I2S2_WS_TX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S2_WS_TX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG48

PADCTRL_REG48 is a drive capability register for the I2S2_SD_TX pin.

Offset Address	Register Name	Total Reset Value
0x00C0	PADCTRL_REG48	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S2_SD_TX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S2_SD_TX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG49

PADCTRL_REG49 is a drive capability register for the SPI_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x00C4	PADCTRL_REG49	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the SPI_SCLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_SCLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG50

PADCTRL_REG50 is a drive capability register for the SPI_SDO pin.

Offset Address	Register Name	Total Reset Value
0x00C8	PADCTRL_REG50	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SPI_SDO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_SDO pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG51

PADCTRL_REG51 is a drive capability register for the SPI_SDI pin.

Offset Address	Register Name	Total Reset Value
0x00CC	PADCTRL_REG51	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SPI_SDI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_SDI pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG52

PADCTRL_REG52 is a drive capability register for the SPI_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x00D0	PADCTRL_REG52	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SPI_CSN0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_CSN0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG54

PADCTRL_REG54 is a drive capability register for the PWM_OUT0 pin.

Offset Address	Register Name	Total Reset Value
0x00D8	PADCTRL_REG54	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the PWM_OUT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the PWM_OUT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG56

PADCTRL_REG56 is a drive capability register for the I2C_SDA pin.

Offset Address	Register Name	Total Reset Value
0x00E0	PADCTRL_REG56	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2C_SDA pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2C_SDA pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG57

PADCTRL_REG57 is a drive capability register for the I2C_SCL pin.

Offset Address	Register Name	Total Reset Value
0x00E4	PADCTRL_REG57	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2C_SCL pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2C_SCL pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG58

PADCTRL_REG58 is a drive capability register for the UART0_RXD pin.

Offset Address	Register Name	Total Reset Value
0x00E8	PADCTRL_REG58	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the UART0_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART0_RXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG59

PADCTRL_REG59 is a drive capability register for the UART0_TXD pin.

Offset Address	Register Name	Total Reset Value
0x00EC	PADCTRL_REG59	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART0_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART0_TXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG60

PADCTRL_REG60 is a drive capability register for the UART0_CTSN pin.

Offset Address	Register Name	Total Reset Value
0x00F0	PADCTRL_REG60	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART0_CTSN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART0_CTSN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG61

PADCTRL_REG61 is a drive capability register for the UART0_RTSN pin.

Offset Address	Register Name	Total Reset Value
0x00F4	PADCTRL_REG61	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the UART0_RTSN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART0_RTSN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG62

PADCTRL_REG62 is a drive capability register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x00F8	PADCTRL_REG62	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART1_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART1_RXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG63

PADCTRL_REG63 is a drive capability register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x00FC	PADCTRL_REG63	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART1_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART1_TXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG64

PADCTRL_REG64 is a drive capability register for the UART2_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0100	PADCTRL_REG64	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the UART2_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART2_RXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG65

PADCTRL_REG65 is a drive capability register for the UART2_TXD pin.

Offset Address	Register Name	Total Reset Value
0x0104	PADCTRL_REG65	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART2_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART2_TXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG66

PADCTRL_REG66 is a drive capability register for the RGMII_RXDV pin.

Offset Address	Register Name	Total Reset Value
0x0108	PADCTRL_REG66	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXDV pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXDV pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG67

PADCTRL_REG67 is a drive capability register for the RGMII_RXD3 pin.

Offset Address	Register Name	Total Reset Value
0x010C	PADCTRL_REG67	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the RGMII_RXD3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXD3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG68

PADCTRL_REG68 is a drive capability register for the RGMII_RXD2 pin.

Offset Address	Register Name	Total Reset Value
0x0110	PADCTRL_REG68	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXD2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXD2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG69

PADCTRL_REG69 is a drive capability register for the RGMII_RXD1 pin.

Offset Address	Register Name	Total Reset Value
0x0114	PADCTRL_REG69	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXD1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXD1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG70

PADCTRL_REG70 is a drive capability register for the RGMII_RXD0 pin.

Offset Address	Register Name	Total Reset Value
0x0118	PADCTRL_REG70	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the RGMII_RXD0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXD0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG71

PADCTRL_REG71 is a drive capability register for the RGMII_RXCK pin.

Offset Address	Register Name	Total Reset Value
0x011C	PADCTRL_REG71	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXCK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXCK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG72

PADCTRL_REG72 is a drive capability register for the RGMII_TXEN pin.

Offset Address	Register Name	Total Reset Value
0x0120	PADCTRL_REG72	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXEN pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXEN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG73

PADCTRL_REG73 is a drive capability register for the RGMII_TXD3 pin.

Offset Address	Register Name	Total Reset Value
0x0124	PADCTRL_REG73	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the RGMII_TXD3 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXD3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG74

PADCTRL_REG74 is a drive capability register for the RGMII_TXD2 pin.

Offset Address	Register Name	Total Reset Value
0x0128	PADCTRL_REG74	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ds				sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXD2 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA

[3]	RW	sl	Level conversion rate of the RGMII_TXD2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG75

PADCTRL_REG75 is a drive capability register for the RGMII_TXD1 pin.

Offset Address	Register Name	Total Reset Value
0x012C	PADCTRL_REG75	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXD1 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXD1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG76

PADCTRL_REG76 is a drive capability register for the RGMII_TXD0 pin.

Offset Address	Register Name	Total Reset Value
0x0130	PADCTRL_REG76	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXD0 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXD0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG77

PADCTRL_REG77 is a drive capability register for the RGMII_TXCKOUT pin.

Offset Address	Register Name	Total Reset Value
0x0134	PADCTRL_REG77	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the RGMII_TXCKOUT pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXCKOUT pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG78

PADCTRL_REG78 is a drive capability register for the RGMII_CRS pin.

Offset Address	Register Name	Total Reset Value
0x0138	PADCTRL_REG78	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_CRS pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_CRS pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG79

PADCTRL_REG79 is a drive capability register for the RGMII_COL pin.

Offset Address	Register Name	Total Reset Value
0x013C	PADCTRL_REG79	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_COL pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_COL pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG82

PADCTRL_REG82 is a drive capability register for the EPHY_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0148	PADCTRL_REG82	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the EPHY_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the EPHY_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG84

PADCTRL_REG84 is a drive capability register for the MDCK pin.

Offset Address	Register Name	Total Reset Value
0x0150	PADCTRL_REG84	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the MDCK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the MDCK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG85

PADCTRL_REG85 is a drive capability register for the MDIO pin.

Offset Address	Register Name	Total Reset Value
0x0154	PADCTRL_REG85	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the MDIO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the MDIO pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG86

PADCTRL_REG86 is a drive capability register for the IR_IN pin.

Offset Address	Register Name	Total Reset Value
0x0158	PADCTRL_REG86	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the IR_IN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the IR_IN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG87

PADCTRL_REG87 is a drive capability register for the SFC_CLK pin.

Offset Address	Register Name	Total Reset Value
0x015C	PADCTRL_REG87	0x0000_0058

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ds				sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the SFC_CLK pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG88

PADCTRL_REG88 is a drive capability register for the SFC_DIO pin.

Offset Address	Register Name	Total Reset Value
0x0160	PADCTRL_REG88	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SFC_DIO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_DIO pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG89

PADCTRL_REG89 is a drive capability register for the SFC_WP_IO2 pin.

Offset Address	Register Name	Total Reset Value
0x0164	PADCTRL_REG89	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SFC_WP_IO2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_WP_IO2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG90

PADCTRL_REG90 is a drive capability register for the SFC_DOI pin.

Offset Address	Register Name	Total Reset Value
0x0168	PADCTRL_REG90	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SFC_DOI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_DOI pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG91

PADCTRL_REG91 is a drive capability register for the SFC_HOLD_IO3 pin.

Offset Address	Register Name	Total Reset Value
0x016C	PADCTRL_REG91	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SFC_HOLD_IO3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_HOLD_IO3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG92

PADCTRL_REG92 is a drive capability register for the SFC_CS0N pin.

Offset Address	Register Name	Total Reset Value
0x0170	PADCTRL_REG92	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SFC_CS0N pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_CS0N pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG93

PADCTRL_REG93 is a drive capability register for the SFC_CS1N pin.

Offset Address	Register Name	Total Reset Value
0x0174	PADCTRL_REG93	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SFC_CS1N pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_CS1N pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG94

PADCTRL_REG94 is a drive capability register for the JTAG_EN pin.

Offset Address	Register Name	Total Reset Value
0x0178	PADCTRL_REG94	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the JTAG_EN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_EN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG95

PADCTRL_REG95 is a drive capability register for the JTAG_TRSTN pin.

Offset Address	Register Name	Total Reset Value
0x017C	PADCTRL_REG95	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the JTAG_TRSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TRSTN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG96

PADCTRL_REG96 is a drive capability register for the JTAG_TCK pin.

Offset Address	Register Name	Total Reset Value
0x0180	PADCTRL_REG96	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the JTAG_TCK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TCK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG97

PADCTRL_REG97 is a drive capability register for the JTAG_TMS pin.

Offset Address	Register Name	Total Reset Value
0x0184	PADCTRL_REG97	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the JTAG_TMS pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TMS pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG98

PADCTRL_REG98 is a drive capability register for the JTAG_TDO pin.

Offset Address	Register Name	Total Reset Value
0x0188	PADCTRL_REG98	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the JTAG_TDO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TDO pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG99

PADCTRL_REG99 is a drive capability register for the JTAG_TDI pin.

Offset Address	Register Name	Total Reset Value
0x018C	PADCTRL_REG99	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the JTAG_TDI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TDI pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG100

PADCTRL_REG100 is a drive capability register for the POR_ENABLE pin.

Offset Address	Register Name	Total Reset Value
0x0190	PADCTRL_REG100	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the POR_ENABLE pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the POR_ENABLE pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG101

PADCTRL_REG101 is a drive capability register for the RSTN pin.

Offset Address	Register Name	Total Reset Value
0x0194	PADCTRL_REG101	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the RSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RSTN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG102

PADCTRL_REG102 is a drive capability register for the WDG_RSTN pin.

Offset Address	Register Name	Total Reset Value
0x0198	PADCTRL_REG102	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the WDG_RSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the WDG_RSTN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG103

PADCTRL_REG103 is a drive capability register for the TEST_MODE pin.

Offset Address	Register Name	Total Reset Value
0x019C	PADCTRL_REG103	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the TEST_MODE pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the TEST_MODE pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG104

PADCTRL_REG104 is a drive capability register for the USB2_OVRCUR0 pin.

Offset Address	Register Name	Total Reset Value
0x01A0	PADCTRL_REG104	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the USB2_OVRCUR0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the USB2_OVRCUR0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG105

PADCTRL_REG105 is a drive capability register for the USB2_PWREN0 pin.

Offset Address	Register Name	Total Reset Value
0x01A4	PADCTRL_REG105	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the USB2_PWREN0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the USB2_PWREN0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG106

PADCTRL_REG106 is a drive capability register for the USB2_OVRCUR1 pin.

Offset Address	Register Name	Total Reset Value
0x01A8	PADCTRL_REG106	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the USB2_OVRCUR1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the USB2_OVRCUR1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG107

PADCTRL_REG107 is a drive capability register for the USB2_PWREN1 pin.

Offset Address	Register Name	Total Reset Value
0x01AC	PADCTRL_REG107	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the USB2_PWREN1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the USB2_PWREN1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG108

PADCTRL_REG108 is a drive capability register for the HDMI_HOTPLUG pin.

Offset Address	Register Name	Total Reset Value
0x01B0	PADCTRL_REG108	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the HDMI_HOTPLUG pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the HDMI_HOTPLUG pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG109

PADCTRL_REG109 is a drive capability register for the HDMI_CEC pin.

Offset Address	Register Name	Total Reset Value
0x01B4	PADCTRL_REG109	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the HDMI_CEC pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the HDMI_CEC pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG110

PADCTRL_REG110 is a drive capability register for the HDMI_SDA pin.

Offset Address	Register Name	Total Reset Value
0x01B8	PADCTRL_REG110	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the HDMI_SDA pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the HDMI_SDA pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG111

PADCTRL_REG111 is a drive capability register for the HDMI_SCL pin.

Offset Address	Register Name	Total Reset Value
0x01BC	PADCTRL_REG111	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the HDMI_SCL pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the HDMI_SCL pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG112

PADCTRL_REG112 is a drive capability register for the SATA_LED_N0 pin.

Offset Address	Register Name	Total Reset Value
0x01C0	PADCTRL_REG112	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SATA_LED_N0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SATA_LED_N0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG113

PADCTRL_REG113 is a drive capability register for the SATA_LED_N1 pin.

Offset Address	Register Name	Total Reset Value
0x01C4	PADCTRL_REG113	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SATA_LED_N1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SATA_LED_N1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG114

PADCTRL_REG114 is a drive capability register for the GPIO0_0 pin.

Offset Address	Register Name	Total Reset Value
0x01C8	PADCTRL_REG114	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the GPIO0_0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG115

PADCTRL_REG115 is a drive capability register for the GPIO0_1 pin.

Offset Address	Register Name	Total Reset Value
0x01CC	PADCTRL_REG115	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the GPIO0_1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG116

PADCTRL_REG116 is a drive capability register for the GPIO0_2 pin.

Offset Address	Register Name	Total Reset Value
0x01D0	PADCTRL_REG116	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the GPIO0_2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG117

PADCTRL_REG117 is a drive capability register for the GPIO0_3 pin.

Offset Address	Register Name	Total Reset Value
0x01D4	PADCTRL_REG117	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the GPIO0_3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

2.6 Software Multiplexed Pins

VI

Table 2-30 lists the software multiplexed pins of VI.

Table 2-30 Software multiplexed pins of VI

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
141	VI0_CLK	muxctrl_reg0	GPIO5_7	VI0_CLK	VI_ADC_REFCLK0
142	VI0_DAT7	muxctrl_reg1	GPIO1_0	VI0_DAT7	-
143	VI0_DAT6	muxctrl_reg2	GPIO1_1	VI0_DAT6	-
144	VI0_DAT5	muxctrl_reg3	GPIO1_2	VI0_DAT5	-
145	VI0_DAT4	muxctrl_reg4	GPIO1_3	VI0_DAT4	-
146	VI0_DAT3	muxctrl_reg5	GPIO1_4	VI0_DAT3	-
147	VI0_DAT2	muxctrl_reg6	GPIO1_5	VI0_DAT2	-
148	VI0_DAT1	muxctrl_reg7	GPIO1_6	VI0_DAT1	-
149	VI0_DAT0	muxctrl_reg8	GPIO1_7	VI0_DAT0	-
150	VI1_CLK	muxctrl_reg9	GPIO10_6	VI1_CLK	VI0_CLK
152	VI1_DAT7	muxctrl_reg10	GPIO2_0	VI1_DAT7	-
153	VI1_DAT6	muxctrl_reg11	GPIO2_1	VI1_DAT6	-
154	VI1_DAT5	muxctrl_reg12	GPIO2_2	VI1_DAT5	-
155	VI1_DAT4	muxctrl_reg13	GPIO2_3	VI1_DAT4	-
156	VI1_DAT3	muxctrl_reg14	GPIO2_4	VI1_DAT3	-
157	VI1_DAT2	muxctrl_reg15	GPIO2_5	VI1_DAT2	-
158	VI1_DAT1	muxctrl_reg16	GPIO2_6	VI1_DAT1	-
159	VI1_DAT0	muxctrl_reg17	GPIO2_7	VI1_DAT0	-
160	VI_ADC_REFCLK0	muxctrl_reg18	GPIO6_0	VI_ADC_REFCLK0	VI1_CLK

Table 2-31 describes the software multiplexed pins of VI.

Table 2-31 Description of the software multiplexed pins of VI

Signal	Direction	Description
GPIO1_0	I/O	GPIO
GPIO1_1	I/O	GPIO
GPIO1_2	I/O	GPIO
GPIO1_3	I/O	GPIO
GPIO1_4	I/O	GPIO
GPIO1_5	I/O	GPIO
GPIO1_6	I/O	GPIO
GPIO1_7	I/O	GPIO
GPIO10_6	I/O	GPIO
GPIO2_0	I/O	GPIO
GPIO2_1	I/O	GPIO
GPIO2_2	I/O	GPIO
GPIO2_3	I/O	GPIO
GPIO2_4	I/O	GPIO
GPIO2_5	I/O	GPIO
GPIO2_6	I/O	GPIO
GPIO2_7	I/O	GPIO
GPIO5_7	I/O	GPIO
GPIO6_0	I/O	GPIO
VI_ADC_REFCLK0	O	VADC working clock 0
VI_ADC_REFCLK1	O	VADC working clock 1
VI0_CLK	I	VI0 clock signal
VI0_DAT0	I	VI0 data input
VI0_DAT1	I	VI0 data input
VI0_DAT2	I	VI0 data input
VI0_DAT3	I	VI0 data input
VI0_DAT4	I	VI0 data input
VI0_DAT5	I	VI0 data input
VI0_DAT6	I	VI0 data input

Signal	Direction	Description
VI0_DAT7	I	VI0 data input
VI1_CLK	I	VI1 clock signal
VI1_DAT0	I	VI1 data input
VI1_DAT1	I	VI1 data input
VI1_DAT2	I	VI1 data input
VI1_DAT3	I	VI1 data input
VI1_DAT4	I	VI1 data input
VI1_DAT5	I	VI1 data input
VI1_DAT6	I	VI1 data input
VI1_DAT7	I	VI1 data input

VGA

Table 2-32 lists the software multiplexed pins of VGA.

Table 2-32 Software multiplexed pins of VGA

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
193	VGA_HS	muxctrl_reg38	GPIO11_6	VGA_HS
194	VGA_VS	muxctrl_reg39	GPIO11_3	VGA_VS

Table 2-33 describes the software multiplexed pins of VGA.

Table 2-33 Description of the software multiplexed pins of VGA

Signal	Direction	Description
GPIO11_3	I/O	GPIO
GPIO11_6	I/O	GPIO
VGA_HS	O	VGA row sync output
VGA_VS	O	VGA field sync output

I2S

Table 2-34 lists the software multiplexed pins of I^2S.

Table 2-34 Software multiplexed pins of I²S

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
139	I2S0_BCLK_RX	muxctrl_reg40	GPIO9_0	I2S0_BCLK_RX	-
138	I2S0_WS_RX	muxctrl_reg41	GPIO9_1	I2S0_WS_RX	-
137	I2S0_SD_RX	muxctrl_reg42	GPIO9_2	I2S0_SD_RX	-
135	I2S1_BCLK_RX	muxctrl_reg43	GPIO9_3	I2S1_BCLK_RX	I2S2_MCLK
134	I2S1_WS_RX	muxctrl_reg44	GPIO9_4	I2S1_WS_RX	-
133	I2S1_SD_RX	muxctrl_reg45	GPIO9_5	I2S1_SD_RX	-
131	I2S2_BCLK_TX	muxctrl_reg46	GPIO9_6	I2S2_BCLK_TX	-
130	I2S2_WS_TX	muxctrl_reg47	GPIO9_7	I2S2_WS_TX	-
129	I2S2_SD_TX	muxctrl_reg48	GPIO5_4	I2S2_SD_TX	-

Table 2-35 describes the software multiplexed pins of I²S.

Table 2-35 Description of the software multiplexed pins of I²S

Signal	Direction	Description
GPIO5_4	I/O	GPIO
GPIO9_0	I/O	GPIO
GPIO9_1	I/O	GPIO
GPIO9_2	I/O	GPIO
GPIO9_3	I/O	GPIO
GPIO9_4	I/O	GPIO
GPIO9_5	I/O	GPIO
GPIO9_6	I/O	GPIO
GPIO9_7	I/O	GPIO
I2S0_BCLK_RX	I/O	I²S0/PCM0 RX clock
I2S0_SD_RX	I	Data input of the I²S0/PCM0 interface
I2S0_WS_RX	I/O	I²S0 RX audio channel select signal or PCM0 RX frame sync signal
I2S1_BCLK_RX	I/O	I²S1/PCM1 RX clock

Signal	Direction	Description
I2S1_SD_RX	I	Data input of the I^2S1/PCM1 interface
I2S1_WS_RX	I/O	I^2S1 RX audio channel select signal or PCM1 RX frame sync signal
I2S2_BCLK_TX	I/O	I^2S2/PCM2 TX clock
I2S2_MCLK	O	Main clock of the I^2S2/PCM2 interface. It can act as the working clock of the audio CODEC.
I2S2_SD_TX	O	Data output of the I^2S2/PCM2 interface
I2S2_WS_TX	I/O	I^2S2 TX audio channel select signal or PCM2 TX frame sync signal

SPI

Table 2-36 lists the software multiplexed pins of SPI.

Table 2-36 Software multiplexed pins of SPI

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
162	SPI_SCLK	muxctrl_reg49	TEST_CLK	SPI_SCLK	GPIO5_0
163	SPI_SDO	muxctrl_reg50	GPIO5_1	SPI_SDO	-
165	SPI_SDI	muxctrl_reg51	GPIO5_2	SPI_SDI	-
161	SPI_CSN0	muxctrl_reg52	GPIO5_3	SPI_CSN0	-

Table 2-37 describes the software multiplexed pins of SPI.

Table 2-37 Description of the software multiplexed pins of SPI

Signal	Direction	Description
GPIO5_0	I/O	GPIO
GPIO5_1	I/O	GPIO
GPIO5_2	I/O	GPIO
GPIO5_3	I/O	GPIO
GPIO8_7	I/O	GPIO
SPI_CSN0	O	SPI CS0 output
SPI_SCLK	I/O	SPI clock signal

Signal	Direction	Description
SPI_SDI	I	SPI data input
SPI_SDO	O	SPI data output
TEST_CLK	O	Output of the main test clock

PWM

Table 2-38 lists the software multiplexed pin of PWM.

Table 2-38 Software multiplexed pin of PWM

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
248	PWM_OUT0	muxctrl_reg54	PWM_OUT0	GPIO5_5

Table 2-39 describes the software multiplexed pins of PWM.

Table 2-39 Description of the software multiplexed pins of PWM

Signal	Direction	Description
GPIO5_5	I/O	GPIO
GPIO5_6	I/O	GPIO
PWM_OUT0	O	PWM output 0

I2C

Table 2-40 lists the software multiplexed pins of I^2C.

Table 2-40 Software multiplexed pins of I^2C

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
168	I2C_SDA	muxctrl_reg56	GPIO12_6	I2C_SDA
167	I2C_SCL	muxctrl_reg57	GPIO12_7	I2C_SCL

Table 2-41 describes the software multiplexed pins of I^2C.

Table 2-41 Description of the software multiplexed pins of I^2C

Signal	Direction	Description
GPIO12_6	I/O	GPIO
GPIO12_7	I/O	GPIO
I2C_SCL	I/O	I^2C bus clock
I2C_SDA	I/O	I^2C bus data/address

UART

Table 2-42 lists the software multiplexed pins of UART.

Table 2-42 Software multiplexed pins of UART

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
254	UART0_RXD	muxctrl_reg58	UART0_RXD	GPIO10_7
255	UART0_TXD	muxctrl_reg59	UART0_TXD	GPIO12_5
1	UART0_CTSN	muxctrl_reg60	UART0_CTSN	GPIO6_2
2	UART0_RTSN	muxctrl_reg61	UART0_RTSN	GPIO6_3
3	UART1_RXD	muxctrl_reg62	GPIO6_5	UART1_RXD
4	UART1_TXD	muxctrl_reg63	GPIO6_7	UART1_TXD
92	UART2_RXD	muxctrl_reg64	GPIO11_4	UART2_RXD
93	UART2_TXD	muxctrl_reg65	GPIO11_5	UART2_TXD

Table 2-43 describes the software multiplexed pins of UART.

Table 2-43 Description of the software multiplexed pins of UART

Signal	Direction	Description
GPIO10_7	I/O	GPIO
GPIO11_4	I/O	GPIO
GPIO11_5	I/O	GPIO
GPIO12_5	I/O	GPIO
GPIO6_2	I/O	GPIO

Signal	Direction	Description
GPIO6_3	I/O	GPIO
GPIO6_5	I/O	GPIO
GPIO6_7	I/O	GPIO
UART0_CTSN	I	UART0 CTS signal, active low
UART0_RTSN	O	UART0 RTS signal, active low
UART0_RXD	I	UART0 RX data
UART0_TXD	O	UART0 TX data
UART1_RXD	I	UART1 RX data
UART1_TXD	O	UART1 TX data
UART2_RXD	I	UART2 RX data
UART2_TXD	O	UART2 TX data

RGMII

Table 2-44 lists the software multiplexed pins of RGMII.

Table 2-44 Software multiplexed pins of RGMII

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2	Multiplexed Signal 3
233	RGMII_RXDV	muxctrl_reg66	GPIO7_0	RGMII_RXDV	-	-
228	RGMII_RXD3	muxctrl_reg67	GPIO7_1	RGMII_RXD3	-	-
229	RGMII_RXD2	muxctrl_reg68	GPIO7_2	RGMII_RXD2	-	-
231	RGMII_RXD1	muxctrl_reg69	GPIO7_3	RGMII_RXD1	-	-
232	RGMII_RXD0	muxctrl_reg70	GPIO7_4	RGMII_RXD0	-	-
226	RGMII_RXCK	muxctrl_reg71	GPIO7_5	RGMII_RXCK	-	-
219	RGMII_TXEN	muxctrl_reg72	GPIO7_6	RGMII_TXEN	-	-
214	RGMII_TXD3	muxctrl_reg73	GPIO7_7	RGMII_TXD3	-	-
216	RGMII_TXD2	muxctrl_reg74	GPIO8_0	RGMII_TXD2	-	-
217	RGMII_TXD1	muxctrl_reg75	GPIO8_1	RGMII_TXD1	-	-

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2	Multiplexed Signal 3
218	RGMII_TXD0	muxctrl_reg76	GPIO8_2	RGMII_TXD0	-	-
223	RGMII_TXCKOUT	muxctrl_reg77	GPIO8_3	RGMII_TXCKOUT	MII_TXCK	RMII_CLK
224	RGMII_CRS	muxctrl_reg78	GPIO8_4	RGMII_CRS	-	-
225	RGMII_COL	muxctrl_reg79	GPIO8_5	RGMII_COL	-	-
212	EPHY_CLK	muxctrl_reg81	GPIO6_6	EPHY_CLK	-	-

Table 2-45 describes the software multiplexed pins of RGMII.

Table 2-45 Description of the software multiplexed pins of RGMII

Signal	Direction	Description
EPHY_CLK	O	Working clock of the Ethernet PHY
GPIO6_4	I/O	GPIO
GPIO6_6	I/O	GPIO
GPIO7_0	I/O	GPIO
GPIO7_1	I/O	GPIO
GPIO7_2	I/O	GPIO
GPIO7_3	I/O	GPIO
GPIO7_4	I/O	GPIO
GPIO7_5	I/O	GPIO
GPIO7_6	I/O	GPIO
GPIO7_7	I/O	GPIO
GPIO8_0	I/O	GPIO
GPIO8_1	I/O	GPIO
GPIO8_2	I/O	GPIO
GPIO8_3	I/O	GPIO
GPIO8_4	I/O	GPIO
GPIO8_5	I/O	GPIO
GPIO8_6	I/O	GPIO

Signal	Direction	Description
MII_TXCK	I	TX clock in MII mode
RGMII_COL	I	Conflict detection signal in MII mode
RGMII_CRS	I	Carrier sense signal in MII mode
RGMII_RXCK	I	RX clock in RGMII or MII mode
RGMII_RXD0	I	RX data 0 in RGMII, MII, or RMII mode
RGMII_RXD1	I	RX data 1 in RGMII, MII, or RMII mode
RGMII_RXD2	I	RX data 2 in RGMII or MII mode
RGMII_RXD3	I	RX data 3 in RGMII or MII mode
RGMII_RXDV	I	RX data validity signal in RGMII or MII mode RX data validity or carrier detection signal in RMII mode
RGMII_TXCKOUT	O	TX clock (active on both edges) in RGMII gigabit mode
RGMII_TXD0	O	TX data 0 in RGMII, MII, or RMII mode
RGMII_TXD1	O	TX data 1 in RGMII, MII, or RMII mode
RGMII_TXD2	O	TX data 2 in RGMII or MII mode
RGMII_TXD3	O	TX data 3 in RGMII or MII mode
RGMII_TXEN	O	TX data validity signal in RGMII, MII, or RMII mode
RMII_CLK	I/O	Reference clock in RMII mode

MDIO

Table 2-46 lists the software multiplexed pins of MDIO.

Table 2-46 Software multiplexed pins of MDIO

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
211	MDCK	muxctrl_reg83	GPIO10_0	MDCK	BOOTROM_SEL
210	MDIO	muxctrl_reg84	GPIO10_1	MDIO	-

Table 2-47 describes the software multiplexed pins of MDIO.

Table 2-47 Description of the software multiplexed pins of MDIO

Signal	Direction	Description
BOOTROM_SEL	I	BOOTROM boot 0: boot from the SPI flash 1: boot from the BOOTROM
GPIO10_0	I/O	GPIO
GPIO10_1	I/O	GPIO
MDCK	O	Clock output of the MDIO0 interface
MDIO	I/O	I/O signal of the MDIO0 interface

IR

Table 2-48 lists the software multiplexed pin of IR.

Table 2-48 Software multiplexed pin of IR

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
95	IR_IN	muxctrl_reg85	GPIO10_2	IR_IN

Table 2-49 describes the software multiplexed pins of IR.

Table 2-49 Description of the software multiplexed pins of IR

Signal	Direction	Description
GPIO10_2	I/O	GPIO
IR_IN	I	IR input

SFC

Table 2-50 lists the software multiplexed pins of SFC

Table 2-50 Software multiplexed pins of SFC

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
123	SFC_DIO	muxctrl_reg86	SFC_DIO	GPIO11_0
128	SFC_WP_IO2	muxctrl_reg87	SFC_WP_IO2	GPIO11_1

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
127	SFC_DOI	muxctrl_reg88	SFC_DOI	GPIO11_2

Table 2-51 describes the software multiplexed pins of SFC.

Table 2-51 Description of the software multiplexed pins of SFC

Signal	Direction	Description
GPIO11_0	I/O	GPIO
GPIO11_1	I/O	GPIO
GPIO11_2	I/O	GPIO
SFC_DIO	I/O	Data output signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode
SFC_DOI	I/O	Data input signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode
SFC_WP_IO2	I/O	Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal in quad-SPI mode

USB2

Table 2-52 lists the software multiplexed pins of USB 2.0.

Table 2-52 Software multiplexed pins of USB 2.0

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
244	USB2_OVRCUR0	muxctrl_reg89	GPIO13_0	USB2_OVRCUR0
245	USB2_PWREN0	muxctrl_reg90	GPIO13_1	USB2_PWREN0
246	USB2_OVRCUR1	muxctrl_reg91	GPIO13_2	USB2_OVRCUR1
247	USB2_PWREN1	muxctrl_reg92	GPIO13_3	USB2_PWREN1

Table 2-53 describes the software multiplexed pins of USB 2.0.

Table 2-53 Description of the software multiplexed pins of USB 2.0

Signal	Direction	Description
GPIO13_0	I/O	GPIO
GPIO13_1	I/O	GPIO
GPIO13_2	I/O	GPIO
GPIO13_3	I/O	GPIO
USB2_OVRCUR0	I	Overcurrent indicator of USB port 0, configurable level, and active high by default
USB2_OVRCUR1	I	Overcurrent indicator of USB port 1, configurable level, and active high by default
USB2_PWREN0	O	Power control output signal of USB port 0, configurable level, and active low by default
USB2_PWREN1	O	Power control output signal of USB port 1, configurable level, and active low by default

HDMI

Table 2-54 lists the software multiplexed pins of HDMI.

Table 2-54 Software multiplexed pins of HDMI

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
195	HDMI_HOTPLUG	muxctrl_reg93	GPIO13_4	HDMI_HOTPLUG
198	HDMI_CEC	muxctrl_reg94	GPIO13_5	HDMI_CEC
196	HDMI_SDA	muxctrl_reg95	GPIO13_6	HDMI_SDA
197	HDMI_SCL	muxctrl_reg96	GPIO13_7	HDMI_SCL

Table 2-55 describes the software multiplexed pins of HDMI.

Table 2-55 Description of the software multiplexed pins of HDMI

Signal	Direction	Description
GPIO13_4	I/O	GPIO
GPIO13_5	I/O	GPIO

Signal	Direction	Description
GPIO13_6	I/O	GPIO
GPIO13_7	I/O	GPIO
HDMI_CEC	I/O	CEC channel signal of the HDMI
HDMI_HOTPLUG	I	Hot plug detection signal of the HDMI
HDMI_SCL	I/O	DDC clock signal of the HDMI
HDMI_SDA	I/O	DDC data/address signal of the HDMI

SATA

Table 2-56 lists the software multiplexed pins of SATA.

Table 2-56 Software multiplexed pins of SATA

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
96	SATA_LED_N0	muxctrl_reg97	GPIO10_3	SATA_LED_N0
97	SATA_LED_N1	muxctrl_reg98	GPIO10_4	SATA_LED_N1

Table 2-57 describes the software multiplexed pins of SATA.

Table 2-57 Description of the software multiplexed pins of SATA

Signal	Direction	Description
GPIO10_3	I/O	GPIO
GPIO10_4	I/O	GPIO
SATA_LED_N0	O	LED indicator signal of SATA port 0, active low
SATA_LED_N1	O	LED indicator signal of SATA port 1, active low

2.7 Hardware Multiplexed Pins

SFC

Table 2-58 lists the hardware multiplexed pin of the SFC.

Table 2-58 Hardware multiplexed pin of the SFC

Pin	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
122	SFC_CLK	SFC_BOOT_MODE

Table 2-59 describes the hardware multiplexed pin of the SFC.

Table 2-59 Description of the hardware multiplexed pin of the SFC

Signal	Direction	Description
SFC_BOOT_MODE	I	Boot address mode of the SPI NOR flash when SFC_DEVICE_MODE is 0 0: 3-byte address mode 1: 4-byte address mode Boot mode of the SPI NAND flash when SFC_DEVICE_MODE is 1 0: 1-wire boot mode 1: 4-wire boot mode

JTAG

Table 2-60 lists the hardware multiplexed pins of the JTAG.

Table 2-60 Hardware multiplexed pins of the JTAG

Pin	Pad Signal	Multiplexed Signal 1 (jtag_en == 1'b0)
91	JTAG_TRSTN	GPIO12_0
87	JTAG_TCK	GPIO12_1
88	JTAG_TMS	GPIO12_2
86	JTAG_TDO	GPIO12_3
89	JTAG_TDI	GPIO12_4

Table 2-61 describes the hardware multiplexed pin of the JTAG.

Table 2-61 Description of the hardware multiplexed pin of the JTAG

Signal	Direction	Description
GPIO12_0	I/O	GPIO

Signal	Direction	Description
GPIO12_1	I/O	GPIO
GPIO12_2	I/O	GPIO
GPIO12_3	I/O	GPIO
GPIO12_4	I/O	GPIO

SYS

Table 2-62 lists the hardware multiplexed pin of the SYS.

Table 2-62 Hardware multiplexed pin of the SYS

Pin	Pad Signal	Multiplexed Signal 1 (por_bypass == 1'b0)
118	WDG_RSTN	SYS_RSTN_OUT

Table 2-63 describes the hardware multiplexed pin of the SYS.

Table 2-63 Description of the hardware multiplexed pin of the SYS

Signal	Direction	Description
SYS_RSTN_OUT	O	System reset output, active low

2.8 Electrical Specifications

2.8.1 Power Consumption Parameters

Table 2-64 describes power consumption parameters.

CAUTION

- The values of power consumption parameters are provided based on typical application scenarios.
- Design board power supplies by following the *Hi3520D V300 Hardware Design User Guide*.

Table 2-64 Power consumption parameters

Parameter	Description	Typ	Max	Unit
Core power	Core power	1128	1578	mA
3.3 V power	Interface current	162	170	mA
1.5 V power	DDR interface current	237	257	mA

NOTE

The typical application scenarios are as follows:

- 4x720p@30 fps H.264 encoding+4xCIF@30 fps H.264 encoding+4x720p@30 fps H.264 decoding+4x720p@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

2.8.2 Temperature and Thermal Resistance Parameters

Table 2-65 describes temperature and thermal resistance parameters.

NOTE

- The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.
- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.
- Design heat dissipation by following the *Hi3520D V300 Hardware Design User Guide*.
- The chip can be stored in the sealed packaging bag for up to 12 months when the temperature is below 40ºC (104ºF) and the relative humidity (RH) is below 90%.
- After the packaging bag is opened, the following conditions must be met before the component is used in the reflow soldering process or other high-temperature processes:

  a. The process is complete within 168 hours at 30ºC (86ºF) or lower and at most 60% RH.

  b. The component is stored at the RH lower than 10%.
- The soldering temperature curve is based on the J-STD-020D.1 standard.

Table 2-65 Temperature and thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature	T_A	0	None	70	ºC
Rated temperature	T_{JMAX}	–20	None	105	ºC
Junction-to-ambient thermal resistance	θ_{JA}	None	19	None	ºC/W
Junction-to-board thermal resistance	θ_{JB}	None	10	None	ºC/W
Junction-to-case thermal resistance	θ_{JC}	None	6	None	ºC/W

CAUTION

The ambient temperature is used in chip operating conditions, while the junction temperature only serves as a reference during thermal simulation.

2.8.3 Operating Conditions

CAUTION

The voltage ranges in Table 2-66 are applicable on the condition that the SVB circuit is used on the demo board of the customer and the resistance-capacitance parameters of the SVB circuit must be designed by completely following table 1-3 and table 1-4 in section 1.1.6 "SVB Dynamic Voltage Scaling" in the *Hi3520D V300 Hardware Design User Guide*.

Table 2-66 to Table 2-67 describes operating conditions.

Table 2-66 Operating conditions for the SVB related power supply

Symbol	Description	Min	Typ	Max	power supply noise Vpp	Unit
DVDD_CORE	Core power	1.15	1.20	1.25	0.06	V
AVDD_VP_SATA0 AVDD_VP_SATA1	SATA core analog power	1.15	1.20	1.25	0.06	V
AVDD_VPTX_SATA0 AVDD_VPTX_SATA1	SATA core analog power	1.15	1.20	1.25	0.06	V
AVDD_PLL	PLL core analog power	1.15	1.20	1.25	0.06	V
AVCC_HDMITX	HDMI TX core analog power	1.15	1.20	1.25	0.06	V
AVCC_USB	USB core analog power	1.15	1.20	1.25	0.06	V

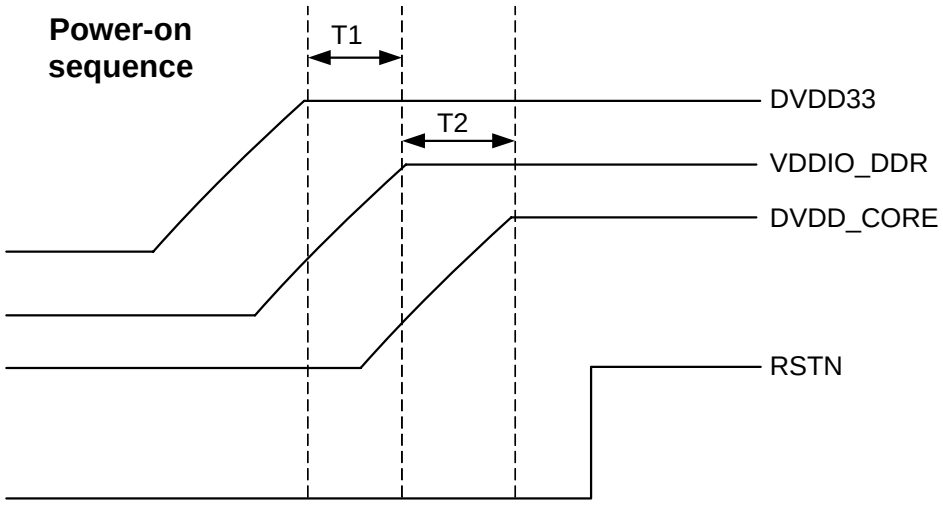
Table 2-67 Operating conditions for the power supply under normal voltage

Symbol	Description	Min	Typ	Max	Unit
DVDD33	I/O power	2.97	3.3	3.63	V
AVDD33_VPH_SATA0 AVDD33_VPH_SATA1	3.3 V SATA analog power	3.125	3.3	3.6	V
DVDD3318_SFC	SFC I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
DVDD3318_I2S	I^2S1/I^2S2 I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
DVDD3318_VI	I^2S0/VI/SPI I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
AVDD_EFUSE	2.5 V eFUSE analog power	2.25	2.5	2.75	V
DVDDIO_RGMII	RGMII power	2.97/2.25	3.3/2.5	3.63/2.75	V
AVDD33_PLL	3.3 V PLL analog power	3.135	3.3	3.465	V
AVDD33_RTC	RTC analog power	3.0	3.3	3.63	V
AVDD33_VDAC	3.3 V VDAC RGB analog power	3.125	3.3	3.465	V
DVDD33_VDAC	3.3 V VDAC digital power	2.97	3.3	3.63	V
AVDD33_HDMITX	3.3 V HDMI TX analog power	3.125	3.3	3.465	V
AVDD33_USB	3.3 V USB analog power	3.125	3.3	3.6	V
AVDD_DDRPLL_0 AVDD_DDRPLL_1 AVDD_DDRPLL_2	3.3 V DDR3 PLL analog power	3.125	3.3	3.465	V
VDDIO_DDR	DDR3 interface power	1.425	1.5	1.575	V
VDDIO_DDR_CK	DDR3 clock interface power	1.425	1.5	1.575	V

2.8.4 Power-On and Power-Off Sequences

- Power on power supplies by following the sequence in Figure 2-6.

Figure 2-6 Power-on sequence

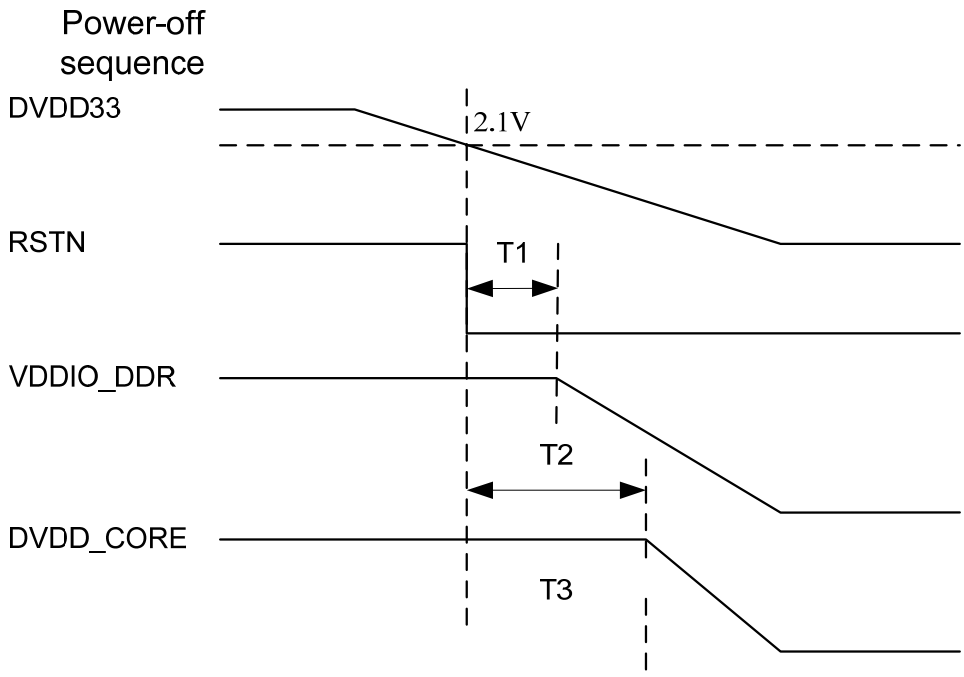


NOTE

T1 + T2 ≤ 100 ms; T2 > 0; T1 > 0.

- Power off power supplies by following the sequence in Figure 2-7.

Figure 2-7 Power-off sequence



NOTE

T1>0; T2>0.

2.8.5 DC and AC Electrical Parameters

Table 2-68 to Table 2-70 describe DC electrical parameters.

Table 2-68 DC electrical parameters (DVDD33 = 3.3 V, some interfaces support the 5 V input voltage)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD33	Interface voltage	3.125	3.3	3.6	V	-
V_{IH}	High-level input voltage	2.0	-	DVDD33 + 0.3	V	Incompatible with the 5 V input voltage. Some interfaces support the 5 V input voltage, and the maximum input voltage is 5.5 V.
V_{IL}	Low-level input voltage	–0.3	-	0.8	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	2.4	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.4	V	-
R_{PU}	Internal pull-up resistor	80	90	100	kΩ	-
R_{PD}	Internal pull-down resistor	80	90	100	kΩ	-
R_{PU8k}	8 kΩ pull-up resistor	7.1	8.5	10	kΩ	-
R_{PD8k}	8 kΩ pull-down resistor	7.1	8.4	10	kΩ	-

Table 2-69 DC electrical parameters (DVDD332518 = 2.5 V, some interfaces support the 5 V input voltage)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD332518	Interface voltage	2.25	2.5	2.75	V	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{IH}	High-level input voltage	1.7	-	DVDD 332518 + 0.3	V	Incompatible with the 5 V input voltage. Some interfaces support the 5 V input voltage, and the maximum input voltage is 5.5 V.
V_{IL}	Low-level input voltage	–0.3	-	0.7	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	1.8	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.5	V	-
R_{PU}	Internal pull-up resistor	80	90	100	kΩ	-
R_{PD}	Internal pull-down resistor	80	90	100	kΩ	-
R_{PU8k}	8 kΩ pull-up resistor	6.7	8.56	10.63	kΩ	-
R_{PD8k}	8 kΩ pull-down resistor	6.49	8.3	10.3	kΩ	-

Table 2-70 DC electrical parameters (DVDD3318 = 1.8 V, some interfaces support the 5 V input voltage)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD3318	Interface voltage	1.71	1.8	1.98	V	1.8 V NAND flash interface
V_{IH}	High-level input voltage	0.65 x DVDD3318	-	DVDD 3318 + 0.3	V	
V_{IL}	Low-level input voltage	–0.3	-	0.35 x DVDD 3318	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{OH}	High-level output voltage	DVDD3318 − 0.45	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.45	V	-
R_{PU}	Internal pull-up resistor	80	90	100	kΩ	-
R_{PD}	Internal pull-down resistor	80	90	100	kΩ	-
R_{PU8k}	8 kΩ pull-up resistor	7.4	9	11	kΩ	
R_{PD8k}	8 kΩ pull-down resistor	7.1	8.9	11	kΩ	

Table 2-71 describes DC electrical parameters in DDR3 mode.

Table 2-71 DC electrical parameters in DDR3 mode (VDDIO_DDR = 1.5 V, DDR3 mode)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.425	1.5	1.575	V	-
Vref	Reference voltage	0.49 x VDDIO_DDR	0.5 x VDDIO_DDR	0.51 x VDDIO_DDR	-	(0.49−0.51) x DDR_DVDDIO
VTT	Termination voltage	Vref − 40	Vref	Vref + 40	mV	-
$V_{IH(DC)}$	High-level input voltage	Vref + 0.1	-	VDDIO_DDR + 0.3	V	-
$V_{IL(DC)}$	Low-level input voltage	–0.3	-	Vref − 0.1	V	-
V_{OH}	High-level output voltage	0.8 x VDDIO_DDR	-	(1 + 0.1) x VDDIO_DDR	V	The drive voltage is configurable.
V_{OL}	Low-level output voltage	0	-	0.2 x VDDIO_DDR	V	The drive voltage is configurable.
Output impedance	-	34	-	80	Ω	

Table 2-72 describes AC electrical parameters in DDR3 mode.

Table 2-72 AC electrical parameters in DDR3 mode (DDR_VDDQ = 1.5 V, DDR3 mode)

Symbol	Description	Min	Max	Unit	Remarks
$V_{IH(AC)}$	High-level input voltage	Vref + 0.15	VDDIO_DDR + 0.3	V	-
$V_{IL(AC)}$	Low-level input voltage	-	Vref − 0.15	V	-
V_{OH}	High-level output voltage	VTT + 0.1 x VDDIO_DDR	-	V	-
V_{OL}	Low-level output voltage	-	VTT − 0.1 x VDDIO_DDR	V	-

2.9 PCB Design Recommendations

For details about printed circuit board (PCB) design recommendations, see the *Hi3520D V300 Hardware Design User Guide*.

2.10 Interface Timings

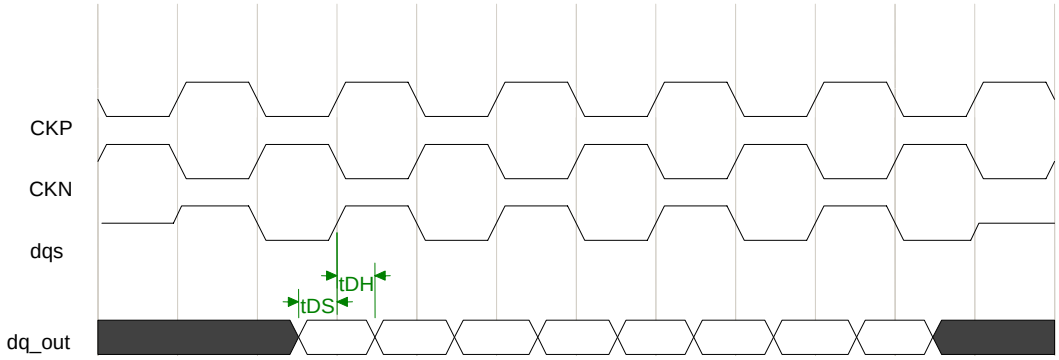
2.10.1 DDR Interface Timings

2.10.1.1 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are tDS and tDH.

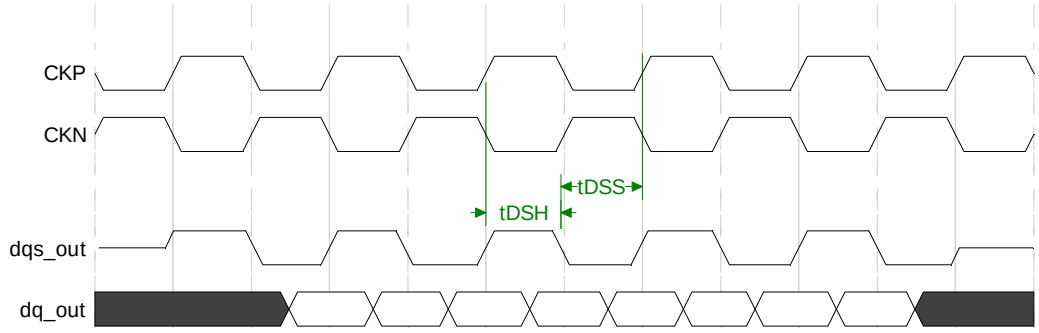
Figure 2-8 Write timing of dqs_out relative to dq_out for the DDR3



Write Timings of dqs_out Relative to CK

Figure 2-9 shows the write timing of dqs_out relative to CK for the DDR3.

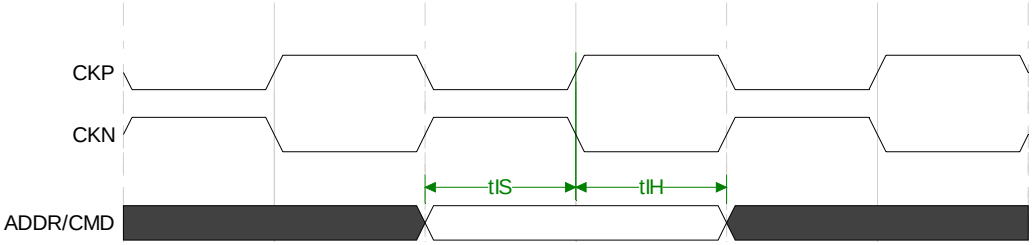
Figure 2-9 Write timing of dqs_out relative to CK for the DDR3



Write Timing of CMD/ADDR Relative to CK

Figure 2-10 shows the write timing of CMD/ADDR relative to CK.

Figure 2-10 Write timing of CMD/ADDR relative to CK



2.10.1.2 Read Timings

Read Timing of CMD/ADDR Relative to CK

The read timing of CMD/ADDR relative to CK is the same as the "Write Timing of CMD/ADDR Relative to CK".

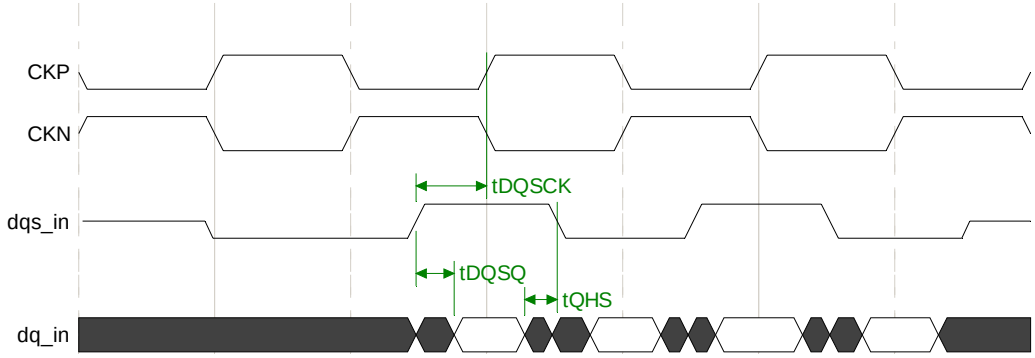
Read Timings of dqs_in Relative to dq_in

The read timings of dqs_in relative to dq_in are classified into the DDRn SDRAM output timing, dqs_in timing on the DDR PHY side, and dq_in timing on the DDR PHY side.

For the DDR SDRAM output timing, the phases of DQS and CK are the same in the ideal condition; however, there is a tDQSCK skew between DQS and CK. The value of tDQSCK is 0.35 ns. tDQSQ is the jitter of the last valid DQ relative to DQS and its value is 0.2 ns; tQHS is the jitter of the first valid DQ relative to DQS and its value is 0.3 ns.

Figure 2-11 shows the output timing of the DDRn SDRAM.

Figure 2-11 Output timing of the DDRn SDRAM



2.10.1.3 Timing Parameters

The timings of the DDR interface comply with the JEDEC standards including JESD79-2E and JESD79-3B standards. All the timings in this document are output on the DDR PHY side.

The Hi3521A is based on the timing parameters of the DDR3-1600 SDRAMs.

Table 2-73 and Table 2-74 describe the clock parameters of the DDR3-1600 SDRAM.

Table 2-73 DDR3 clock parameters

Parameter	Typ	Unit
DDR clock frequency	800.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	47.000	%
Clock skew	0.100	ns

Table 2-74 Parameters for the DDR3-1600 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.025	ns
Hold time, DQ/DM to DQS	tDH	0.100	ns
Skew between DQS and DQ	tDQSQ	0.150	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.125	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.200	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.300	ns

2.10.2 SFC Interface Timings

Figure 2-12 shows the SFC input timing.

Figure 2-12 SFC input timing

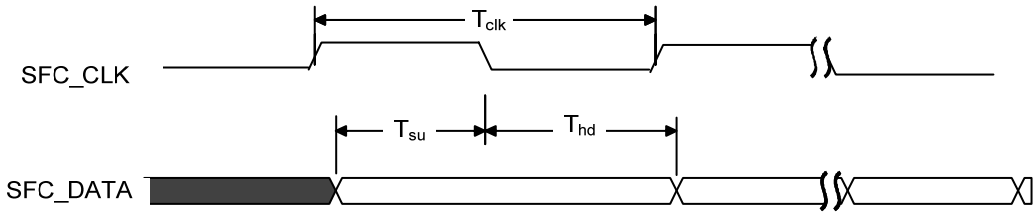


Table 2-75 describes the SFC input timing parameters.

Table 2-75 SFC input timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK	T_{clk}	13	None	83.2	ns
Input signal setup time	T_{su}	6	None	None	ns
Input signal hold time	T_{hd}	1.1	None	None	ns

Figure 2-13 shows the SFC output timing.

Figure 2-13 SFC output timing

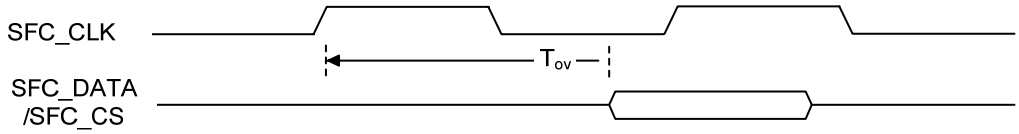


Table 2-76 describes the SFC output timing parameters.

Table 2-76 SFC output timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFCCLK	T	13.3	None	83.2	ns
Output data signal delay	T_{ov}	0	None	6.3	ns
Output CS signal delay	T_{ov}	0	None	6.3	ns

2.10.3 Ethernet MAC Port Timings

2.10.3.1 MII Timings

The Hi3521A provides standard MIIs that comply with the MII timing standard. These interfaces are used to connect to the physical layer (PHY).

Figure 2-14 shows the 100 Mbit/s RX timing of the MII.

Figure 2-14 100 Mbit/s RX timing of the MII

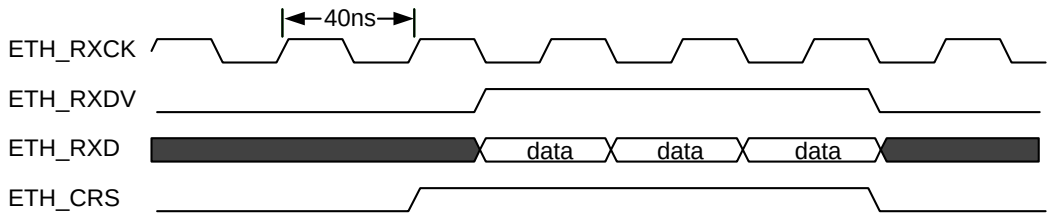


Figure 2-15 shows the 100 Mbit/s TX timing of the MII.

Figure 2-15 100 Mbit/s TX timing of the MII

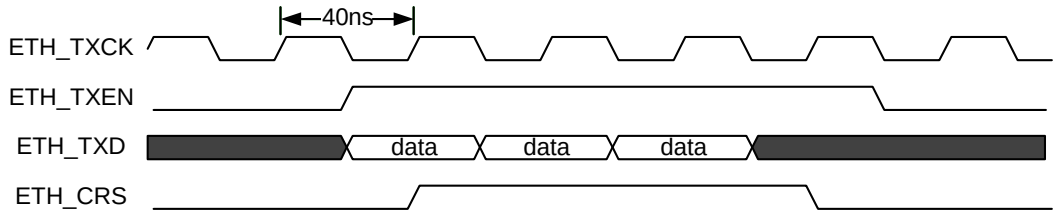


Figure 2-16 shows the 10 Mbit/s RX timing of the MII.

Figure 2-16 10 Mbit/s RX timing of the MII

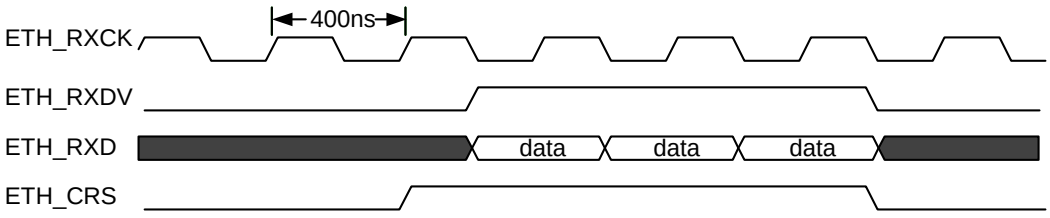


Figure 2-17 shows the 10 Mbit/s TX timing of the MII.

Figure 2-17 10 Mbit/s TX timing of the MII

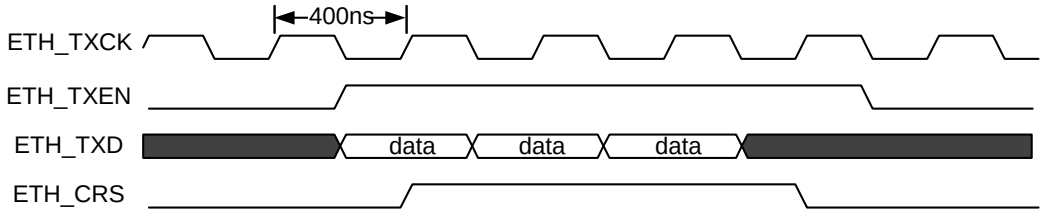


Figure 2-18 shows the RX timing parameters of the MII.

Figure 2-18 RX timing parameters of the MII

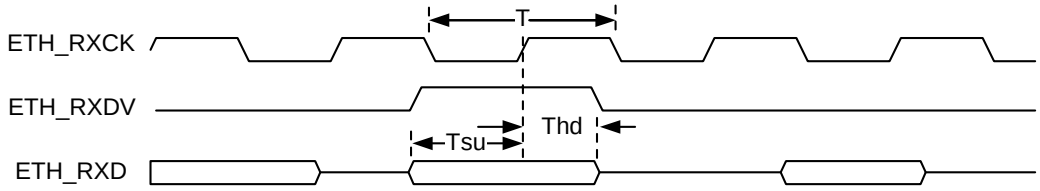


Figure 2-19 shows the TX timing parameters of the MII.

Figure 2-19 TX timing parameters of the MII

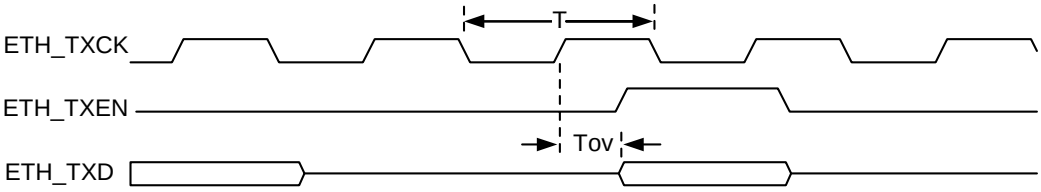


Table 2-77 describes the MII timing parameters.

Table 2-77 MII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
MII clock cycle	T	RGMII_RXC, RGMII_TXCK	400 (10 Mbit/s)	400	ns
			40 (100 Mbit/s)	40	
MII signal setup time	Tsu (RX)	RGMII_RXE, RGMII_RXD, RGMII_RXD[3:0], RGMII_RGMII_CRS, RGMII_RGMII_COL	10	None	ns

Parameter	Symbol	Signal	Min	Max	Unit
MII signal hold time	Thd (RX)	RGMII_RXE, RGMII_RXDV, RGMII_RXD[3:0], RGMII_RGMII_CRS, RGMII_RGMII_COL	10	None	ns
MII output signal delay	Tov (MIITX)	RGMII_TXD[3:0], RGMII_TXE, RGMII_TXER	0	25	ns

2.10.3.2 RMII Timings

Figure 2-20 shows the 100 Mbit/s RX timing of the RMII.

Figure 2-20 100 Mbit/s RX timing of the RMII

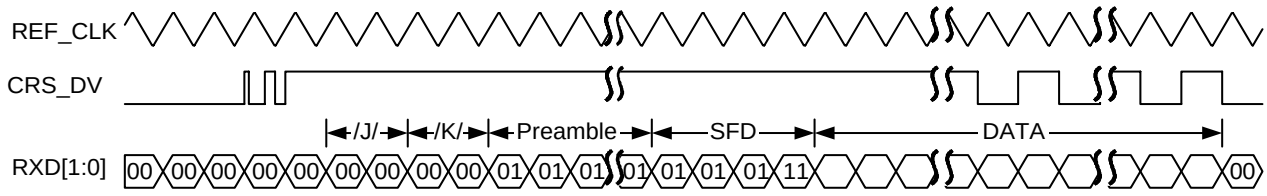


Figure 2-21 shows the 100 Mbit/s TX timing of the RMII interface.

Figure 2-21 100 Mbit/s TX timing of the RMII

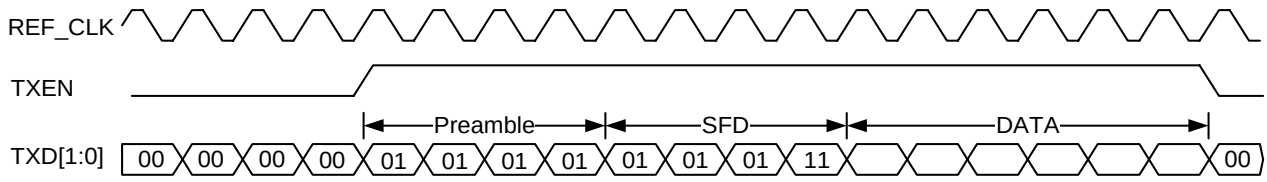


Figure 2-22 shows the 10 Mbit/s RX timing of the RMII.

Figure 2-22 10 Mbit/s RX timing of the RMII

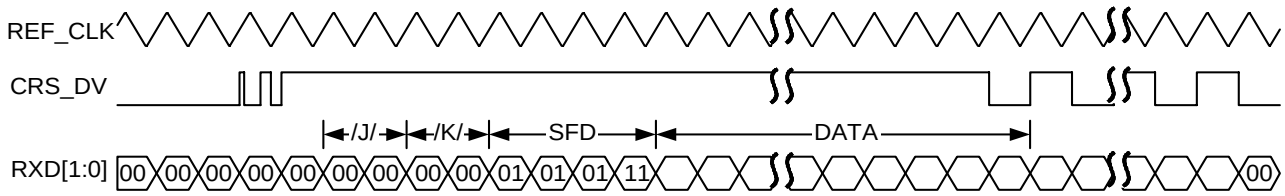


Figure 2-23 shows the 10 Mbit/s TX timing of the RMII.

Figure 2-23 10 Mbit/s TX timing of the RMII

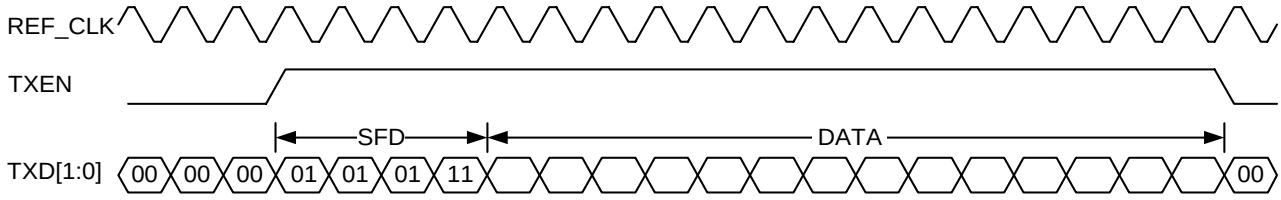


Figure 2-24 shows the timing parameters of the RMII.

Figure 2-24 Timing parameters of the RMII

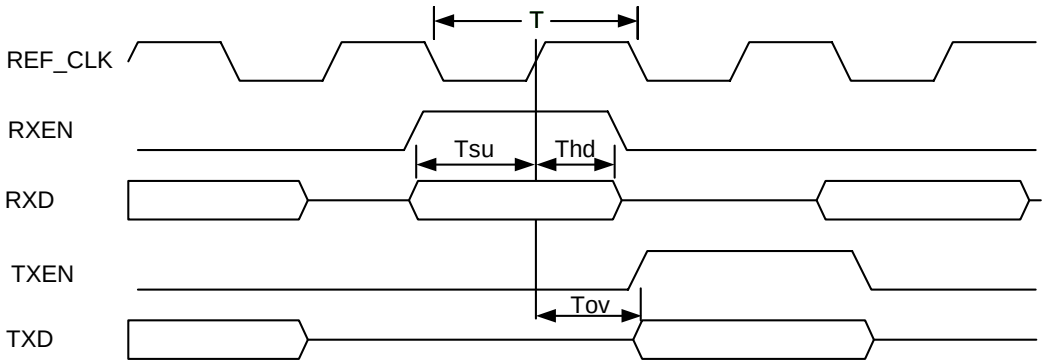


Table 2-78 describes the RMII timing parameters of the RMII.

Table 2-78 Timing parameters of the RMII

Parameter	Symbol	Signal	Min	Max	Unit
RMII clock cycle	T	RGMII_TXCKOUT	20	20	ns
Setup time of RMII signal	Tsu (RX)	RGMII_RXDV, RGMII_RXD[1:0], RGMII_RXER	4	None	ns
Hold time of RMII signal	Thd (RX)	RGMII_RXDV, RGMII_RXD[1:0], RGMII_RXER	2	None	ns

Parameter	Symbol	Signal	Min	Max	Unit
RMII output signal delay	Tov (TX)	RGMII_TXEN, RGMII_TXD[1:0]	3	16	ns

2.10.3.3 RGMII Timings

Figure 2-25 shows the 1000 Mbit/s RX timing of the RGMII.

Figure 2-25 1000 Mbit/s RX timing of the RGMII

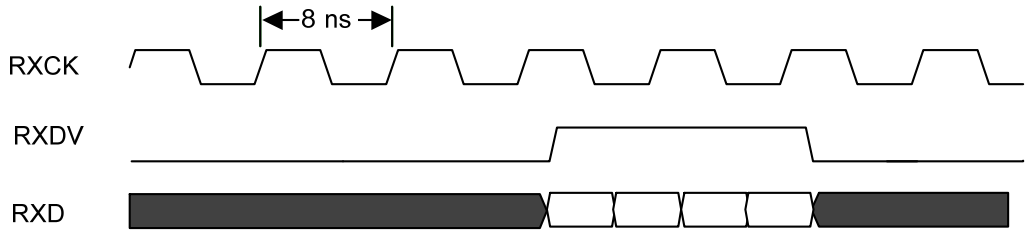


Figure 2-26 shows the 1000 Mbit/s TX timing of the RGMII.

Figure 2-26 1000 Mbit/s TX timing of the RGMII

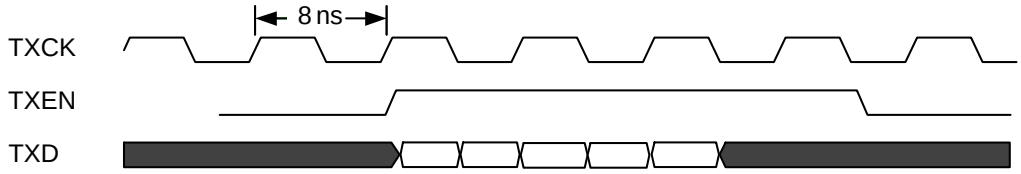


Table 2-79 describes the timing parameters of the RGMII.

Table 2-79 Timing parameters of the RGMII

Parameter	Symbol	Signal	Min	Max	Unit
RGMII clock cycle	T	RGMII_RXCK, RGMII_TXCK	8	8	ns
RGMII signal setup time	Tsu (RX)	RGMII_RXDV, RGMII_RXD[3:0]	1	None	ns
RGMII signal hold time	Thd (RX)	RGMII_RXDV, RGMII_RXD[3:0]	1	None	ns
RGMII output signal delay	Tov (TX)	RGMII_TXD[3:0], RGMII_TXEN	-0.5	0.5	ns

2.10.3.4 MDIO Interface Timings

Figure 2-27 shows the read timing of the MDIO interface.

Figure 2-27 Read timing of the MDIO interface

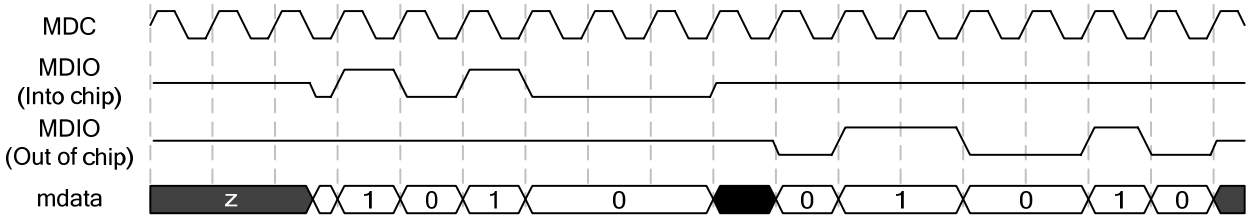


Figure 2-28 shows the write timing of the MDIO interface.

Figure 2-28 Write timing of the MDIO interface

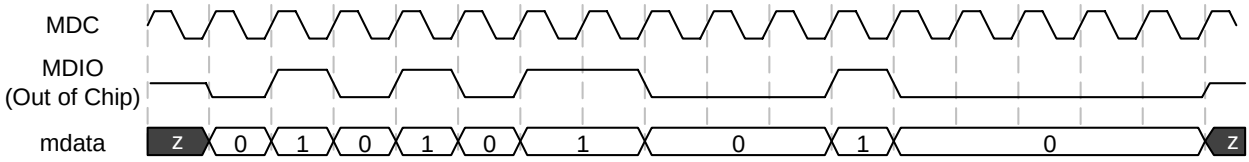


Figure 2-29 shows the RX timing parameters of the MDIO interface.

Figure 2-29 RX timing parameters of the MDIO interface

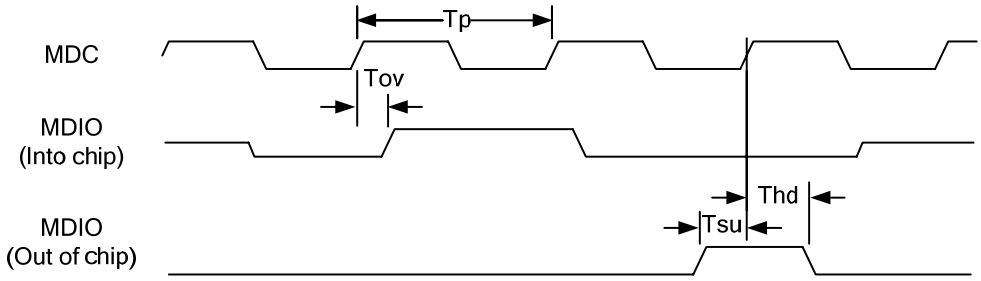


Table 2-80 describes the timing parameters of the MDIO interface.

Table 2-80 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data RX delay	Tov	MDIO	0	300	ns
MDIO clock cycle	Tp	MDCK	400	400	ns
MDIO data TX setup time	Tsu	MDIO	10	None	ns
MDIO data TX hold time	Thd	MDIO	10	None	ns

2.10.4 VI Interface Timing

Figure 2-30 shows the VI interface timing in single-edge mode.

Figure 2-30 VI interface timing in single-edge mode

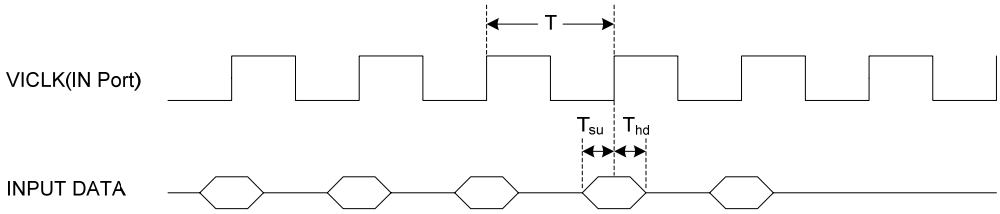


Table 2-81 describes the VI interface timing parameters.

Table 2-81 VI interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.73	None	None	ns
Input signal setup time	T_{su}	4.43	None	None	ns
Input signal hold time	T_{hd}	0.5	None	None	ns

Table 2-82 describes the VI interface timing parameters in dual-edge mode.

Table 2-82 VI interface timing parameters in dual-edge mode

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.73	-	-	ns
Input signal setup time	T_{su}	1	-	-	ns
Input signal hold time	T_{hd}	0.5	-	-	ns
duty cycle requirement	-	47.5	50	52.5	%

2.10.5 AIAO Interface Timings

2.10.5.1 I²S Interface Timing

Figure 2-31 shows the RX timing of the I^2S interface.

Figure 2-31 RX timing of the I²S interface

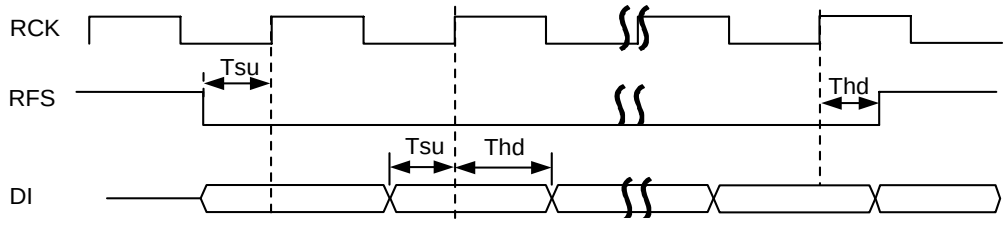


Figure 2-32 shows the TX timing of the I²S interface.

Figure 2-32 TX timing of the I²S interface

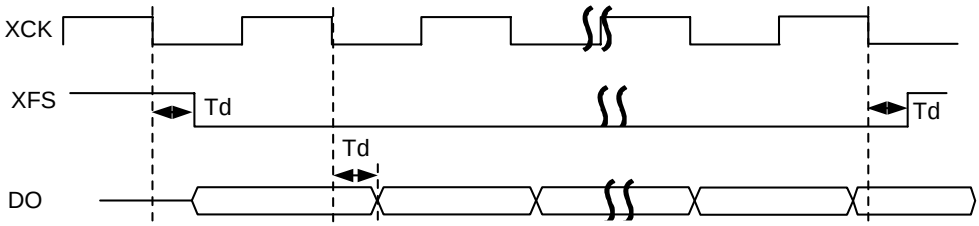


Table 2-83 describes the timing parameters of the I²S interface.

Table 2-83 Timing parameters of the I²S interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

2.10.5.2 PCM Interface Timings

Figure 2-33 shows the RX timing of the PCM interface.

Figure 2-33 RX timing of the PCM interface

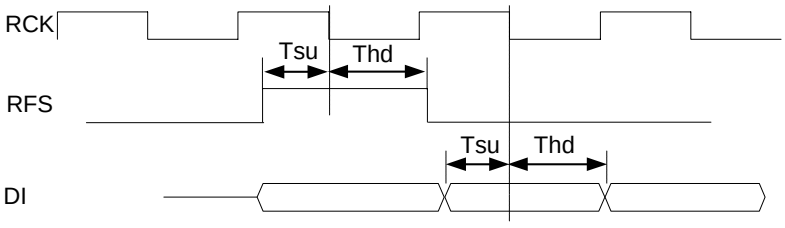


Figure 2-34 shows the TX timing of the PCM interface

Figure 2-34 TX timing of the PCM interface

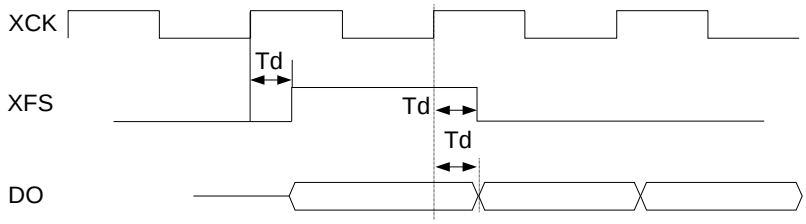


Table 2-84 describes the timing parameters of the PCM interface.

Table 2-84 Timing parameters of the PCM interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

2.10.6 I²C Interface Timing

Figure 2-35 shows the I²C transfer timing.

Figure 2-35 I²C transfer timing

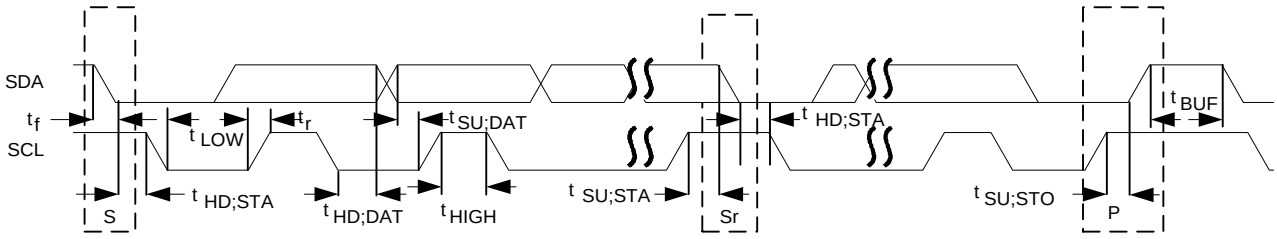


Table 2-85 describes the timing parameters of the I²C interface.

Table 2-85 Timing parameters of the I²C interface

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz
Start hold time	$t_{HD;STA}$	4.0	None	0.6	None	µs
SCL low-level cycle	t_{LOW}	4.7	None	1.3	None	µs

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL high-level cycle	t_{HIGH}	4.0	None	0.6	None	µs
Start setup time	$t_{SU;STA}$	4.7	None	0.6	None	µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU;DAT}$	250	None	100	None	ns
Serial data (SDA) and SCL rising time	t_r	None	1000	20 + 0.1 x C_b	300	ns
SDA and SCL falling time	t_f	None	300	20 + 0.1 x C_b	300	ns
End setup time	$t_{SU;STO}$	4.0	None	0.6	None	µs
Bus release time from start to end	t_{BUF}	4.7	None	1.3	None	µs
Bus load	C_b	None	400	None	400	pF
Low-level noise tolerance	V_{nL}	0.1 x V_{DD}	None	0.1 x V_{DD}	None	V
High-level noise tolerance	V_{nH}	0.2 x V_{DD}	None	0.2 x V_{DD}	None	V

2.10.7 SPI Timings

NOTE

In Figure Figure 2-36 to Figure 2-38, the conventions are as follows:

- MSB = most significant bit
- LSB = least significant bit
- SPI_CK(0):spo = 0
- SPI_CK(1):spo = 1

Figure 2-36 shows the SPI clock (SPICK) timing.

Figure 2-36 SPICK timing

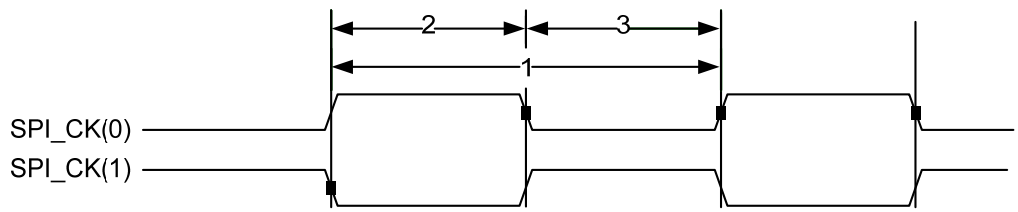


Figure 2-37 and Figure 2-38 show the SPI timings in master mode.

Figure 2-37 SPI timing in master mode (sph = 0)

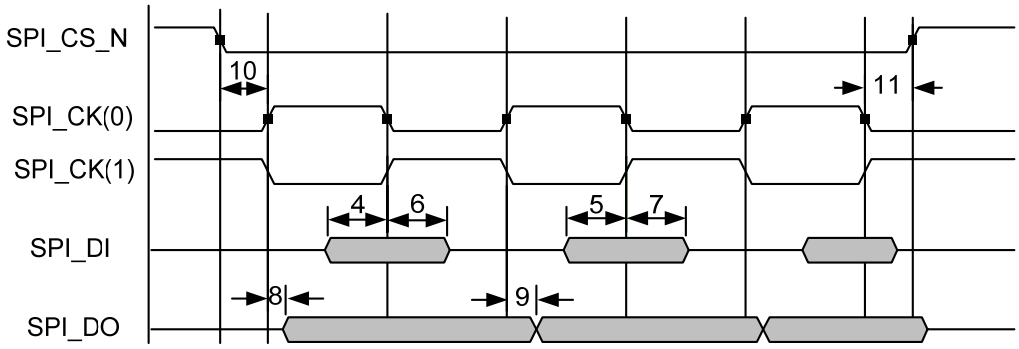


Figure 2-38 SPI timing in master mode (sph = 1)

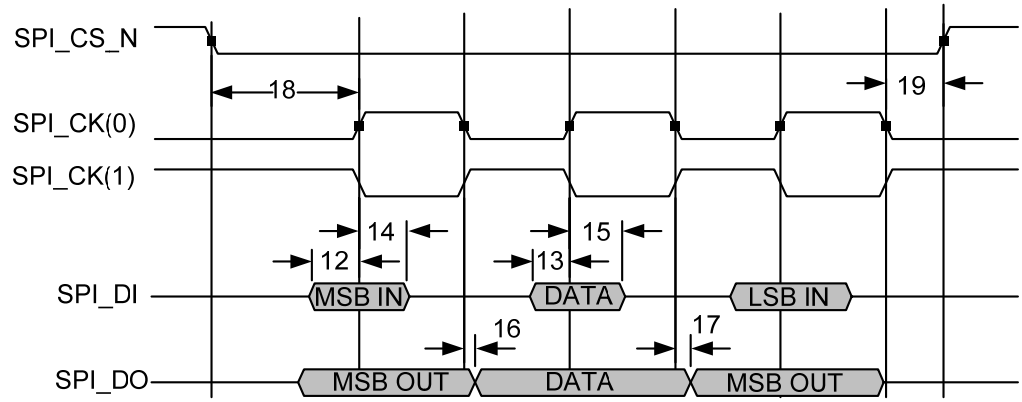


Table 2-86 describes the SPI timing parameters.

Table 2-86 SPI timing parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_CK	tc	None	None	None	ns
2	Pulse duration, SPI_CK high (all master modes)	tw1	None	None	None	ns
3	Pulse duration. SPI_CK low (all master modes)	tw2	None	None	None	ns
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	None	None	None	ns
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	None	None	None	ns
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	None	None	None	ns
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	None	None	None	ns

No.	Parameter	Symbol	Min	Typ	Max	Unit
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	None	None	None	ns
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	None	None	None	ns
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	None	None	None	ns
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	None	None	None	ns
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	None	None	None	ns
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	None	None	None	ns
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	None	None	None	ns
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	None	None	None	ns
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	None	None	None	ns
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	None	None	None	ns
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	None	None	None	ns
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	None	None	None	ns

Contents

Figures

Tables

2 Hardware

2.1 Package and Pinout

2.1.1 Package

The Hi3521A uses the thin & fine-pitch ball grid array (TFBGA) package. It has 437 pins, its body size is 19 mm x 19 mm (0.91 in. x 0.91 in.), and its ball pitch is 0.8 mm (0.03 in.). Figure 2-1 to Figure 2-4 show the package of the Hi3521A. Table 2-1 shows the package specifications.

Figure 2-1 Top view

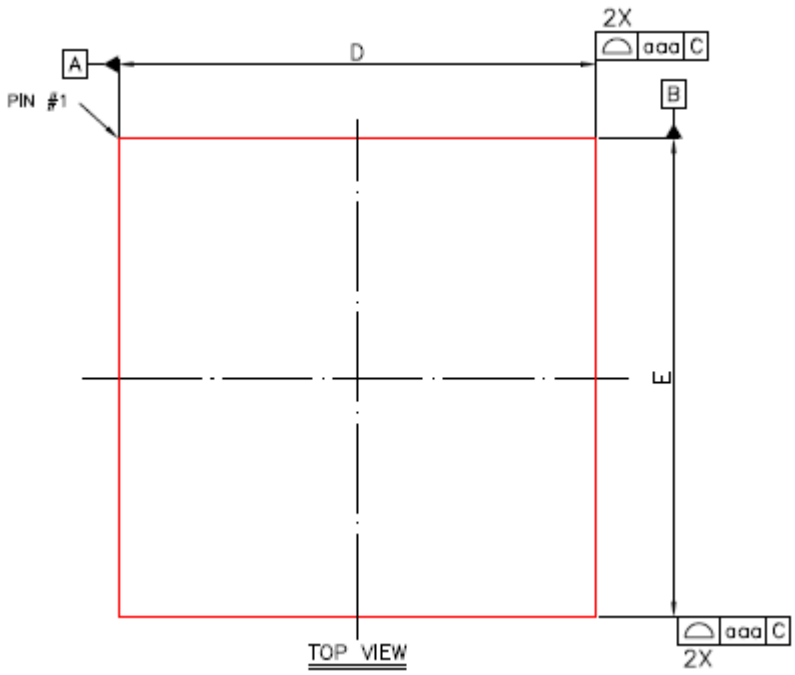


Figure 2-2 Bottom view

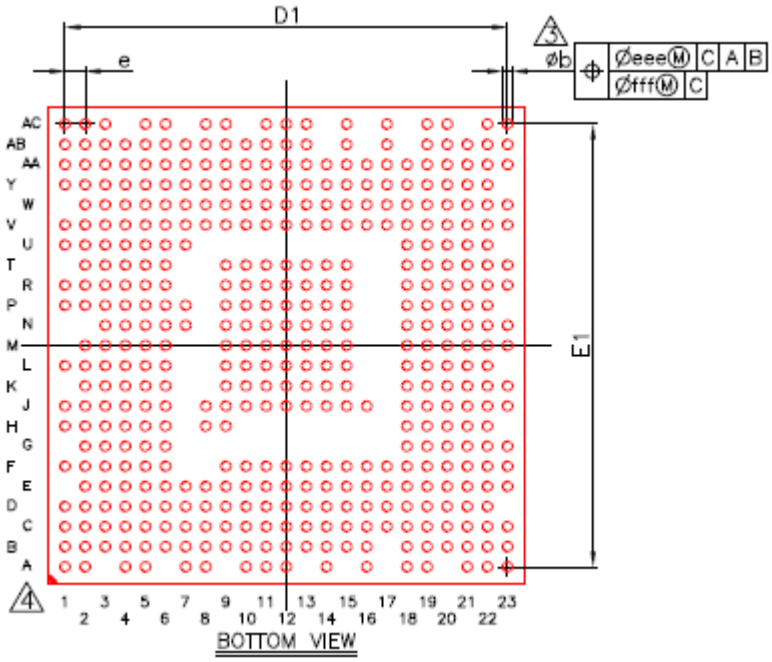


Figure 2-3 Side view

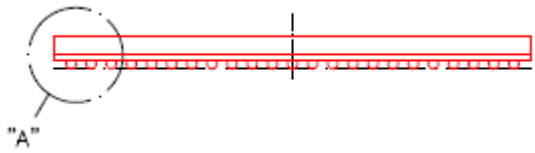


Figure 2-4 Enlarged view of detail "A"

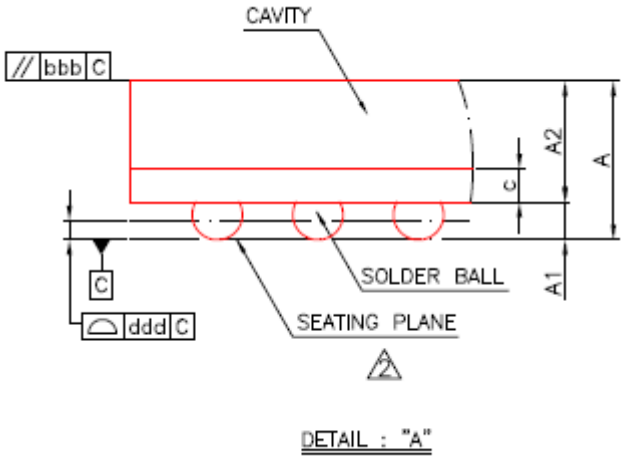


Table 2-1 Package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.19	1.26	1.33	0.047	0.050	0.052
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.15			0.006		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
5. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd

2.1.2 Pinout

Table 2-2 lists the pin quantity of the Hi3521A by type.

Table 2-2 Pin quantity

Pin Type	Quantity
I/O	225
Digital power	49
Digital GND	121
Others/Analog power	17
Others/Analog GND	25
Total	437

Pin Map

Figure 2-5 to Figure 2-8 show pin maps.

Figure 2-5 Pin map part 1 (A1–K12)

	01	02	03	04	05	06	07	08	09	10	11	12
A	VSS	GPIO0_1		USB2_OVRCUR1	USB2_OVRCUR0		USB2_DM1	USB2_REXT		RGMII_RXCK	VSS	RGMII_TXD0
B	GPIO0_3	GPIO0_2	PWM_OUT1	USB2_PWREN1	USB2_PWREN0	USB2_DM0	USB2_DP1	RGMII_RXD0	RGMII_RXD2	RGMII_RXD3	RGMII_TXCKOUT	RGMII_TXD1
C	GPIO0_5	GPIO0_4	GPIO0_0	PWM_OUT0	VSS	USB2_DP0	AVSS_USB	VSS	RGMII_RXD1	VSS	VSS	VSS
D	UART0_RXD	GPIO0_7	GPIO0_6	VSS	VSS	VSS	AVSS_USB	AVCC_USB	VSS	RGMII_RXDV	RGMII_COL	RGMII_CRS
E		UART0_TXD	UART0_CTSN	VSS	DVDD_CPU	DVDD_CPU	VSS	AVDD33_USB	AVSS_USB	VSS	RGMII_RXER	RGMII_TXEN
F	UART1_TXD	UART1_RXD	UART0_RTSN	VSS	DVDD_CPU	DVDD_CPU			VSS	DVDD33	VSS	VSS
G		VSS	VSS	VSS	VSS	VSS						
H	VSS	DDR_DQ11	DDR_DM1	DDR_DQ2	DDR_DQ6	DDR_ZQ		DVDD_CPU	DVDD_CPU			
J	DDR_DQ15	VSS	DDR_DQ13	VSS	DDR_DQ4	VDDIO_DDR		DVDD_CPU	DVDD_CPU	VSS	DVDD_CORE	VSS
K		DDR_DQ0	DDR_DQ9	VSS	DDR_DQ7	VDDIO_DDR			VSS	DVDD_CORE	DVDD_CORE	VSS

Figure 2-6 Pin map part 2 (A13–K23)

13	14	15	16	17	18	19	20	21	22	23	
	MDCK		HDMI_TX1N		HDMI_TXCN	HDMI_CEC		VGA_R	VGA_G	AVSS_VDAC	A
RGMII_TXD2	VSS	HDMI_TX2N	HDMI_TX1P		HDMI_TXCP	HDMI_SCL	VGA_VS	AVSS_VDAC	VGA_B	CVBS_OUT	B
RGMII_TXD3	AVSS_HDMITX	HDMI_TX2P	AVSS_HDMITX	HDMI_TX0N	AVSS_HDMITX	HDMI_SDA	VGA_HS	VSS	AVSS_VDAC	VDAC_REXT	C
EPHY_RSTN	MDIO	AVSS_HDMITX	AVSS_HDMITX	HDMI_TX0P	AVSS_HDMITX	HDMI_HOTPLUG	AVSS_RTC	RTC_XIN	RTC_XOUT		D
VSS	EPHY_CLK	RGMII_TXER	AVSS_HDMITX	AVDD33_HDMITX	AVSS_HDMITX	AVDD_BAT	AVSS_RTC	VSS	XOUT	XIN	E
DVDDIO_RGMII	VSS	VSS	AVSS_HDMITX	AVSS_HDMITX	VSS	VSS	I2C_SCL	VSS	SPI_CSN0	SPI_CSN1	F
					AVSS_RTC	I2C_SDA	SPI_SDI	SPI_SCLK	VSS	VI_ADC_REFCLK1	G
					AVDD33_RTC	VSS	SPI_SDO	VI3_DAT0	VI3_DAT1		H
AVCC_HDMITX	AVSS_VDAC	AVDD33_VDAC	AVSS_VDAC_0		DVDD33	VI3_DAT4	VI3_DAT5	VI3_DAT2	VI3_DAT3	VSS	J
AVSS_HDMITX	DVSS_VDAC	DVDD33_VDAC			VSS	VI3_DAT7	VSS	VI3_DAT6	VI3_CLK	VSS	K

Figure 2-7 Pin map part 3 (L1–AC12)

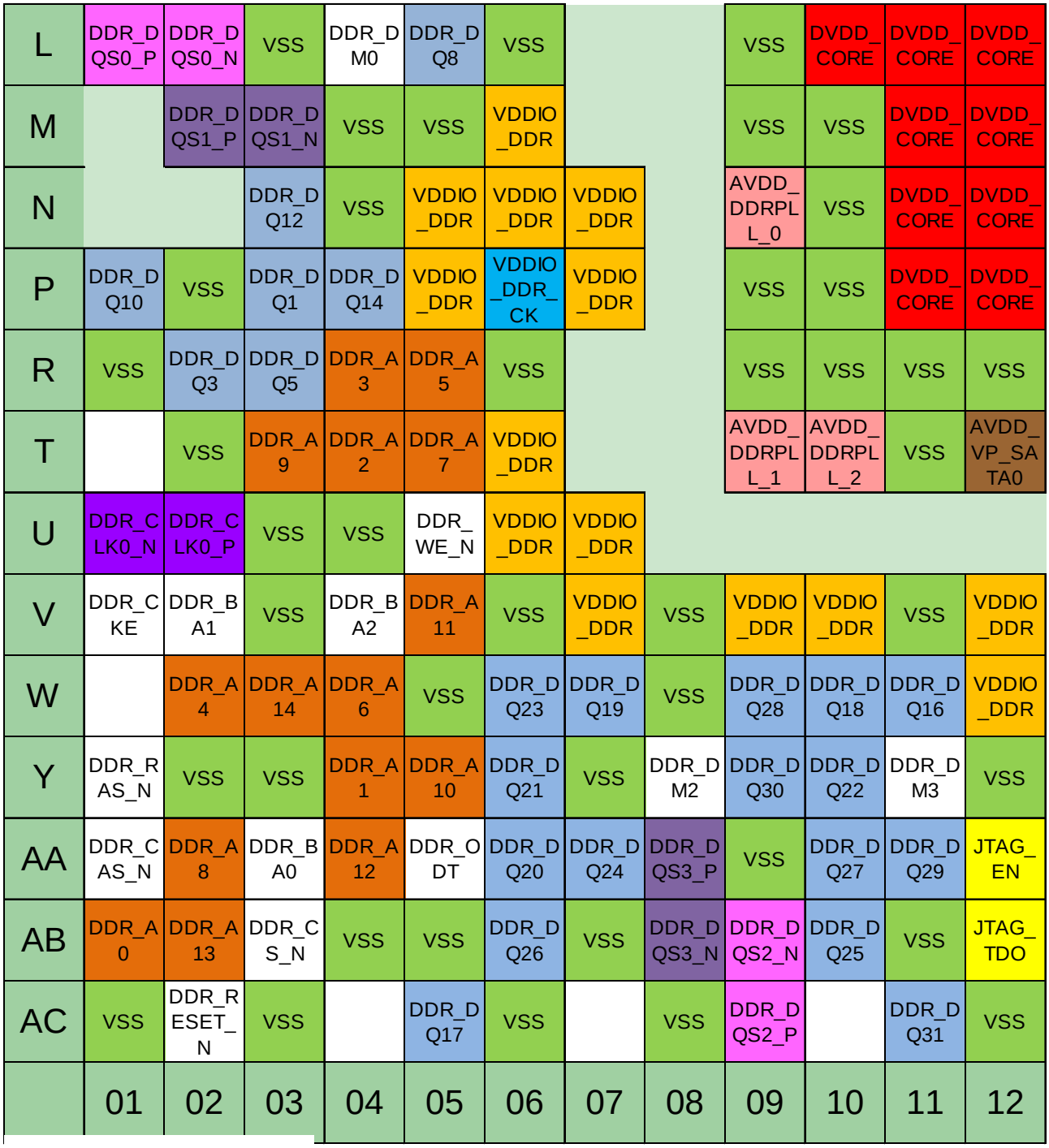
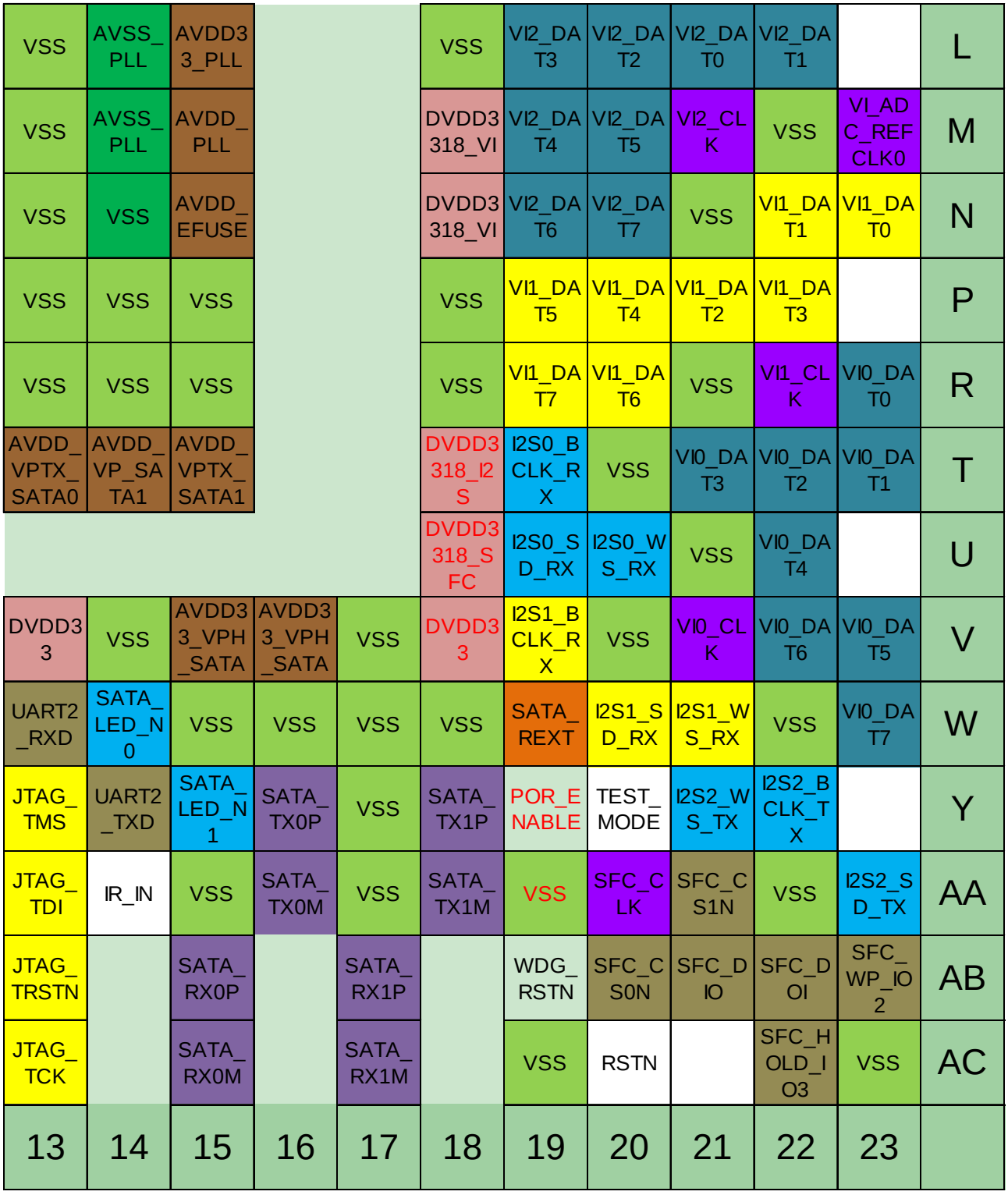


Figure 2-8 Pin map part 4 (L13–AC23)



Pin Arrangement

Table 2-3 lists the pins of the Hi3521A based on their positions.

Table 2-3 Pin arrangement

Position	Pin Name	Position	Pin Name	Position	Pin Name
A1	VSS	H19	VSS	T15	AVDD_VPTX_SATA1
A2	GPIO0_1	H20	SPI_SDO	T18	DVDD3318_I2S
A4	USB2_OVRCUR1	H21	VI3_DAT0	T19	I2S0_BCLK_RX
A5	USB2_OVRCUR0	H22	VI3_DAT1	T20	VSS
A7	USB2_DM1	J1	DDR_DQ15	T21	VI0_DAT3
A8	USB2_REXT	J2	VSS	T22	VI0_DAT2
A10	RGMII_RXCK	J3	DDR_DQ13	T23	VI0_DAT1
A11	VSS	J4	VSS	U1	DDR_CLK0_N
A12	RGMII_TXD0	J5	DDR_DQ4	U2	DDR_CLK0_P
A14	MDCK	J6	VDDIO_DDR	U3	VSS
A16	HDMI_TX1N	J8	DVDD_CPU	U4	VSS
A18	HDMI_TXCN	J9	DVDD_CPU	U5	DDR_WE_N
A19	HDMI_CEC	J10	VSS	U6	VDDIO_DDR
A21	VGA_R	J11	DVDD_CORE	U7	VDDIO_DDR
A22	VGA_G	J12	VSS	U18	DVDD3318_SFC
A23	AVSS_VDAC	J13	AVCC_HDMITX	U19	I2S0_SD_RX
B1	GPIO0_3	J14	AVSS_VDAC	U20	I2S0_WS_RX
B2	GPIO0_2	J15	AVDD33_VDAC	U21	VSS
B3	PWM_OUT1	J16	AVSS_VDAC_0	U22	VI0_DAT4
B4	USB2_PWREN1	J18	DVDD33	V1	DDR_CKE
B5	USB2_PWREN0	J19	VI3_DAT4	V2	DDR_BA1
B6	USB2_DM0	J20	VI3_DAT5	V3	VSS
B7	USB2_DP1	J21	VI3_DAT2	V4	DDR_BA2
B8	RGMII_RXD0	J22	VI3_DAT3	V5	DDR_A11
B9	RGMII_RXD2	J23	VSS	V6	VSS
B10	RGMII_RXD3	K2	DDR_DQ0	V7	VDDIO_DDR
B11	RGMII_TXCKOUT	K3	DDR_DQ9	V8	VSS
B12	RGMII_TXD1	K4	VSS	V9	VDDIO_DDR
B13	RGMII_TXD2	K5	DDR_DQ7	V10	VDDIO_DDR
B14	VSS	K6	VDDIO_DDR	V11	VSS

Position	Pin Name	Position	Pin Name	Position	Pin Name
B15	HDMI_TX2N	K9	VSS	V12	VDDIO_DDR
B16	HDMI_TX1P	K10	DVDD_CORE	V13	DVDD33
B18	HDMI_TXCP	K11	DVDD_CORE	V14	VSS
B19	HDMI_SCL	K12	VSS	V15	AVDD33_VPH_SATA0
B20	VGA_VS	K13	AVSS_HDMITX	V16	AVDD33_VPH_SATA1
B21	AVSS_VDAC	K14	DVSS_VDAC	V17	VSS
B22	VGA_B	K15	DVDD33_VDAC	V18	DVDD33
B23	CVBS_OUT	K18	VSS	V19	I2S1_BCLK_RX
C1	GPIO0_5	K19	VI3_DAT7	V20	VSS
C2	GPIO0_4	K20	VSS	V21	VI0_CLK
C3	GPIO0_0	K21	VI3_DAT6	V22	VI0_DAT6
C4	PWM_OUT0	K22	VI3_CLK	V23	VI0_DAT5
C5	VSS	K23	VSS	W2	DDR_A4
C6	USB2_DP0	L1	DDR_DQS0_P	W3	DDR_A14
C7	AVSS_USB	L2	DDR_DQS0_N	W4	DDR_A6
C8	VSS	L3	VSS	W5	VSS
C9	RGMII_RXD1	L4	DDR_DM0	W6	DDR_DQ23
C10	VSS	L5	DDR_DQ8	W7	DDR_DQ19
C11	VSS	L6	VSS	W8	VSS
C12	VSS	L9	VSS	W9	DDR_DQ28
C13	RGMII_TXD3	L10	DVDD_CORE	W10	DDR_DQ18
C14	AVSS_HDMITX	L11	DVDD_CORE	W11	DDR_DQ16
C15	HDMI_TX2P	L12	DVDD_CORE	W12	VDDIO_DDR
C16	AVSS_HDMITX	L13	VSS	W13	UART2_RXD
C17	HDMI_TX0N	L14	AVSS_PLL	W14	SATA_LED_N0
C18	AVSS_HDMITX	L15	AVDD33_PLL	W15	VSS
C19	HDMI_SDA	L18	VSS	W16	VSS
C20	VGA_HS	L19	VI2_DAT3	W17	VSS
C21	VSS	L20	VI2_DAT2	W18	VSS
C22	AVSS_VDAC	L21	VI2_DAT0	W19	SATA_REXT
C23	VDAC_REXT	L22	VI2_DAT1	W20	I2S1_SD_RX

Position	Pin Name	Position	Pin Name	Position	Pin Name
D1	UART0_RXD	M2	DDR_DQS1_P	W21	I2S1_WS_RX
D2	GPIO0_7	M3	DDR_DQS1_N	W22	VSS
D3	GPIO0_6	M4	VSS	W23	VI0_DAT7
D4	VSS	M5	VSS	Y1	DDR_RAS_N
D5	VSS	M6	VDDIO_DDR	Y2	VSS
D6	VSS	M9	VSS	Y3	VSS
D7	AVSS_USB	M10	VSS	Y4	DDR_A1
D8	AVCC11_USB	M11	DVDD_CORE	Y5	DDR_A10
D9	VSS	M12	DVDD_CORE	Y6	DDR_DQ21
D10	RGMII_RXDV	M13	VSS	Y7	VSS
D11	RGMII_COL	M14	AVSS_PLL	Y8	DDR_DM2
D12	RGMII_CRS	M15	AVDD11_PLL	Y9	DDR_DQ30
D13	EPHY_RSTN	M18	DVDD3318_VI	Y10	DDR_DQ22
D14	MDIO	M19	VI2_DAT4	Y11	DDR_DM3
D15	AVSS_HDMITX	M20	VI2_DAT5	Y12	VSS
D16	AVSS_HDMITX	M21	VI2_CLK	Y13	JTAG_TMS
D17	HDMI_TX0P	M22	VSS	Y14	UART2_TXD
D18	AVSS_HDMITX	M23	VI_ADC_REFCLK0	Y15	SATA_LED_N1
D19	HDMI_HOTPLUG	N3	DDR_DQ12	Y16	SATA_TX0P
D20	AVSS_RTC	N4	VSS	Y17	VSS
D21	RTC_XIN	N5	VDDIO_DDR	Y18	SATA_TX1P
D22	RTC_XOUT	N6	VDDIO_DDR	Y19	POR_ENABLE
E2	UART0_TXD	N7	VDDIO_DDR	Y20	TEST_MODE
E3	UART0_CTSN	N9	AVDD_DDRPLL_0	Y21	I2S2_WS_TX
E4	VSS	N10	VSS	Y22	I2S2_BCLK_TX
E5	DVDD_CPU	N11	DVDD_CORE	AA1	DDR_CAS_N
E6	DVDD_CPU	N12	DVDD_CORE	AA2	DDR_A8
E7	VSS	N13	VSS	AA3	DDR_BA0
E8	AVDD33_USB	N14	VSS	AA4	DDR_A12
E9	AVSS_USB	N15	AVDD_EFUSE	AA5	DDR_ODT
E10	VSS	N18	DVDD3318_VI	AA6	DDR_DQ20

Position	Pin Name	Position	Pin Name	Position	Pin Name
E11	RGMII_RXER	N19	VI2_DAT6	AA7	DDR_DQ24
E12	RGMII_TXEN	N20	VI2_DAT7	AA8	DDR_DQS3_P
E13	VSS	N21	VSS	AA9	VSS
E14	EPHY_CLK	N22	VI1_DAT1	AA10	DDR_DQ27
E15	RGMII_TXER	N23	VI1_DAT0	AA11	DDR_DQ29
E16	AVSS_HDMITX	P1	DDR_DQ10	AA12	JTAG_EN
E17	AVDD33_HDMITX	P2	VSS	AA13	JTAG_TDI
E18	AVSS_HDMITX	P3	DDR_DQ1	AA14	IR_IN
E19	AVDD_BAT	P4	DDR_DQ14	AA15	VSS
E20	AVSS_RTC	P5	VDDIO_DDR	AA16	SATA_TX0M
E21	VSS	P6	VDDIO_DDR_CK	AA17	VSS
E22	XOUT	P7	VDDIO_DDR	AA18	SATA_TX1M
E23	XIN	P9	VSS	AA19	VSS
F1	UART1_TXD	P10	VSS	AA20	SFC_CLK
F2	UART1_RXD	P11	DVDD_CORE	AA21	SFC_CS1N
F3	UART0_RTSN	P12	DVDD_CORE	AA22	VSS
F4	VSS	P13	VSS	AA23	I2S2_SD_TX
F5	DVDD_CPU	P14	VSS	AB1	DDR_A0
F6	DVDD_CPU	P15	VSS	AB2	DDR_A13
F9	VSS	P18	VSS	AB3	DDR_CS_N
F10	DVDD33	P19	VI1_DAT5	AB4	VSS
F11	VSS	P20	VI1_DAT4	AB5	VSS
F12	VSS	P21	VI1_DAT2	AB6	DDR_DQ26
F13	DVDDIO_RGMII	P22	VI1_DAT3	AB7	VSS
F14	VSS	R1	VSS	AB8	DDR_DQS3_N
F15	VSS	R2	DDR_DQ3	AB9	DDR_DQS2_N
F16	AVSS_HDMITX	R3	DDR_DQ5	AB10	DDR_DQ25
F17	AVSS_HDMITX	R4	DDR_A3	AB11	VSS
F18	VSS	R5	DDR_A5	AB12	JTAG_TDO
F19	VSS	R6	VSS	AB13	JTAG_TRSTN
F20	I2C_SCL	R9	VSS	AB15	SATA_RX0P

Position	Pin Name	Position	Pin Name	Position	Pin Name
F21	VSS	R10	VSS	AB17	SATA_RX1P
F22	SPI_CSN0	R11	VSS	AB19	WDG_RSTN
F23	SPI_CSN1	R12	VSS	AB20	SFC_CS0N
G2	VSS	R13	VSS	AB21	SFC_DIO
G3	VSS	R14	VSS	AB22	SFC_DOI
G4	VSS	R15	VSS	AB23	SFC_WP_IO2
G5	VSS	R18	VSS	AC1	VSS
G6	VSS	R19	VI1_DAT7	AC2	DDR_RESET_N
G18	AVSS_RTC	R20	VI1_DAT6	AC3	VSS
G19	I2C_SDA	R21	VSS	AC5	DDR_DQ17
G20	SPI_SDI	R22	VI1_CLK	AC6	VSS
G21	SPI_SCLK	R23	VI0_DAT0	AC8	VSS
G22	VSS	T2	VSS	AC9	DDR_DQS2_P
G23	VI_ADC_REFCLK 1	T3	DDR_A9	AC11	DDR_DQ31
H1	VSS	T4	DDR_A2	AC12	VSS
H2	DDR_DQ11	T5	DDR_A7	AC13	JTAG_TCK
H3	DDR_DM1	T6	VDDIO_DDR	AC15	SATA_RX0M
H4	DDR_DQ2	T9	AVDD_DDRPLL_1	AC17	SATA_RX1M
H5	DDR_DQ6	T10	AVDD_DDRPLL_2	AC19	VSS
H6	DDR_ZQ	T11	VSS	AC20	RSTN
H8	DVDD_CPU	T12	AVDD_VP_SATA0	AC22	SFC_HOLD_IO3
H9	DVDD_CPU	T13	AVDD_VPTX_SAT A0	AC23	VSS
H18	AVDD33_RTC	T14	AVDD_VP_SATA1		

2.2 Pin Description

2.2.1 Pin Types

Table 2-4 describes the I/O pin types.

Table 2-4 I/O types

I/O	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with a Schmitt trigger
I_{SPD}	Input signal with a Schmitt trigger, internal pull-down
I_{SPU}	Input signal with a Schmitt trigger, internal pull-up
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (input/output) signal
I_{PD}/O	Bidirectional signal, input pull-down
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPU}/O	Bidirectional signal with a Schmitt trigger, input pull-up
I_{SPD}/O	Bidirectional signal with Schmitt trigger, input pull-down
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD
I_S/O	Bidirectional signal, input with a Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with a Schmitt trigger and output OD
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground (GND)

2.2.2 Pin Details

NOTE

- The drive current of pins with the symbol of "CFG" in the **Drive Current (mV)** column can be configured in the pin drive capability register. When the CFG pin is used as the output pin, the default drive current is determined by the default value of the pin drive capability register.
- Pins with the symbol of "5 V tol" in the **Voltage (V)** column support the 5 V tolerance.

VDAC Pins

Table 2-5 describes video digital-to-analog converter (VDAC) pins.

Table 2-5 VDAC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
B23	CVBS_OUT	O	-	-	CVBS channel output
C23	VDAC_REXT	I/O	-	-	VDAC reference current. A 12 kΩ resistor is recommended.
B22	VGA_B	O	-	-	B channel output of the VGA
A22	VGA_G	O	-	-	G channel output of the VGA
A21	VGA_R	O	-	-	R channel output of the VGA
C20	VGA_HS	I/O	CFG	3.3	Function 0: GPIO11_6 General-purpose input/output (GPIO) Function 1: VGA_HS VGA row sync output
B20	VGA_VS	I/O	CFG	3.3	Function 0: GPIO11_3 GPIO Function 1: VGA_VS VGA field sync output

HDMI Pins

Table 2-6 describes high definition multimedia interface (HDMI) pins.

Table 2-6 HDMI pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A19	HDMI_CEC	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO13_5 GPIO Function 1: HDMI_CEC Consumer electronics control (CEC) channel signal of the HDMI
D19	HDMI_HOT PLUG	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO13_4 GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					Function 1: HDMI_HOTPLUG Hot plug detection signal of the HDMI
B19	HDMI_SCL	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO13_7 GPIO Function 1: HDMI_SCL Display data channel (DDC) clock signal of the HDMI
C19	HDMI_SDA	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO13_6 GPIO Function 1: HDMI_SDA DDC data/address signal of the HDMI
C17	HDMI_TX0N	O	-	-	Negative terminal of the serial differential signal of HDMI TX channel 0
D17	HDMI_TX0P	O	-	-	Positive terminal of the serial differential signal of HDMI TX channel 0
A16	HDMI_TX1N	O	-	-	Negative terminal of the serial differential signal of HDMI TX channel 1
B16	HDMI_TX1P	O	-	-	Positive terminal of the serial differential signal of HDMI TX channel 1
B15	HDMI_TX2N	O	-	-	Negative terminal of the serial differential signal of HDMI TX channel 2
C15	HDMI_TX2P	O	-	-	Positive terminal of the serial differential signal of HDMI TX channel 2
A18	HDMI_TXCN	O	-	-	Negative terminal of the HDMI TX differential pixel clock
B18	HDMI_TXCP	O	-	-	Positive terminal of the HDMI TX differential pixel clock

DDR Pins

Table 2-7 describes double data rate (DDR) pins.

Table 2-7 DDR pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AB1	DDR_A0	O	-	1.5/1.35	DDR SDRAM address 0
Y4	DDR_A1	O	-	1.5/1.35	DDR SDRAM address 1
T4	DDR_A2	O	-	1.5/1.35	DDR SDRAM address 2
R4	DDR_A3	O	-	1.5/1.35	DDR SDRAM address 3
W2	DDR_A4	O	-	1.5/1.35	DDR SDRAM address 4
R5	DDR_A5	O	-	1.5/1.35	DDR SDRAM address 5
W4	DDR_A6	O	-	1.5/1.35	DDR SDRAM address 6
T5	DDR_A7	O	-	1.5/1.35	DDR SDRAM address 7
AA2	DDR_A8	O	-	1.5/1.35	DDR SDRAM address 8
T3	DDR_A9	O	-	1.5/1.35	DDR SDRAM address 9
Y5	DDR_A10	O	-	1.5/1.35	DDR SDRAM address 10
V5	DDR_A11	O	-	1.5/1.35	DDR SDRAM address 11
AA4	DDR_A12	O	-	1.5/1.35	DDR SDRAM address 12
AB2	DDR_A13	O	-	1.5/1.35	DDR SDRAM address 13
W3	DDR_A14	O	-	1.5/1.35	DDR SDRAM address 14
AA3	DDR_BA0	O	-	1.5/1.35	Bank address signal 0 of the DDR SDRAM
V2	DDR_BA1	O	-	1.5/1.35	Bank address signal 1 of the DDR SDRAM
V4	DDR_BA2	O	-	1.5/1.35	Bank address signal 2 of the DDR SDRAM
AA1	DDR_CAS_N	O	-	1.5/1.35	Column address select signal of the DDR SDRAM
V1	DDR_CKE	O	-	1.5/1.35	Clock enable signal of the DDR SDRAM

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
U1	DDR_CLK0_N	O	-	1.5/1.35	(Negative) differential clock of the DDR SDRAM
U2	DDR_CLK0_P	O	-	1.5/1.35	(Positive) differential clock of the DDR SDRAM
AB3	DDR_CS_N	O	-	1.5/1.35	Chip select (CS) signal of the DDR SDRAM
L4	DDR_DM0	I/O	-	1.5/1.35	Data mask signal 0 of the DDR SDRAM
H3	DDR_DM1	I/O	-	1.5/1.35	Data mask signal 1 of the DDR SDRAM
Y8	DDR_DM2	I/O	-	1.5/1.35	Data mask signal 2 of the DDR SDRAM
Y11	DDR_DM3	I/O	-	1.5/1.35	Data mask signal 3 of the DDR SDRAM
K2	DDR_DQ0	I/O	-	1.5/1.35	DDR SDRAM data 0
P3	DDR_DQ1	I/O	-	1.5/1.35	DDR SDRAM data 1
H4	DDR_DQ2	I/O	-	1.5/1.35	DDR SDRAM data 2
R2	DDR_DQ3	I/O	-	1.5/1.35	DDR SDRAM data 3
J5	DDR_DQ4	I/O	-	1.5/1.35	DDR SDRAM data 4
R3	DDR_DQ5	I/O	-	1.5/1.35	DDR SDRAM data 5
H5	DDR_DQ6	I/O	-	1.5/1.35	DDR SDRAM data 6
K5	DDR_DQ7	I/O	-	1.5/1.35	DDR SDRAM data 7
L5	DDR_DQ8	I/O	-	1.5/1.35	DDR SDRAM data 8
K3	DDR_DQ9	I/O	-	1.5/1.35	DDR SDRAM data 9
P1	DDR_DQ10	I/O	-	1.5/1.35	DDR SDRAM data 10
H2	DDR_DQ11	I/O	-	1.5/1.35	DDR SDRAM data 11
N3	DDR_DQ12	I/O	-	1.5/1.35	DDR SDRAM data 12
J3	DDR_DQ13	I/O	-	1.5/1.35	DDR SDRAM data 13
P4	DDR_DQ14	I/O	-	1.5/1.35	DDR SDRAM data 14

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
J1	DDR_DQ15	I/O	-	1.5/1.35	DDR SDRAM data 15
W11	DDR_DQ16	I/O	-	1.5/1.35	DDR SDRAM data 16
AC5	DDR_DQ17	I/O	-	1.5/1.35	DDR SDRAM data 17
W10	DDR_DQ18	I/O	-	1.5/1.35	DDR SDRAM data 18
W7	DDR_DQ19	I/O	-	1.5/1.35	DDR SDRAM data 19
AA6	DDR_DQ20	I/O	-	1.5/1.35	DDR SDRAM data 20
Y6	DDR_DQ21	I/O	-	1.5/1.35	DDR SDRAM data 21
Y10	DDR_DQ22	I/O	-	1.5/1.35	DDR SDRAM data 22
W6	DDR_DQ23	I/O	-	1.5/1.35	DDR SDRAM data 23
AA7	DDR_DQ24	I/O	-	1.5/1.35	DDR SDRAM data 24
AB10	DDR_DQ25	I/O	-	1.5/1.35	DDR SDRAM data 25
AB6	DDR_DQ26	I/O	-	1.5/1.35	DDR SDRAM data 26
AA10	DDR_DQ27	I/O	-	1.5/1.35	DDR SDRAM data 27
W9	DDR_DQ28	I/O	-	1.5/1.35	DDR SDRAM data 28
AA11	DDR_DQ29	I/O	-	1.5/1.35	DDR SDRAM data 29
Y9	DDR_DQ30	I/O	-	1.5/1.35	DDR SDRAM data 30
AC11	DDR_DQ31	I/O	-	1.5/1.35	DDR SDRAM data 31
L2	DDR_DQS0_N	I/O	-	1.5/1.35	(Negative) data strobe (DQS) signal 0 of the DDR SDRAM, corresponding to DDR_DQ0−DDR_DQ7
L1	DDR_DQS0_P	I/O	-	1.5/1.35	(Positive) data strobe (DQS) signal 0 of the DDR SDRAM, corresponding to DDR_DQ0−DDR_DQ7
M3	DDR_DQS1_N	I/O	-	1.5/1.35	(Negative) data strobe (DQS) signal 1 of the DDR SDRAM, corresponding to DDR_DQ8−DDR_DQ15

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
M2	DDR_DQS1_P	I/O	-	1.5/1.35	(Positive) data strobe (DQS) signal 1 of the DDR SDRAM, corresponding to DDR_DQ8−DDR_DQ15
AB9	DDR_DQS2_N	I/O	-	1.5/1.35	(Negative) data strobe (DQS) signal 2 of the DDR SDRAM, corresponding to DDR_DQ16−DDR_DQ23
AC9	DDR_DQS2_P	I/O	-	1.5/1.35	(Positive) data strobe (DQS) signal 2 of the DDR SDRAM, corresponding to DDR_DQ16−DDR_DQ23
AB8	DDR_DQS3_N	I/O	-	1.5/1.35	(Negative) data strobe (DQS) signal 3 of the DDR SDRAM, corresponding to DDR_DQ24−DDR_DQ31
AA8	DDR_DQS3_P	I/O	-	1.5/1.35	(Positive) data strobe (DQS) signal 3 of the DDR SDRAM, corresponding to DDR_DQ24−DDR_DQ31
AA5	DDR_ODT	I/O	-	1.5/1.35	Matched termination resistor of the DDR SDRAM
Y1	DDR_RAS_N	O	-	1.5/1.35	Row address select signal of the DDR SDRAM
AC2	DDR_RESET_N	O	-	1.5/1.35	Reset signal of the DDR SDRAM
U5	DDR_WE_N	O	-	1.5/1.35	Write enable signal of the DDR SDRAM
H6	DDR_ZQ	I/O	-	1.5/1.35	ZQ calibration signal of the DDR SDRAM

RGMII Pins

The Hi3521A Ethernet port supports the reduced gigabit media independent interface (RGMII), reduced media independent interface (RMII), and media independent interface (MII) modes. Table 2-8 describes the functions of RGMII pins in each mode.

Table 2-8 Functions of RGMII pins in three modes

Pin Name	RGMII Mode	MII Mode	RMII Mode
RGMII_COL	-	Conflict detection	-

Pin Name	RGMII Mode	MII Mode	RMII Mode
RGMII_CRS	-	Carrier detection	-
RGMII_RXCK	RX clock	RX clock	-
RGMII_RXD0	RX data 0	RX data 0	RX data 0
RGMII_RXD1	RX data 1	RX data 1	RX data 1
RGMII_RXD2	RX data 2	RX data 2	-
RGMII_RXD3	RX data 3	RX data 3	-
RGMII_RXDV	RX data validity	RX data validity	RX data validity/carrier detection
RGMII_RXER	-	RX error indicator	RX error indicator
RGMII_TXCKOUT	TX clock	TX clock	Reference clock
RGMII_TXD0	TX data 0	TX data 0	TX data 0
RGMII_TXD1	TX data 1	TX data 1	TX data 1
RGMII_TXD2	TX data 2	TX data 2	-
RGMII_TXD3	TX data 3	TX data 3	-
RGMII_TXEN	TX data enable	TX data enable	TX data enable
RGMII_TXER	-	TX error indicator	-

Table 2-9 describes RGMII pins.

Table 2-9 RGMII pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
E14	EPHY_CLK	I/O	CFG	3.3/2.5	Function 0: GPIO6_6 GPIO Function 1: EPHY_CLK Working clock of the Ethernet PHY
D13	EPHY_RSTN	I/O	CFG	3.3/2.5	Function 0: GPIO6_4 GPIO Function 1: EPHY_RSTN Reset signal of the Ethernet PHY, active low

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
D11	RGMII_COL	I_{PD}/O	CFG	3.3/2.5	Function 0: GPIO8_5 GPIO Function 1: RGMII_COL Conflict detection signal in MII mode
D12	RGMII_CRS	I_{PD}/O	CFG	3.3/2.5	Function 0: GPIO8_4 GPIO Function 1: RGMII_CRS Carrier sense signal in MII mode
A10	RGMII_RXCK	I/O	CFG	3.3/2.5	Function 0: GPIO7_5 GPIO Function 1: RGMII_RXCK RX clock in RGMII or MII mode
B8	RGMII_RXD0	I/O	CFG	3.3/2.5	Function 0: GPIO7_4 GPIO Function 1: RGMII_RXD0 RX data 0 in RGMII, MII, or RMII mode
C9	RGMII_RXD1	I/O	CFG	3.3/2.5	Function 0: GPIO7_3 GPIO Function 1: RGMII_RXD1 RX data 1 in RGMII, MII, or RMII mode
B9	RGMII_RXD2	I/O	CFG	3.3/2.5	Function 0: GPIO7_2 GPIO Function 1: RGMII_RXD2 RX data 2 in RGMII or MII mode
B10	RGMII_RXD3	I/O	CFG	3.3/2.5	Function 0: GPIO7_1 GPIO Function 1: RGMII_RXD3 RX data 3 in RGMII or MII mode
D10	RGMII_RXDV	I/O	CFG	3.3/2.5	Function 0: GPIO7_0 GPIO Function 1: RGMII_RXDV

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					RX data validity signal in RGMII or MII mode RX data validity and carrier detection signals in RMII mode
E11	RGMII_RXER	I_{PD}/O	CFG	3.3/2.5	Function 0: GPIO8_6 GPIO Function 1: RGMII_RXER RX error signal in MII or RMII mode
B11	RGMII_TXCKOUT	I/O	CFG	3.3/2.5	Function 0: GPIO8_3 GPIO Function 1: RGMII_TXCKOUT TX clock (active on both edges) in RGMII gigabit mode Function 2: MII_TXCK TX clock in MII mode Function 3: RMII_CLK Reference clock in RMII mode
A12	RGMII_TXD0	I/O	CFG	3.3/2.5	Function 0: GPIO8_2 GPIO Function 1: RGMII_TXD0 TX data 0 in RGMII, MII, or RMII mode
B12	RGMII_TXD1	I/O	CFG	3.3/2.5	Function 0: GPIO8_1 GPIO Function 1: RGMII_TXD1 TX data 1 in RGMII, MII, or RMII mode
B13	RGMII_TXD2	I/O	CFG	3.3/2.5	Function 0: GPIO8_0 GPIO Function 1: RGMII_TXD2 TX data 2 in RGMII or MII mode
C13	RGMII_TXD3	I/O	CFG	3.3/2.5	Function 0: GPIO7_7 GPIO Function 1: RGMII_TXD3 TX data 3 in RGMII or MII

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					mode
E12	RGMII_TXEN	I/O	CFG	3.3/2.5	Function 0: GPIO7_6 GPIO Function 1: RGMII_TXEN TX data validity signal in RGMII, MII, or RMII mode
E15	RGMII_TXER	I_{PD}/O	CFG	3.3/2.5	Function 0: RGMII_TXER TX error signal in MII mode Function 1: SFC_DEVICE_MODE Serial peripheral interface (SPI) flash type select (hardware multiplexing, valid during reset) 0: SPI NOR flash 1: SPI NAND flash

MDIO Pins

Table 2-10 describes management data input/output (MDIO) pins.

Table 2-10 MDIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A14	MDCK	I_{PD}/O	CFG	3.3/2.5	Function 0: GPIO10_0 GPIO Function 1: MDCK MIDO interface clock output Function 2: BOOTROM_SEL BOOTROM boot 0: boot from the SPI flash 1: boot from the BOOTROM
D14	MDIO	I/O	CFG	3.3/2.5	Function 0: GPIO10_1 GPIO Function 1: MDIO Input/Output signal of the MDIO interface

I²C Pins

Table 2-11 describes inter-integrated circuit (I^2C) pins.

Table 2-11 I^2C pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
F20	I2C_SCL	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO12_7 GPIO Function 1: I2C_SCL I^2C bus clock
G19	I2C_SDA	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO12_6 GPIO Function 1: I2C_SDA I^2C bus data/address

IR Pins

Table 2-12 describes the infrared (IR) pin.

Table 2-12 IR pin

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AA14	IR_IN	I_{PU}/O	CFG	3.3 (5 V tol)	Function 0: GPIO10_2 GPIO Function 1: IR_IN IR input signal

PWM Pins

Table 2-13 describes pulse-width modulation (PWM) pins.

Table 2-13 PWM pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
C4	PWM_OUT0	I/O	CFG	DVDDIO_33	Function 0: PWM_OUT0 PWM output 0 Function 1: GPIO5_5 GPIO
B3	PWM_OUT1	I/O	CFG	DVDDIO_33	Function 0: PWM_OUT1 PWM output 1 Function 1: GPIO5_6 GPIO

SFC Pins

Table 2-14 describes SFC pins.

Table 2-14 SFC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AA20	SFC_CLK	I_{PD}/O	CFG	3.3/1.8	Function 0: SFC_CLK Clock of the SPI NAND/NOR flash Function 1: SFC_BOOT_MODE Boot address mode of the SPI NOR flash when SFC_DEVICE_MODE is 0 0: 3-byte address mode 1: 4-byte address mode Boot mode of the SPI NAND flash when SFC_DEVICE_MODE is 1 0: 1-wire boot mode 1: 4-wire boot mode
AB20	SFC_CS0N	I/O	CFG	3.3/1.8	CS0 signal of the SPI NAND/NOR flash, active low
AA21	SFC_CS1N	I/O	CFG	3.3/1.8	CS1 signal of the SPI NAND/NOR flash, active low
AB21	SFC_DIO	I/O	CFG	3.3/1.8	Function 0: SFC_DIO Data output signal in standard SPI

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode Function 1: GPIO11_0 GPIO
AB22	SFC_DOI	I/O	CFG	3.3/1.8	Function 0: SFC_DOI Data input signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode Function 1: GPIO11_2 GPIO
AC22	SFC_HOLD_IO3	I/O	CFG	3.3/1.8	Hold function in standard SPI mode, active low Hold function in dual-SPI mode, active low Data I/O signal in quad-SPI mode
AB23	SFC_WP_IO2	I/O	CFG	3.3/1.8	Function 0: SFC_WP_IO2 Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal in quad-SPI mode Function 1: GPIO11_1 GPIO

UART Pins

Table 2-15 describes universal asynchronous receiver transmitter (UART) pins.

Table 2-15 UART pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
E3	UART0_CTSN	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: UART0_CTSN UART0 clear-to-send (CTS) signal, active low Function 1: GPIO6_2

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					GPIO
F3	UART0_ RTSN	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: UART0_RTSN UART0 request to send (RTS) signal, active low Function 1: GPIO6_3 GPIO
D1	UART0_ RXD	I_{PU} /O	CFG	DVDDIO_33 (5 V tol)	Function 0: UART0_RXD UART0 RX data Function 1: GPIO10_7 GPIO
E2	UART0_T XD	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: UART0_TXD UART0 TX data Function 1: GPIO12_5 GPIO
F2	UART1_ RXD	I_{PU} /O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO6_5 GPIO Function 1: UART1_RXD UART1 RX data
F1	UART1_T XD	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO6_7 GPIO Function 1: UART1_TXD UART1 TX data
W13	UART2_ RXD	I_{PU} /O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO11_4 GPIO Function 1: UART2_RXD UART2 RX data
Y14	UART2_T XD	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO11_5 GPIO Function 1: UART2_TXD UART2 TX data

SATA Pins

Table 2-16 describes serial advanced technology attachment (SATA) pins.

Table 2-16 SATA pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W14	SATA_LED_N0	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO10_3 GPIO Function 1: SATA_LED_N0 Light emitting diode (LED) indicator of SATA port 0, active low
Y15	SATA_LED_N1	I/O	CFG	3.3 (5 V tol)	Function 0: GPIO10_4 GPIO Function 1: SATA_LED_N1 LED indicator of SATA port 1, active low
AC15	SATA_RX0M	I	-	-	Negative terminal of the RX differential signal of SATA port 0
AB15	SATA_RX0P	I	-	-	Positive terminal of the RX differential signal of SATA port 0
AA16	SATA_TX0M	O	-	-	Negative terminal of the TX differential signal of SATA port 0
Y16	SATA_TX0P	O	-	-	Positive terminal of the TX differential signal of SATA port 0
AC17	SATA_RX1M	I	-	-	Negative terminal of the RX differential signal of SATA port 1
AB17	SATA_RX1P	I	-	-	Positive terminal of the RX differential signal of SATA port 1
AA18	SATA_TX1M	O	-	-	Negative terminal of the TX differential signal of SATA port 1
Y18	SATA_TX1P	O	-	-	Positive terminal of the TX differential signal of SATA port 1
W19	SATA_REXT	I/O			External resistor of the SATA port. A 200±1% resistor is recommended.

USB 2.0 Pins

Table 2-17 describes USB 2.0 pins.

Table 2-17 USB 2.0 pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
B6	USB2_DM0	I/O	-	-	Negative terminal of the data signal of USB 2.0 port 0
A7	USB2_DM1	I/O	-	-	Negative terminal of the data signal of USB 2.0 port 1
C6	USB2_DP0	I/O	-	-	Positive terminal of the data signal of USB 2.0 port 0
B7	USB2_DP1	I/O	-	-	Positive terminal of the data signal of USB 2.0 port 1
A5	USB2_OVRCUR0	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO13_0 GPIO Function 1: SB2_OVRCUR0 Overcurrent indicator of USB port 0, configurable level, and active high by default
A4	USB2_OVRCUR1	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO13_2 GPIO Function 1: USB2_OVRCUR1 Overcurrent indicator of USB port 1, configurable level, and active high by default
B5	USB2_PWREN0	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO13_1 GPIO Function 1: USB2_PWREN0 Power control output signal of USB port 0, configurable level, and active low by default

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
B4	USB2_PWREN1	I/O	CFG	DVDDIO_33 (5 V tol)	Function 0: GPIO13_3 GPIO Function 1: USB2_PWREN1 Power control output signal of USB port 1, configurable level, and active low by default
A8	USB2_REXT	I/O	-	3.3	External reference resistor of USB 2.0 port. A 135±1% resistor is recommended.

VI Pins

Table 2-18 describes video input (VI) pins.

Table 2-18 VI pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
M23	VI_ADC_REFCLK0	I/O	CFG	3.3/1.8	Function 0: GPIO6_0 GPIO Function 1: VI_ADC_REFCLK0 Video analog-to-digital converter (VADC) working clock 0 Function 2: VI1_CLK VI1 clock signal
G23	VI_ADC_REFCLK1	I/O	CFG	3.3/1.8	Function 0: GPIO6_1 GPIO Function 1: VI_ADC_REFCLK1 VADC working clock 1 Function 2: VI3_CLK VI3 clock signal

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V21	VI0_CLK	I/O	CFG	3.3/1.8	Function 0: GPIO5_7 GPIO Function 1: VI0_CLK VI0 clock signal Function 2: VI_ADC_REFCLK0 VADC working clock 0
R23	VI0_DAT0	I/O	CFG	3.3/1.8	Function 0: GPIO1_7 GPIO Function 1: VI0_DAT0 VI0 data input
T23	VI0_DAT1	I/O	CFG	3.3/1.8	Function 0: GPIO1_6 GPIO Function 1: VI0_DAT1 VI0 data input
T22	VI0_DAT2	I/O	CFG	3.3/1.8	Function 0: GPIO1_5 GPIO Function 1: VI0_DAT2 VI0 data input
T21	VI0_DAT3	I/O	CFG	3.3/1.8	Function 0: GPIO1_4 GPIO Function 1: VI0_DAT3 VI0 data input
U22	VI0_DAT4	I/O	CFG	3.3/1.8	Function 0: GPIO1_3 GPIO Function 1: VI0_DAT4 VI0 data input
V23	VI0_DAT5	I/O	CFG	3.3/1.8	Function 0: GPIO1_2 GPIO Function 1: VI0_DAT5 VI0 data input

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
V22	VI0_DAT6	I/O	CFG	3.3/1.8	Function 0: GPIO1_1 GPIO Function 1: VI0_DAT6 VI0 data input
W23	VI0_DAT7	I/O	CFG	3.3/1.8	Function 0: GPIO1_0 GPIO Function 1: VI0_DAT7 VI0 data input
R22	VI1_CLK	I/O	CFG	3.3/1.8	Function 0: GPIO10_6 GPIO Function 1: VI1_CLK VI1 clock signal Function 2: VI0_CLK VI0 clock signal
N23	VI1_DAT0	I/O	CFG	3.3/1.8	Function 0: GPIO2_7 GPIO Function 1: VI1_DAT0 VI1 data input
N22	VI1_DAT1	I/O	CFG	3.3/1.8	Function 0: GPIO2_6 GPIO Function 1: VI1_DAT1 VI1 data input
P21	VI1_DAT2	I/O	CFG	3.3/1.8	Function 0: GPIO2_5 GPIO Function 1: VI1_DAT2 VI1 data input
P22	VI1_DAT3	I/O	CFG	3.3/1.8	Function 0: GPIO2_4 GPIO Function 1: VI1_DAT3 VI1 data input

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
P20	VI1_DAT4	I/O	CFG	3.3/1.8	Function 0: GPIO2_3 GPIO Function 1: VI1_DAT4 VI1 data input
P19	VI1_DAT5	I/O	CFG	3.3/1.8	Function 0: GPIO2_2 GPIO Function 1: VI1_DAT5 VI1 data input
R20	VI1_DAT6	I/O	CFG	3.3/1.8	Function 0: GPIO2_1 GPIO Function 1: VI1_DAT6 VI1 data input
R19	VI1_DAT7	I/O	CFG	3.3/1.8	Function 0: GPIO2_0 GPIO Function 1: VI1_DAT7 VI1 data input
M21	VI2_CLK	I/O	CFG	3.3/1.8	Function 0: GPIO11_7 GPIO Function 1: VI2_CLK VI2 clock signal Function 2: VI_ADC_REFCLK1 VADC working clock 1
L21	VI2_DAT0	I/O	CFG	3.3/1.8	Function 0: GPIO3_7 GPIO Function 1: VI2_DAT0 VI2 data input
L22	VI2_DAT1	I/O	CFG	3.3/1.8	Function 0: GPIO3_6 GPIO Function 1: VI2_DAT1

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					VI2 data input
L20	VI2_DAT2	I/O	CFG	3.3/1.8	Function 0: GPIO3_5 GPIO Function 1: VI2_DAT2 VI2 data input
L19	VI2_DAT3	I/O	CFG	3.3/1.8	Function 0: GPIO3_4 GPIO Function 1: VI2_DAT3 VI2 data input
M19	VI2_DAT4	I/O	CFG	3.3/1.8	Function 0: GPIO3_3 GPIO Function 1: VI2_DAT4 VI2 data input
M20	VI2_DAT5	I/O	CFG	3.3/1.8	Function 0: GPIO3_2 GPIO Function 1: VI2_DAT5 VI2 data input
N19	VI2_DAT6	I/O	CFG	3.3/1.8	Function 0: GPIO3_1 GPIO Function 1: VI2_DAT6 VI2 data input
N20	VI2_DAT7	I/O	CFG	3.3/1.8	Function 0: GPIO3_0 GPIO Function 1: VI2_DAT7 VI2 data input
K22	VI3_CLK	I/O	CFG	3.3/1.8	Function 0: GPIO10_5 GPIO Function 1: VI3_CLK VI3 clock signal Function 2:

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					VI2_CLK VI2 clock signal
H21	VI3_DAT0	I/O	CFG	3.3/1.8	Function 0: GPIO4_7 GPIO Function 1: VI3_DAT0 VI3 data input
H22	VI3_DAT1	I/O	CFG	3.3/1.8	Function 0: GPIO4_6 GPIO Function 1: VI3_DAT1 VI3 data input
J21	VI3_DAT2	I/O	CFG	3.3/1.8	Function 0: GPIO4_5 GPIO Function 1: VI3_DAT2 VI3 data input
J22	VI3_DAT3	I/O	CFG	3.3/1.8	Function 0: GPIO4_4 GPIO Function 1: VI3_DAT3 VI3 data input
J19	VI3_DAT4	I/O	CFG	3.3/1.8	Function 0: GPIO4_3 GPIO Function 1: VI3_DAT4 VI3 data input
J20	VI3_DAT5	I/O	CFG	3.3/1.8	Function 0: GPIO4_2 GPIO Function 1: VI3_DAT5 VI3 data input
K21	VI3_DAT6	I/O	CFG	3.3/1.8	Function 0: GPIO4_1 GPIO Function 1: VI3_DAT6 VI3 data input

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
K19	VI3_DAT7	I/O	CFG	3.3/1.8	Function 0: GPIO4_0 GPIO Function 1: VI3_DAT7 VI3 data input

I²S Pins

Table 2-19 describes inter-IC sound (I^2S) pins.

Table 2-19 I^2S pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
T19	I2S0_BCLK_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_0 GPIO Function 1: I2S0_BCLK_RX RX clock of the I^2S0/PCM0 interface
U19	I2S0_SD_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_2 GPIO Function 1: I2S0_SD_RX Data input of the I^2S0/PCM0 interface
U20	I2S0_WS_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_1 GPIO Function 1: I2S0_WS_RX I^2S0 RX audio channel select signal or PCM0 RX frame sync signal
V19	I2S1_BCLK_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_3 GPIO Function 1: I2S1_BCLK_RX RX clock of the I2S1/PCM1 interface Function 2: I2S2_MCLK Main clock of the I^2S2 or PCM2 interface. It can act as the working clock of the audio CODEC.

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
W20	I2S1_SD_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_5 GPIO Function 1: I2S1_SD_RX Data input of the I^{2}S1 or PCM1 interface
W21	I2S1_WS_RX	I/O	CFG	3.3/1.8	Function 0: GPIO9_4 GPIO Function 1: I2S1_WS_RX I^{2}S1 RX audio channel select signal or PCM1 RX frame sync signal
Y22	I2S2_BCLK_TX	I/O	CFG	3.3/1.8	Function 0: GPIO9_6 GPIO Function 1: I2S2_BCLK_TX TX clock of the I^{2}S2/PCM2 interface
AA23	I2S2_SD_TX	I/O	CFG	3.3/1.8	Function 0: GPIO5_4 GPIO Function 1: I2S2_SD_TX TX data output of the I^{2}S2 or PCM2 interface
Y21	I2S2_WS_TX	I/O	CFG	3.3/1.8	Function 0: GPIO9_7 GPIO Function 1: I2S2_WS_TX I^{2}S2 TX audio channel select signal or PCM2 TX frame sync signal

SPI Pins

Table 2-20 describes SPI pins.

Table 2-20 SPI pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
F22	SPI_CSN0	I/O	CFG	3.3/1.8	Function 0: GPIO5_3 GPIO Function1: SPI_CSN0

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
					SPI CS 0 output
F23	SPI_CSN1	I/O	CFG	3.3/1.8	Function 0: GPIO8_7 GPIO Function 1: SPI_CSN1 SPI CS 1 output
G21	SPI_SCLK	I/O	CFG	3.3/1.8	Function 0: TEST_CLK Output of the main test clock Function 1: SPI_SCLK SPI clock signal Function 2: GPIO5_0 GPIO
G20	SPI_SDI	I/O	CFG	3.3/1.8	Function 0: GPIO5_2 GPIO Function 1: SPI_SDI SPI data input
H20	SPI_SDO	I/O	CFG	3.3/1.8	Function 0: GPIO5_1 GPIO Function 1: SPI_SDO SPI data output

OSC Pins

Table 2-21 describes oscillator (OSC) pins.

Table 2-21 OSC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
E23	XIN	CIN	-	3.3	24 MHz crystal input
E22	XOUT	COUT	-	3.3	24 MHz crystal drive output

RTC Pins

Table 2-22 describes real-time clock (RTC) pins.

Table 2-22 RTC pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
D21	RTC_XIN	CIN	-	3.3	RTC crystal input
D22	RTC_XOUT	COUT	-	3.3	RTC crystal drive output

SYS Pins

Table 2-23 describes system (SYS) pins.

Table 2-23 SYS pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
Y19	POR_ENABLE	I_{PD}/O	CFG	DVDDIO_33	Power-on reset (POR) enable 0: The internal POR is disabled. 1: The internal POR is enabled.
AC20	RSTN	I_{PU} /O	CFG	DVDDIO_33	System POR signal input, active low
Y20	TEST_MODE	I_{PD}/O	CFG	DVDDIO_33	Mode select 0: function mode 1: test mode
AB19	WDG_RSTN	I/O	CFG	DVDDIO_33	Function 0: WDG_RSTN Watchdog reset output signal, active low and OD output Function 1: SYS_RSTN_OUT System reset output signal, active low

JTAG Pins

Table 2-24 describes Joint Test Action Group (JTAG) pins.

Table 2-24 JTAG pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
AA12	JTAG_EN	I_{PD}/O	CFG	3.3 (5 V tol)	JTAG function enable
AC13	JTAG_TCK	I_{PD}/O	CFG	3.3 (5 V tol)	Function 0: JTAG_TCK JTAG clock input Function 1: GPIO12_1 GPIO
AA13	JTAG_TDI	I_{PU} /O	CFG	3.3 (5 V tol)	Function 0: JTAG_TDI JTAG data input Function 1: GPIO12_4 GPIO
AB12	JTAG_TDO	I/O	CFG	3.3 (5 V tol)	Function 0: JTAG_TDO JTAG data output Function 1: GPIO12_3 GPIO
Y13	JTAG_TMS	I_{PU} /O	CFG	3.3 (5 V tol)	Function 0: JTAG_TMS JTAG mode select input or data output for software trace, controlled by using the CPU Function 1: GPIO12_2 GPIO
AB13	JTAG_TRSTN	I_{PD}/O	CFG	3.3 (5 V tol)	Function 0: JTAG_TRSTN JTAG reset input Function 1: GPIO12_0 GPIO

GPIO Pins

Table 2-25 describes GPIO pins.

Table 2-25 GPIO pins

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
C3	GPIO0_0	I/O	CFG	3.3 (5 V tol)	GPIO

Pin Position	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
A2	GPIO0_1	I/O	CFG	3.3 (5 V tol)	GPIO
B2	GPIO0_2	I/O	CFG	3.3 (5 V tol)	GPIO
B1	GPIO0_3	I/O	CFG	3.3 (5 V tol)	GPIO
C2	GPIO0_4	I/O	CFG	3.3 (5 V tol)	GPIO
C1	GPIO0_5	I/O	CFG	3.3 (5 V tol)	GPIO
D3	GPIO0_6	I/O	CFG	3.3 (5 V tol)	GPIO
D2	GPIO0_7	I/O	CFG	3.3 (5 V tol)	GPIO

Power and GND Pins

Table 2-26 describes power and GND pins.

Table 2-26 Power and GND pins

Pin Position	Pin Name	Type	Voltage (V)	Description
J13	AVCC_HDMITX	P	1.1	HDMI TX core analog power
D8	AVCC_USB	P	1.1	USB core analog power
E19	AVDD_BAT	P	3.3	RTC batter power pin
N9	AVDD_DDRPLL_0	P	3.3	3.3 V DDR3 PLL analog power
T9	AVDD_DDRPLL_1	P	3.3	3.3 V DDR3 PLL analog power
T10	AVDD_DDRPLL_2	P	3.3	3.3 V DDR3 PLL analog power
N15	AVDD_EFUSE	P	2.5	2.5 V eFUSE analog power
M15	AVDD_PLL	P	1.1	PLL core analog power
T12	AVDD_VP_SATA0	P	1.1	SATA core analog power
T14	AVDD_VP_SATA1	P	1.1	SATA core analog

Pin Position	Pin Name	Type	Voltage (V)	Description
				power
T13	AVDD_VPTX_SATA0	P	1.1.	SATA core analog power
T15	AVDD_VPTX_SATA1	P	1.1	SATA core analog power
E17	AVDD33_HDMITX	P	3.3	3.3 V HDMI TX analog power
L15	AVDD33_PLL	P	3.3	3.3 V PLL analog power
H18	AVDD33_RTC	P	3.3	RTC analog power
E8	AVDD33_USB	P	3.3	3.3 V USB analog power
J15	AVDD33_VDAC	P	3.3	3.3 V VDAC RGB analog power
V15	AVDD33_VPH_SATA0	P	3.3	3.3 V SATA analog power
V16	AVDD33_VPH_SATA1	P	3.3	3.3 V SATA analog power
J11, K10, K11, L10, L11, L12, M11, M12, N11, N12, P11, P12	DVDD_CORE	P	1.1	Core power
E5, E6, F5, F6, H8, H9, J8, J9	DVDD_CPU	P	1.1	CPU core power
F10, J18, V13, V18	DVDD33	P	3.3	I/O power
K15	DVDD33_VDAC	P	3.3	3.3 V VDAC digital power
T18	DVDD3318_I2S	P	3.3/1.8	I^2S1/I^2S2 I/O power
U18	DVDD3318_SFC	P	3.3/1.8	SFC I/O power
M18, N18	DVDD3318_VI	P	3.3/1.8	I^2S0/VI/SPI I/O power
F13	DVDDIO_RGMII	P	3.3/2.5	RGMII power
P6	VDDIO_DDR_CK	P	1.5	DDR3 clock interface power
J6, K6, M6, N5, N6, N7, P5, P7,	VDDIO_DDR	P	1.5	DDR3 interface power

Pin Position	Pin Name	Type	Voltage (V)	Description
T6, U6, U7, V7, V9, V10, V12, W12				
C14, C16, C18, D15, D16, D18, E16, E18, F16, F17, K13	AVSS_HDMITX	G	-	HDMI TX analog GND
L14, M14	AVSS_PLL	G	-	PLL analog GND
D20, E20, G18	AVSS_RTC	G	-	RTC analog GND
C7, D7, E9	AVSS_USB	G	-	USB analog GND
J16	AVSS_VDAC_0	G	-	VDAC analog GND
A23, B21, C22, J14	AVSS_VDAC	G	-	VDAC analog GND
K14	DVSS_VDAC	G	-	VDAC digital GND
A1, A11, B14, C5, C8, C10, C11, C12, C21, D4, D5, D6, D9, E4, E7, E10, E13, E21, F4, F9, F11, F12, F14, F15, F18, F19, F21, G2, G3, G4, G5, G6, G22, H1, H19, J2, J4, J10, J12, J23, K4, K9, K12, K18, K20, K23, L3, L6, L9, L13, L18, M4, M5, M9, M10, M13, M22, N4, N10, N13, N14, N21, P2, P9, P10, P13, P14, P15, P18, R1, R6, R9, R10, R11, R12, R13, R14, R15, R18, R21, T2, T11, T20, U3, U4, U21, V3, V6, V8, V11, V14, V17, V20, W5,	VSS	P	-	Digital GND

Pin Position	Pin Name	Type	Voltage (V)	Description
W8, W15, W16, W17, W18, W22, Y2, Y3, Y7, Y12, Y17, AA9, AA15, AA17, AA19, AA22, AB4, AB5, AB7, AB11, AC1, AC3, AC6, AC8, AC12, AC19, AC23				

2.3 Default Reset Status of Digital Pins

Table 2-27 describes the default reset status of digital pins.

Table 2-27 Default reset status of digital pins

Position	Pin Name	Default Status	Remarks
E14	EPHY_CLK	Input	-
D13	EPHY_RSTN	Input	-
C3	GPIO0_0	Input	-
A2	GPIO0_1	Input	-
B2	GPIO0_2	Input	-
B1	GPIO0_3	Input	-
C2	GPIO0_4	Input	-
C1	GPIO0_5	Input	-
D3	GPIO0_6	Input	-
D2	GPIO0_7	Input	-
A19	HDMI_CEC	Input	-
D19	HDMI_HOTPLUG	Input	-

Position	Pin Name	Default Status	Remarks
B19	HDMI_SCL	Input	-
C19	HDMI_SDA	Input	-
F20	I2C_SCL	Input	-
G19	I2C_SDA	Input	-
T19	I2S0_BCLK_RX	Input	-
U19	I2S0_SD_RX	Input	-
U20	I2S0_WS_RX	Input	-
V19	I2S1_BCLK_RX	Input	-
W20	I2S1_SD_RX	Input	-
W21	I2S1_WS_RX	Input	-
Y22	I2S2_BCLK_TX	Input	-
AA23	I2S2_SD_TX	Input	-
Y21	I2S2_WS_TX	Input	-
AA14	IR_IN	Input	Internal pull-up
AA12	JTAG_EN	Input	Internal pull-down
AC13	JTAG_TCK	Input	Internal pull-down
AA13	JTAG_TDI	Input	Internal pull-up
AB12	JTAG_TDO	Output when JTAG_EN is high, and input when JTAG_EN is low	-
Y13	JTAG_TMS	Input	Internal pull-up
AB13	JTAG_TRSTN	Input	Internal pull-down
A14	MDCK	Input	Internal pull-down

Position	Pin Name	Default Status	Remarks
D14	MDIO	Input	-
Y19	POR_ENABLE	Input	Internal pull-down
C4	PWM_OUT0	Low-level output	-
B3	PWM_OUT1	Low-level output	-
D11	RGMII_COL	Input	Internal pull-down
D12	RGMII_CRS	Input	Internal pull-down
A10	RGMII_RXCK	Input	-
B8	RGMII_RXD0	Input	-
C9	RGMII_RXD1	Input	-
B9	RGMII_RXD2	Input	-
B10	RGMII_RXD3	Input	-
D10	RGMII_RXDV	Input	-
E11	RGMII_RXER	Input	Internal pull-down
B11	RGMII_TXCKOUT	Input	--
A12	RGMII_TXD0	Input	-
B12	RGMII_TXD1	Input	-
B13	RGMII_TXD2	Input	-
C13	RGMII_TXD3	Input	-
E12	RGMII_TXEN	Input	-
E15	RGMII_TXER	Low-level output	-
AC20	RSTN	Input	Internal pull-up
W14	SATA_LED_N0	Input	-
Y15	SATA_LED_N1	Input	-
AA20	SFC_CLK	Low-level	-

Position	Pin Name	Default Status	Remarks
		output	
AB20	SFC_CS0N	High-level output	-
AA21	SFC_CS1N	High-level output	-
AB21	SFC_DIO	Input	-
AB22	SFC_DOI	Input	-
AC22	SFC_HOLD_IO3	Input	-
AB23	SFC_WP_IO2	Input	-
F22	SPI_CSN0	Input	-
F23	SPI_CSN1	Input	-
G21	SPI_SCLK	Low-level output	-
G20	SPI_SDI	Input	-
H20	SPI_SDO	Input	-
Y20	TEST_MODE	Input	Internal pull-down
E3	UART0_CTSN	Input	-
F3	UART0_RTSN	High-level output	-
D1	UART0_RXD	Input	Internal pull-up
E2	UART0_TXD	High-level output	-
F2	UART1_RXD	Input	Internal pull-up
F1	UART1_TXD	Input	-
W13	UART2_RXD	Input	Internal pull-up
Y14	UART2_TXD	Input	-
A5	USB2_OVRCUR0	Input	-
A4	USB2_OVRCUR1	Input	-

Position	Pin Name	Default Status	Remarks
B5	USB2_PWREN0	Input	-
B4	USB2_PWREN1	Input	-
C20	VGA_HS	Input	-
B20	VGA_VS	Input	-
M23	VI_ADC_REFCLK0	Input	-
G23	VI_ADC_REFCLK1	Input	-
V21	VI0_CLK	Input	-
R23	VI0_DAT0	Input	-
T23	VI0_DAT1	Input	-
T22	VI0_DAT2	Input	-
T21	VI0_DAT3	Input	-
U22	VI0_DAT4	Input	-
V23	VI0_DAT5	Input	-
V22	VI0_DAT6	Input	-
W23	VI0_DAT7	Input	-
R22	VI1_CLK	Input	-
N23	VI1_DAT0	Input	-
N22	VI1_DAT1	Input	-
P21	VI1_DAT2	Input	-
P22	VI1_DAT3	Input	-
P20	VI1_DAT4	Input	-
P19	VI1_DAT5	Input	-
R20	VI1_DAT6	Input	-
R19	VI1_DAT7	Input	-

Position	Pin Name	Default Status	Remarks
M21	VI2_CLK	Input	-
L21	VI2_DAT0	Input	-
L22	VI2_DAT1	Input	-
L20	VI2_DAT2	Input	-
L19	VI2_DAT3	Input	-
M19	VI2_DAT4	Input	-
M20	VI2_DAT5	Input	-
N19	VI2_DAT6	Input	-
N20	VI2_DAT7	Input	-
K22	VI3_CLK	Input	-
H21	VI3_DAT0	Input	-
H22	VI3_DAT1	Input	-
J21	VI3_DAT2	Input	-
J22	VI3_DAT3	Input	-
J19	VI3_DAT4	Input	-
J20	VI3_DAT5	Input	-
K21	VI3_DAT6	Input	-
K19	VI3_DAT7	Input	-
AB19	WDG_RSTN	OD output	-

2.4 Pin Multiplexing Control Registers

2.4.1 Register Summary

Table 2-28 describes pin multiplexing control registers.

Table 2-28 Summary of pin multiplexing control registers (base address: 0x120F_0000)

Offset Address	Register	Description	Page
0x000	muxctrl_reg0	Multiplexing control register for the VI0_CLK pin	2-55
0x004	muxctrl_reg1	Multiplexing control register for the VI0_DAT7 pin	2-55
0x008	muxctrl_reg2	Multiplexing control register for the VI0_DAT6 pin	2-56
0x00C	muxctrl_reg3	Multiplexing control register for the VI0_DAT5 pin	2-56
0x010	muxctrl_reg4	Multiplexing control register for the VI0_DAT4 pin	2-57
0x014	muxctrl_reg5	Multiplexing control register for the VI0_DAT3 pin	2-57
0x018	muxctrl_reg6	Multiplexing control register for the VI0_DAT2 pin	2-58
0x01C	muxctrl_reg7	Multiplexing control register for the VI0_DAT1 pin	2-58
0x020	muxctrl_reg8	Multiplexing control register for the VI0_DAT0 pin	2-59
0x024	muxctrl_reg9	Multiplexing control register for the VI1_CLK pin	2-59
0x028	muxctrl_reg10	Multiplexing control register for the VI1_DAT7 pin	2-60
0x02C	muxctrl_reg11	Multiplexing control register for the VI1_DAT6 pin	2-60
0x030	muxctrl_reg12	Multiplexing control register for the VI1_DAT5 pin	2-61
0x034	muxctrl_reg13	Multiplexing control register for the VI1_DAT4 pin	2-61
0x038	muxctrl_reg14	Multiplexing control register for the VI1_DAT3 pin	2-62
0x03C	muxctrl_reg15	Multiplexing control register for the VI1_DAT2 pin	2-62
0x040	muxctrl_reg16	Multiplexing control register for the VI1_DAT1 pin	2-63
0x044	muxctrl_reg17	Multiplexing control register for the VI1_DAT0 pin	2-63
0x048	muxctrl_reg18	Multiplexing control register for the VI_ADC_REFCLK0 pin	2-64

Offset Address	Register	Description	Page
0x04C	muxctrl_reg19	Multiplexing control register for the VI2_CLK pin	2-64
0x050	muxctrl_reg20	Multiplexing control register for the VI2_DAT7 pin	2-65
0x054	muxctrl_reg21	Multiplexing control register for the VI2_DAT6 pin	2-65
0x058	muxctrl_reg22	Multiplexing control register for the VI2_DAT5 pin	2-66
0x05C	muxctrl_reg23	Multiplexing control register for the VI2_DAT4 pin	2-66
0x060	muxctrl_reg24	Multiplexing control register for the VI2_DAT3 pin	2-67
0x064	muxctrl_reg25	Multiplexing control register for the VI2_DAT2 pin	2-67
0x068	muxctrl_reg26	Multiplexing control register for the VI2_DAT1 pin	2-68
0x06C	muxctrl_reg27	Multiplexing control register for the VI2_DAT0 pin	2-68
0x070	muxctrl_reg28	Multiplexing control register for the VI3_CLK pin	2-69
0x074	muxctrl_reg29	Multiplexing control register for the VI3_DAT7 pin	2-69
0x078	muxctrl_reg30	Multiplexing control register for the VI3_DAT6 pin	2-70
0x07C	muxctrl_reg31	Multiplexing control register for the VI3_DAT5 pin	2-70
0x080	muxctrl_reg32	Multiplexing control register for the VI3_DAT4 pin	2-71
0x084	muxctrl_reg33	Multiplexing control register for the VI3_DAT3 pin	2-71
0x088	muxctrl_reg34	Multiplexing control register for the VI3_DAT2 pin	2-72
0x08C	muxctrl_reg35	Multiplexing control register for the VI3_DAT1 pin	2-72
0x090	muxctrl_reg36	Multiplexing control register for the VI3_DAT0 pin	2-73
0x094	muxctrl_reg37	Multiplexing control register for the VI_ADC_REFCLK1 pin	2-73
0x098	muxctrl_reg3	Multiplexing control register for the	2-74

Offset Address	Register	Description	Page
	8	VGA_HS pin	
0x09C	muxctrl_reg39	Multiplexing control register for the VGA_VS pin	2-74
0x0A0	muxctrl_reg40	Multiplexing control register for the I2S0_BCLK_RX pin	2-75
0x0A4	muxctrl_reg41	Multiplexing control register for the I2S0_WS_RX pin	2-75
0x0A8	muxctrl_reg42	Multiplexing control register for the I2S0_SD_RX pin	2-76
0x0AC	muxctrl_reg43	Multiplexing control register for the I2S1_BCLK_RX pin	2-76
0x0B0	muxctrl_reg44	Multiplexing control register for the I2S1_WS_RX pin	2-77
0x0B4	muxctrl_reg45	Multiplexing control register for the I2S1_SD_RX pin	2-77
0x0B8	muxctrl_reg46	Multiplexing control register for the I2S2_BCLK_TX pin	2-78
0x0BC	muxctrl_reg47	Multiplexing control register for the I2S2_WS_TX pin	2-78
0x0C0	muxctrl_reg48	Multiplexing control register for the I2S2_SD_TX pin	2-79
0x0C4	muxctrl_reg49	Multiplexing control register for the SPI_SCLK pin	2-79
0x0C8	muxctrl_reg50	Multiplexing control register for the SPI_SDO pin	2-80
0x0CC	muxctrl_reg51	Multiplexing control register for the SPI_SDI pin	2-80
0x0D0	muxctrl_reg52	Multiplexing control register for the SPI_CSN0 pin	2-81
0x0D4	muxctrl_reg53	Multiplexing control register for the SPI_CSN1 pin	2-81
0x0D8	muxctrl_reg54	Multiplexing control register for the PWM_OUT0 pin	2-82
0x0DC	muxctrl_reg55	Multiplexing control register for the PWM_OUT1 pin	2-82
0x0E0	muxctrl_reg56	Multiplexing control register for the I2C_SDA pin	2-83
0x0E4	muxctrl_reg57	Multiplexing control register for the I2C_SCL pin	2-83

Offset Address	Register	Description	Page
0x0E8	muxctrl_reg58	Multiplexing control register for the UART0_RXD pin	2-84
0x0EC	muxctrl_reg59	Multiplexing control register for the UART0_TXD pin	2-84
0x0F0	muxctrl_reg60	Multiplexing control register for the UART0_CTSN pin	2-85
0x0F4	muxctrl_reg61	Multiplexing control register for the UART0_RTSN pin	2-85
0x0F8	muxctrl_reg62	Multiplexing control register for the UART1_RXD pin	2-86
0x0FC	muxctrl_reg63	Multiplexing control register for the UART1_TXD pin	2-86
0x100	muxctrl_reg64	Multiplexing control register for the UART2_RXD pin	2-87
0x104	muxctrl_reg65	Multiplexing control register for the UART2_TXD pin	2-87
0x108	muxctrl_reg66	Multiplexing control register for the RGMII_RXDV pin	2-88
0x10C	muxctrl_reg67	Multiplexing control register for the RGMII_RXD3 pin	2-88
0x110	muxctrl_reg68	Multiplexing control register for the RGMII_RXD2 pin	2-89
0x114	muxctrl_reg69	Multiplexing control register for the RGMII_RXD1 pin	2-89
0x118	muxctrl_reg70	Multiplexing control register for the RGMII_RXD0 pin	2-90
0x11C	muxctrl_reg71	Multiplexing control register for the RGMII_RXCK pin	2-90
0x120	muxctrl_reg72	Multiplexing control register for the RGMII_TXEN pin	2-91
0x124	muxctrl_reg73	Multiplexing control register for the RGMII_TXD3 pin	2-91
0x128	muxctrl_reg74	Multiplexing control register for the RGMII_TXD2 pin	2-92
0x12C	muxctrl_reg75	Multiplexing control register for the RGMII_TXD1 pin	2-92
0x130	muxctrl_reg76	Multiplexing control register for the RGMII_TXD0 pin	2-93
0x134	muxctrl_reg7	Multiplexing control register for the	2-93

Offset Address	Register	Description	Page
	7	RGMII_TXCKOUT pin	
0x138	muxctrl_reg78	Multiplexing control register for the RGMII_CRS pin	2-94
0x13C	muxctrl_reg79	Multiplexing control register for the RGMII_COL pin	2-94
0x140	muxctrl_reg80	Multiplexing control register for the RGMII_RXER pin	2-95
0x144	muxctrl_reg81	Multiplexing control register for the EPHY_CLK pin	2-95
0x148	muxctrl_reg82	Multiplexing control register for the EPHY_RSTN pin	2-96
0x14C	muxctrl_reg83	Multiplexing control register for the MDCK pin	2-96
0x150	muxctrl_reg84	Multiplexing control register for the MDIO pin	2-97
0x154	muxctrl_reg85	Multiplexing control register for the IR_IN pin	2-97
0x158	muxctrl_reg86	Multiplexing control register for the SFC_DIO pin	2-98
0x15C	muxctrl_reg87	Multiplexing control register for the SFC_WP_IO2 pin	2-98
0x160	muxctrl_reg88	Multiplexing control register for the SFC_DOI pin	2-99
0x164	muxctrl_reg89	Multiplexing control register for the USB2_OVRCUR0 pin	2-99
0x168	muxctrl_reg90	Multiplexing control register for the USB2_PWREN0 pin	2-100
0x16C	muxctrl_reg91	Multiplexing control register for the USB2_OVRCUR1 pin	2-100
0x170	muxctrl_reg92	Multiplexing control register for the USB2_PWREN1 pin	2-101
0x174	muxctrl_reg93	Multiplexing control register for the HDMI_HOTPLUG pin	2-101
0x178	muxctrl_reg94	Multiplexing control register for the HDMI_CEC pin	2-102
0x17C	muxctrl_reg95	Multiplexing control register for the HDMI_SDA pin	2-102
0x180	muxctrl_reg96	Multiplexing control register for the HDMI_SCL pin	2-103

Offset Address	Register	Description	Page
0x184	muxctrl_reg97	Multiplexing control register for the SATA_LED_N0 pin	2-103
0x188	muxctrl_reg98	Multiplexing control register for the SATA_LED_N1 pin	2-104

2.4.2 Register Description

muxctrl_reg0

muxctrl_reg0 is a multiplexing control register for the VI0_CLK pin.

Offset Address	Register Name	Total Reset Value
0x000	muxctrl_reg0	0x00000000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	reserved								muxctrl_reg0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg0	Multiplexing control for the VI0_CLK pin 00: GPIO5_7 01: VI0_CLK 10: VI_ADC_REFCLK0 Other values: reserved

muxctrl_reg1

muxctrl_reg1 is a multiplexing control register for the VI0_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x004	muxctrl_reg1	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg1	Multiplexing control for the VI0_DAT7 pin 0: GPIO1_0 1: VI0_DAT7

muxctrl_reg2

muxctrl_reg2 is a multiplexing control register for the VI0_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x008	muxctrl_reg2	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg2
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg2	Multiplexing control for the VI0_DAT6 pin 0: GPIO1_1 1: VI0_DAT6

muxctrl_reg3

muxctrl_reg3 is a multiplexing control register for the VI0_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x00C	muxctrl_reg3	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg3
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg3	Multiplexing control for the VI0_DAT5 pin 0: GPIO1_2 1: VI0_DAT5

muxctrl_reg4

muxctrl_reg4 is a multiplexing control register for the VI0_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x010	muxctrl_reg4	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg4
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg4	Multiplexing control for the VI0_DAT4 pin 0: GPIO1_3 1: VI0_DAT4

muxctrl_reg5

muxctrl_reg5 is a multiplexing control register for the VI0_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x014	muxctrl_reg5	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg5
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg5	Multiplexing control for the VI0_DAT3 pin 0: GPIO1_4 1: VI0_DAT3

muxctrl_reg6

muxctrl_reg6 is a multiplexing control register for the VI0_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x018	muxctrl_reg6	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg6
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg6	Multiplexing control for the VI0_DAT2 pin 0: GPIO1_5 1: VI0_DAT2

muxctrl_reg7

muxctrl_reg7 is a multiplexing control register for the VI0_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x01C	muxctrl_reg7	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg7
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg7	Multiplexing control for the VI0_DAT1 pin 0: GPIO1_6 1: VI0_DAT1

muxctrl_reg8

muxctrl_reg8 is a multiplexing control register for the VI0_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x020	muxctrl_reg8	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg8
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg8	Multiplexing control for the VI0_DAT0 pin 0: GPIO1_7 1: VI0_DAT0

muxctrl_reg9

muxctrl_reg9 is a multiplexing control register for the VI1_CLK pin.

Offset Address	Register Name	Total Reset Value
0x024	muxctrl_reg9	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg9	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg9	Multiplexing control for the VI1_CLK pin 00: GPIO10_6 01: VI1_CLK 10: VI0_CLK Other values: reserved

muxctrl_reg10

muxctrl_reg10 is a multiplexing control register for the VI1_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x028	muxctrl_reg10	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg10	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg10	Multiplexing control for the VI1_DAT7 pin 0: GPIO2_0 1: VI1_DAT7

muxctrl_reg11

muxctrl_reg11 is a multiplexing control register for the VI1_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x02C	muxctrl_reg11	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg11
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg11	Multiplexing control for the VI1_DAT6 pin 0: GPIO2_1 1: VI1_DAT6

muxctrl_reg12

muxctrl_reg12 is a multiplexing control register for the VI1_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x030	muxctrl_reg12	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg12
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg12	Multiplexing control for the VI1_DAT5 pin 0: GPIO2_2 1: VI1_DAT5

muxctrl_reg13

muxctrl_reg13 is a multiplexing control register for the VI1_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x034	muxctrl_reg13	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg13
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg13	Multiplexing control for the VI1_DAT4 pin 0: GPIO2_3 1: VI1_DAT4

muxctrl_reg14

muxctrl_reg14 is a multiplexing control register for the VI1_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x038	muxctrl_reg14	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg14
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg14	Multiplexing control for the VI1_DAT3 pin 0: GPIO2_4 1: VI1_DAT3

muxctrl_reg15

muxctrl_reg15 is a multiplexing control register for the VI1_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x03C	muxctrl_reg15	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg15
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg15	Multiplexing control for the VI1_DAT2 pin 0: GPIO2_5 1: VI1_DAT2

muxctrl_reg16

muxctrl_reg16 is a multiplexing control register for the VI1_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x040	muxctrl_reg16	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg16	Multiplexing control for the VI1_DAT1 pin 0: GPIO2_6 1: VI1_DAT1

muxctrl_reg17

muxctrl_reg17 is a multiplexing control register for the VI1_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x044	muxctrl_reg17	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg17	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg17	Multiplexing control for the VI1_DAT0 pin 0: GPIO2_7 1: VI1_DAT0

muxctrl_reg18

muxctrl_reg18 is a multiplexing control register for the VI_ADC_REFCLK0 pin.

Offset Address	Register Name	Total Reset Value
0x048	muxctrl_reg18	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg18	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg18	Multiplexing control for the VI_ADC_REFCLK0 pin 00: GPIO6_0 01: VI_ADC_REFCLK0 10: VI1_CLK Other values: reserved

muxctrl_reg19

muxctrl_reg19 is a multiplexing control register for the VI2_CLK pin.

Offset Address	Register Name	Total Reset Value
0x04C	muxctrl_reg19	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 19	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg19	Multiplexing control for the VI2_CLK pin 00: GPIO11_7 01: VI2_CLK 10: VI_ADC_REFCLK1 Other values: reserved

muxctrl_reg20

muxctrl_reg20 is a multiplexing control register for the VI2_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x050	muxctrl_reg20	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 20	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg20	Multiplexing control for the VI2_DAT7 pin 0: GPIO3_0 1: VI2_DAT7

muxctrl_reg21

muxctrl_reg21 is a multiplexing control register for the VI2_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x054	muxctrl_reg21	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg21
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg21	Multiplexing control for the VI2_DAT6 pin 0: GPIO3_1 1: VI2_DAT6

muxctrl_reg22

muxctrl_reg22 is a multiplexing control register for the VI2_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x058	muxctrl_reg22	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg22
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg22	Multiplexing control for the VI2_DAT5 pin 0: GPIO3_2 1: VI2_DAT5

muxctrl_reg23

muxctrl_reg23 is a multiplexing control register for the VI2_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x05C	muxctrl_reg23	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg23
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg23	Multiplexing control for the VI2_DAT4 pin 0: GPIO3_3 1: VI2_DAT4

muxctrl_reg24

muxctrl_reg24 is a multiplexing control register for the VI2_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x060	muxctrl_reg24	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg24
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg24	Multiplexing control for the VI2_DAT3 pin 0: GPIO3_4 1: VI2_DAT3

muxctrl_reg25

muxctrl_reg25 is a multiplexing control register for the VI2_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x064	muxctrl_reg25	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg25
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg25	Multiplexing control for the VI2_DAT2 pin 0: GPIO3_5 1: VI2_DAT2

muxctrl_reg26

muxctrl_reg26 is a multiplexing control register for the VI2_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x068	muxctrl_reg26	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg26
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg26	Multiplexing control for the VI2_DAT1 pin 0: GPIO3_6 1: VI2_DAT1

muxctrl_reg27

muxctrl_reg27 is a multiplexing control register for the VI2_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x06C	muxctrl_reg27	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg27	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg27	Multiplexing control for the VI2_DAT0 pin 0: GPIO3_7 1: VI2_DAT0

muxctrl_reg28

muxctrl_reg28 is a multiplexing control register for the VI3_CLK pin.

Offset Address	Register Name	Total Reset Value
0x070	muxctrl_reg28	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg28	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg28	Multiplexing control for the VI3_CLK pin 00: GPIO10_5 01: VI3_CLK 10: VI2_CLK Other values: reserved

muxctrl_reg29

muxctrl_reg29 is a multiplexing control register for the VI3_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x074	muxctrl_reg29	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg29
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg29	Multiplexing control for the VI3_DAT7 pin 0: GPIO4_0 1: VI3_DAT7

muxctrl_reg30

muxctrl_reg30 is a multiplexing control register for the VI3_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x078	muxctrl_reg30	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg30
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg30	Multiplexing control for the VI3_DAT6 pin 0: GPIO4_1 1: VI3_DAT6

muxctrl_reg31

muxctrl_reg31 is a multiplexing control register for the VI3_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x07C	muxctrl_reg31	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg31
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg31	Multiplexing control for the VI3_DAT5 pin 0: GPIO4_2 1: VI3_DAT5

muxctrl_reg32

muxctrl_reg32 is a multiplexing control register for the VI3_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x080	muxctrl_reg32	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg32	Multiplexing control for the VI3_DAT4 pin 0: GPIO4_3 1: VI3_DAT4

muxctrl_reg33

muxctrl_reg33 is a multiplexing control register for the VI3_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x084	muxctrl_reg33	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg33
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg33	Multiplexing control for the VI3_DAT3 pin 0: GPIO4_4 1: VI3_DAT3

muxctrl_reg34

muxctrl_reg34 is a multiplexing control register for the VI3_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x088	muxctrl_reg34	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg34
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg34	Multiplexing control for the VI3_DAT2 pin 0: GPIO4_5 1: VI3_DAT2

muxctrl_reg35

muxctrl_reg35 is a multiplexing control register for the VI3_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x08C	muxctrl_reg35	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg35
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg35	Multiplexing control for the VI3_DAT1 pin 0: GPIO4_6 1: VI3_DAT1

muxctrl_reg36

muxctrl_reg36 is a multiplexing control register for the VI3_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x090	muxctrl_reg36	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg36
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg36	Multiplexing control for the VI3_DAT0 pin 0: GPIO4_7 1: VI3_DAT0

muxctrl_reg37

muxctrl_reg37 is a multiplexing control register for the VI_ADC_REFCLK1 pin.

Offset Address	Register Name	Total Reset Value
0x094	muxctrl_reg37	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg37	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg37	Multiplexing control for the VI_ADC_REFCLK1 pin 00: GPIO6_1 01: VI_ADC_REFCLK1 10: VI3_CLK Other values: reserved

muxctrl_reg38

muxctrl_reg38 is a multiplexing control register for the VGA_HS pin.

Offset Address	Register Name	Total Reset Value
0x098	muxctrl_reg38	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg38	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg38	Multiplexing control for the VGA_HS pin 0: GPIO11_6 1: VGA_HS

muxctrl_reg39

muxctrl_reg39 is a multiplexing control register for the VGA_VS pin.

Offset Address	Register Name	Total Reset Value
0x09C	muxctrl_reg39	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg39
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg39	Multiplexing control for the VGA_VS pin 0: GPIO11_3 1: VGA_VS

muxctrl_reg40

muxctrl_reg40 is a multiplexing control register for the I2S0_BCLK_RX pin.

Offset Address	Register Name	Total Reset Value
0x0A0	muxctrl_reg40	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg40
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg40	Multiplexing control for the I2S0_BCLK_RX pin 0: GPIO9_0 1: I2S0_BCLK_RX

muxctrl_reg41

muxctrl_reg41 is a multiplexing control register for the I2S0_WS_RX pin.

Offset Address	Register Name	Total Reset Value
0x0A4	muxctrl_reg41	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg41
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg41	Multiplexing control for the I2S0_WS_RX pin 0: GPIO9_1 1: I2S0_WS_RX

muxctrl_reg42

muxctrl_reg42 is a multiplexing control register for the I2S0_SD_RX pin.

Offset Address	Register Name	Total Reset Value
0x0A8	muxctrl_reg42	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg42
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg42	Multiplexing control for the I2S0_SD_RX pin 0: GPIO9_2 1: I2S0_SD_RX

muxctrl_reg43

muxctrl_reg43 is a multiplexing control register for the I2S1_BCLK_RX pin.

Offset Address	Register Name	Total Reset Value
0x0AC	muxctrl_reg43	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg43	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg43	Multiplexing control for the I2S1_BCLK_RX pin 00: GPIO9_3 01: I2S1_BCLK_RX 10: I2S2_MCLK Other values: reserved

muxctrl_reg44

muxctrl_reg44 is a multiplexing control register for the I2S1_WS_RX pin.

Offset Address	Register Name	Total Reset Value
0x0B0	muxctrl_reg44	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg44	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg44	Multiplexing control for the I2S1_WS_RX pin 0: GPIO9_4 1: I2S1_WS_RX

muxctrl_reg45

muxctrl_reg45 is a multiplexing control register for the I2S1_SD_RX pin.

Offset Address	Register Name	Total Reset Value
0x0B4	muxctrl_reg45	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg45
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg45	Multiplexing control for the I2S1_SD_RX pin 0: GPIO9_5 1: I2S1_SD_RX

muxctrl_reg46

muxctrl_reg46 is a multiplexing control register for the I2S2_BCLK_TX pin.

Offset Address	Register Name	Total Reset Value
0x0B8	muxctrl_reg46	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg46
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg46	Multiplexing control for the I2S2_BCLK_TX pin 0: GPIO9_6 1: I2S2_BCLK_TX

muxctrl_reg47

muxctrl_reg47 is a multiplexing control register for the I2S2_WS_TX pin.

Offset Address	Register Name	Total Reset Value
0x0BC	muxctrl_reg47	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg47
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg47	Multiplexing control for the I2S2_WS_TX pin 0: GPIO9_7 1: I2S2_WS_TX

muxctrl_reg48

muxctrl_reg48 is a multiplexing control register for the I2S2_SD_TX pin.

Offset Address	Register Name	Total Reset Value
0x0C0	muxctrl_reg48	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg48	Multiplexing control for the I2S2_SD_TX pin 0: GPIO5_4 1: I2S2_SD_TX

muxctrl_reg49

muxctrl_reg49 is a multiplexing control register for the SPI_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x0C4	muxctrl_reg49	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 49	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg49	Multiplexing control for the SPI_SCLK pin 00: TEST_CLK 01: SPI_SCLK 10: GPIO5_0 Other values: reserved

muxctrl_reg50

muxctrl_reg50 is a multiplexing control register for the SPI_SDO pin.

Offset Address	Register Name	Total Reset Value
0x0C8	muxctrl_reg50	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg 50	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg50	Multiplexing control for the SPI_SDO pin 0: GPIO5_1 1: SPI_SDO

muxctrl_reg51

muxctrl_reg51 is a multiplexing control register for the SPI_SDI pin.

Offset Address	Register Name	Total Reset Value
0x0CC	muxctrl_reg51	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg51
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg51	Multiplexing control for the SPI_SDI pin 0: GPIO5_2 1: SPI_SDI

muxctrl_reg52

muxctrl_reg52 is a multiplexing control register for the SPI_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x0D0	muxctrl_reg52	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg52
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg52	Multiplexing control for the SPI_CSN0 pin 0: GPIO5_3 1: SPI_CSN0

muxctrl_reg53

muxctrl_reg53 is a multiplexing control register for the SPI_CSN1 pin.

Offset Address	Register Name	Total Reset Value
0x0D4	muxctrl_reg53	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg53
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg53	Multiplexing control for the SPI_CSN1 pin 0: GPIO8_7 1: SPI_CSN1

muxctrl_reg54

muxctrl_reg54 is a multiplexing control register for the PWM_OUT0 pin.

Offset Address	Register Name	Total Reset Value
0x0D8	muxctrl_reg54	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg54
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg54	Multiplexing control for the PWM_OUT0 pin 0: PWM_OUT0 1: GPIO5_5

muxctrl_reg55

muxctrl_reg55 is a multiplexing control register for the PWM_OUT1 pin.

Offset Address	Register Name	Total Reset Value
0x0DC	muxctrl_reg55	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg55
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg55	Multiplexing control for the PWM_OUT1 pin 0: PWM_OUT1 1: GPIO5_6

muxctrl_reg56

muxctrl_reg56 is a multiplexing control register for the I2C_SDA pin.

Offset Address	Register Name	Total Reset Value
0x0E0	muxctrl_reg56	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg56
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg56	Multiplexing control for the I2C_SDA pin 0: GPIO12_6 1: I2C_SDA

muxctrl_reg57

muxctrl_reg57 is a multiplexing control register for the I2C_SCL pin.

Offset Address	Register Name	Total Reset Value
0x0E4	muxctrl_reg57	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg57
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg57	Multiplexing control for the I2C_SCL pin 0: GPIO12_7 1: I2C_SCL

muxctrl_reg58

muxctrl_reg58 is a multiplexing control register for the UART0_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0E8	muxctrl_reg58	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg58
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg58	Multiplexing control for the UART0_RXD pin 0: UART0_RXD 1: GPIO10_7

muxctrl_reg59

muxctrl_reg59 is a multiplexing control register for the UART0_TXD pin.

Offset Address	Register Name	Total Reset Value
0x0EC	muxctrl_reg59	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg59
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg59	Multiplexing control for the UART0_TXD pin 0: UART0_TXD 1: GPIO12_5

muxctrl_reg60

muxctrl_reg60 is a multiplexing control register for the UART0_CTSN pin.

Offset Address	Register Name	Total Reset Value
0x0F0	muxctrl_reg60	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg60
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg60	Multiplexing control for the UART0_CTSN pin 0: UART0_CTSN 1: GPIO6_2

muxctrl_reg61

muxctrl_reg61 is a multiplexing control register for the UART0_RTSN pin.

Offset Address	Register Name	Total Reset Value
0x0F4	muxctrl_reg61	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg61
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg61	Multiplexing control for the UART0_RTSN pin 0: UART0_RTSN 1: GPIO6_3

muxctrl_reg62

muxctrl_reg62 is a multiplexing control register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0F8	muxctrl_reg62	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg62
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg62	Multiplexing control for the UART1_RXD pin 0: GPIO6_5 1: UART1_RXD

muxctrl_reg63

muxctrl_reg63 is a multiplexing control register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x0FC	muxctrl_reg63	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg63
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg63	Multiplexing control for the UART1_TXD pin 0: GPIO6_7 1: UART1_TXD

muxctrl_reg64

muxctrl_reg64 is a multiplexing control register for the UART2_RXD pin.

Offset Address	Register Name	Total Reset Value
0x100	muxctrl_reg64	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg64
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg64	Multiplexing control for the UART2_RXD pin 0: GPIO11_4 1: UART2_RXD

muxctrl_reg65

muxctrl_reg65 is a multiplexing control register for the UART2_TXD pin.

Offset Address	Register Name	Total Reset Value
0x104	muxctrl_reg65	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg65
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg65	Multiplexing control for the UART2_TXD pin 0: GPIO11_5 1: UART2_TXD

muxctrl_reg66

muxctrl_reg66 is a multiplexing control register for the RGMII_RXDV pin.

Offset Address	Register Name	Total Reset Value
0x108	muxctrl_reg66	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg66
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg66	Multiplexing control for the RGMII_RXDV pin 0: GPIO7_0 1: RGMII_RXDV

muxctrl_reg67

muxctrl_reg67 is a multiplexing control register for the RGMII_RXD3 pin.

Offset Address	Register Name	Total Reset Value
0x10C	muxctrl_reg67	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg67
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg67	Multiplexing control for the RGMII_RXD3 pin 0: GPIO7_1 1: RGMII_RXD3

muxctrl_reg68

muxctrl_reg68 is a multiplexing control register for the RGMII_RXD2 pin.

Offset Address	Register Name	Total Reset Value
0x110	muxctrl_reg68	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg68
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg68	Multiplexing control for the RGMII_RXD2 pin 0: GPIO7_2 1: RGMII_RXD2

muxctrl_reg69

muxctrl_reg69 is a multiplexing control register for the RGMII_RXD1 pin.

Offset Address	Register Name	Total Reset Value
0x114	muxctrl_reg69	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg69
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg69	Multiplexing control for the RGMII_RXD1 pin 0: GPIO7_3 1: RGMII_RXD1

muxctrl_reg70

muxctrl_reg70 is a multiplexing control register for the RGMII_RXD0 pin.

Offset Address	Register Name	Total Reset Value
0x118	muxctrl_reg70	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg70
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg70	Multiplexing control for the RGMII_RXD0 pin 0: GPIO7_4 1: RGMII_RXD0

muxctrl_reg71

muxctrl_reg71 is a multiplexing control register for the RGMII_RXCK pin.

Offset Address	Register Name	Total Reset Value
0x11C	muxctrl_reg71	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg71
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg71	Multiplexing control for the RGMII_RXCK pin 0: GPIO7_5 1: RGMII_RXCK

muxctrl_reg72

muxctrl_reg72 is a multiplexing control register for the RGMII_TXEN pin.

Offset Address	Register Name	Total Reset Value
0x120	muxctrl_reg72	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg72
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg72	Multiplexing control for the RGMII_TXEN pin 0: GPIO7_6 1: RGMII_TXEN

muxctrl_reg73

muxctrl_reg73 is a multiplexing control register for the RGMII_TXD3 pin.

Offset Address	Register Name	Total Reset Value
0x124	muxctrl_reg73	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg73
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg73	Multiplexing control for the RGMII_TXD3 pin 0: GPIO7_7 1: RGMII_TXD3

muxctrl_reg74

muxctrl_reg74 is a multiplexing control register for the RGMII_TXD2 pin.

Offset Address	Register Name	Total Reset Value
0x128	muxctrl_reg74	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg74
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg74	Multiplexing control for the RGMII_TXD2 pin 0: GPIO8_0 1: RGMII_TXD2

muxctrl_reg75

muxctrl_reg75 is a multiplexing control register for the RGMII_TXD1 pin.

Offset Address	Register Name	Total Reset Value
0x12C	muxctrl_reg75	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg75
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg75	Multiplexing control for the RGMII_TXD1 pin 0: GPIO8_1 1: RGMII_TXD1

muxctrl_reg76

muxctrl_reg76 is a multiplexing control register for the RGMII_TXD0 pin.

Offset Address	Register Name	Total Reset Value
0x130	muxctrl_reg76	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg76
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg76	Multiplexing control for the RGMII_TXD0 pin 0: GPIO8_2 1: RGMII_TXD0

muxctrl_reg77

muxctrl_reg77 is a multiplexing control register for the RGMII_TXCKOUT pin.

Offset Address	Register Name	Total Reset Value
0x134	muxctrl_reg77	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg77	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg77	Multiplexing control for the RGMII_TXCKOUT pin 00: GPIO8_3 01: RGMII_TXCKOUT 10: MII_TXCK 11: RMII_CLK

muxctrl_reg78

muxctrl_reg78 is a multiplexing control register for the RGMII_CRS pin.

Offset Address	Register Name	Total Reset Value
0x138	muxctrl_reg78	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg78	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg78	Multiplexing control for the RGMII_CRS pin 0: GPIO8_4 1: RGMII_CRS

muxctrl_reg79

muxctrl_reg79 is a multiplexing control register for the RGMII_COL pin.

Offset Address	Register Name	Total Reset Value
0x13C	muxctrl_reg79	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg79
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg79	Multiplexing control for the RGMII_COL pin 0: GPIO8_5 1: RGMII_COL

muxctrl_reg80

muxctrl_reg80 is a multiplexing control register for the RGMII_RXER pin.

Offset Address	Register Name	Total Reset Value
0x140	muxctrl_reg80	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg80
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg80	Multiplexing control for the RGMII_RXER pin 0: GPIO8_6 1: RGMII_RXER

muxctrl_reg81

muxctrl_reg81 is a multiplexing control register for the EPHY_CLK pin.

Offset Address	Register Name	Total Reset Value
0x144	muxctrl_reg81	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg81
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg81	Multiplexing control for the EPHY_CLK pin 0: GPIO6_6 1: EPHY_CLK

muxctrl_reg82

muxctrl_reg82 is a multiplexing control register for the EPHY_RSTN pin.

Offset Address	Register Name	Total Reset Value
0x148	muxctrl_reg82	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg82
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg82	Multiplexing control for the EPHY_RSTN pin 0: GPIO6_4 1: EPHY_RSTN

muxctrl_reg83

muxctrl_reg83 is a multiplexing control register for the MDCK pin.

Offset Address	Register Name	Total Reset Value
0x14C	muxctrl_reg83	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg83	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	muxctrl_reg83	Multiplexing control for the MDCK pin 00: GPIO10_0 01: MDCK 10: BOOTROM_SEL Other values: reserved

muxctrl_reg84

muxctrl_reg84 is a multiplexing control register for the MDIO pin.

Offset Address	Register Name	Total Reset Value
0x150	muxctrl_reg84	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														muxctrl_reg84	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg84	Multiplexing control for the MDIO pin 0: GPIO10_1 1: MDIO

muxctrl_reg85

muxctrl_reg85 is a multiplexing control register for the IR_IN pin.

Offset Address	Register Name	Total Reset Value
0x154	muxctrl_reg85	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg85
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg85	Multiplexing control for the IR_IN pin 0: GPIO10_2 1: IR_IN

muxctrl_reg86

muxctrl_reg86 is a multiplexing control register for the SFC_DIO pin.

Offset Address	Register Name	Total Reset Value
0x158	muxctrl_reg86	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg86
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg86	Multiplexing control for the SFC_DIO pin 0: SFC_DIO 1: GPIO11_0

muxctrl_reg87

muxctrl_reg87 is a multiplexing control register for the SFC_WP_IO2 pin.

Offset Address	Register Name	Total Reset Value
0x15C	muxctrl_reg87	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg87
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg87	Multiplexing control for the SFC_WP_IO2 pin 0: SFC_WP_IO2 1: GPIO11_1

muxctrl_reg88

muxctrl_reg88 is a multiplexing control register for the SFC_DOI pin.

Offset Address	Register Name	Total Reset Value
0x160	muxctrl_reg88	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg88
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg88	Multiplexing control for the SFC_DOI pin 0: SFC_DOI 1: GPIO11_2

muxctrl_reg89

muxctrl_reg89 is a multiplexing control register for the USB2_OVRCUR0 pin.

Offset Address	Register Name	Total Reset Value
0x164	muxctrl_reg89	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg89
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg89	Multiplexing control for the USB2_OVRCUR0 pin 0: GPIO13_0 1: USB2_OVRCUR0

muxctrl_reg90

muxctrl_reg90 is a multiplexing control register for the USB2_PWREN0 pin.

Offset Address	Register Name	Total Reset Value
0x168	muxctrl_reg90	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg90
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg90	Multiplexing control for the USB2_PWREN0 pin 0: GPIO13_1 1: USB2_PWREN0

muxctrl_reg91

muxctrl_reg91 is a multiplexing control register for the USB2_OVRCUR1 pin.

Offset Address	Register Name	Total Reset Value
0x16C	muxctrl_reg91	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg91
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg91	Multiplexing control for the USB2_OVRCUR1 pin 0: GPIO13_2 1: USB2_OVRCUR1

muxctrl_reg92

muxctrl_reg92 is a multiplexing control register for the USB2_PWREN1 pin.

Offset Address	Register Name	Total Reset Value
0x170	muxctrl_reg92	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg92
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg92	Multiplexing control for the USB2_PWREN1 pin 0: GPIO13_3 1: USB2_PWREN1

muxctrl_reg93

muxctrl_reg93 is a multiplexing control register for the HDMI_HOTPLUG pin.

Offset Address	Register Name	Total Reset Value
0x174	muxctrl_reg93	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg93
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg93	Multiplexing control for the HDMI_HOTPLUG pin 0: GPIO13_4 1: HDMI_HOTPLUG

muxctrl_reg94

muxctrl_reg94 is a multiplexing control register for the HDMI_CEC pin.

Offset Address	Register Name	Total Reset Value
0x178	muxctrl_reg94	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg94
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg94	Multiplexing control for the HDMI_CEC pin 0: GPIO13_5 1: HDMI_CEC

muxctrl_reg95

muxctrl_reg95 is a multiplexing control register for the HDMI_SDA pin.

Offset Address	Register Name	Total Reset Value
0x17C	muxctrl_reg95	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg95
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg95	Multiplexing control for the HDMI_SDA pin 0: GPIO13_6 1: HDMI_SDA

muxctrl_reg96

muxctrl_reg96 is a multiplexing control register for the HDMI_SCL pin.

Offset Address	Register Name	Total Reset Value
0x180	muxctrl_reg96	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg96
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg96	Multiplexing control for the HDMI_SCL pin 0: GPIO13_7 1: HDMI_SCL

muxctrl_reg97

muxctrl_reg97 is a multiplexing control register for the SATA_LED_N0 pin.

Offset Address	Register Name	Total Reset Value
0x184	muxctrl_reg97	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg97
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg97	Multiplexing control for the SATA_LED_N0 pin 0: GPIO10_3 1: SATA_LED_N0

muxctrl_reg98

muxctrl_reg98 is a multiplexing control register for the SATA_LED_N1 pin.

Offset Address	Register Name	Total Reset Value
0x188	muxctrl_reg98	0x00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															muxctrl_reg98
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	muxctrl_reg98	Multiplexing control for the SATA_LED_N1 pin 0: GPIO10_4 1: SATA_LED_N1

2.5 Pin Drive Capability Registers

2.5.1 Register Summary

Table 2-29 describes pin drive capability registers.

Table 2-29 Summary of pad_ctrl registers (base address: 0x120F_0800)

Offset Address	Register	Description	Page
0x0000	PADCTRL_REG0	Drive capability register for the VI0_CLK pin	2-111
0x0004	PADCTRL_REG1	Drive capability register for the VI0_DAT7 pin	2-112
0x0008	PADCTRL_REG2	Drive capability register for the VI0_DAT6 pin	2-113
0x000C	PADCTRL_REG3	Drive capability register for the VI0_DAT5 pin	2-113
0x0010	PADCTRL_REG4	Drive capability register for the VI0_DAT4 pin	2-114
0x0014	PADCTRL_REG5	Drive capability register for the VI0_DAT3 pin	2-114
0x0018	PADCTRL_REG6	Drive capability register for the VI0_DAT2 pin	2-115
0x001C	PADCTRL_REG7	Drive capability register for the VI0_DAT1 pin	2-116
0x0020	PADCTRL_REG8	Drive capability register for the VI0_DAT0 pin	2-116
0x0024	PADCTRL_REG9	Drive capability register for the VI1_CLK pin	2-117
0x0028	PADCTRL_REG10	Drive capability register for the VI1_DAT7 pin	2-118
0x002C	PADCTRL_REG11	Drive capability register for the VI1_DAT6 pin	2-118
0x0030	PADCTRL_REG12	Drive capability register for the VI1_DAT5 pin	2-119
0x0034	PADCTRL_REG13	Drive capability register for the VI1_DAT4 pin	2-120
0x0038	PADCTRL_REG14	Drive capability register for the VI1_DAT3 pin	2-120
0x003C	PADCTRL_REG15	Drive capability register for the VI1_DAT2 pin	2-121
0x0040	PADCTRL_REG16	Drive capability register for the VI1_DAT1 pin	2-122
0x0044	PADCTRL_REG17	Drive capability register for the VI1_DAT0 pin	2-122
0x0048	PADCTRL_REG18	Drive capability register for the	2-123

Offset Address	Register	Description	Page
		VI_ADC_REFCLK0 pin	
0x004C	PADCTRL_REG19	Drive capability register for the VI2_CLK pin	2-124
0x0050	PADCTRL_REG20	Drive capability register for the VI2_DAT7 pin	2-125
0x0054	PADCTRL_REG21	Drive capability register for the VI2_DAT6 pin	2-125
0x0058	PADCTRL_REG22	Drive capability register for the VI2_DAT5 pin	2-126
0x005C	PADCTRL_REG23	Drive capability register for the VI2_DAT4 pin	2-127
0x0060	PADCTRL_REG24	Drive capability register for the VI2_DAT3 pin	2-127
0x0064	PADCTRL_REG25	Drive capability register for the VI2_DAT2 pin	2-128
0x0068	PADCTRL_REG26	Drive capability register for the VI2_DAT1 pin	2-129
0x006C	PADCTRL_REG27	Drive capability register for the VI2_DAT0 pin	2-129
0x0070	PADCTRL_REG28	Drive capability register for the VI3_CLK pin	2-130
0x0074	PADCTRL_REG29	Drive capability register for the VI3_DAT7 pin	2-131
0x0078	PADCTRL_REG30	Drive capability register for the VI3_DAT6 pin	2-131
0x007C	PADCTRL_REG31	Drive capability register for the VI3_DAT5 pin	2-132
0x0080	PADCTRL_REG32	Drive capability register for the VI3_DAT4 pin	2-133
0x0084	PADCTRL_REG33	Drive capability register for the VI3_DAT3 pin	2-133
0x0088	PADCTRL_REG34	Drive capability register for the VI3_DAT2 pin	2-134
0x008C	PADCTRL_REG35	Drive capability register for the VI3_DAT1 pin	2-135
0x0090	PADCTRL_REG36	Drive capability register for the VI3_DAT0 pin	2-135
0x0094	PADCTRL_REG37	Drive capability register for the	2-136

Offset Address	Register	Description	Page
		VI_ADC_REFCLK1 pin	
0x0098	PADCTRL_REG38	Drive capability register for the VGA_HS pin	2-137
0x009C	PADCTRL_REG39	Drive capability register for the VGA_VS pin	2-138
0x00A0	PADCTRL_REG40	Drive capability register for the I2S0_BCLK_RX pin	2-138
0x00A4	PADCTRL_REG41	Drive capability register for the I2S0_WS_RX pin	2-139
0x00A8	PADCTRL_REG42	Drive capability register for the I2S0_SD_RX pin	2-140
0x00AC	PADCTRL_REG43	Drive capability register for the I2S1_BCLK_RX pin	2-140
0x00B0	PADCTRL_REG44	Drive capability register for the I2S1_WS_RX pin	2-141
0x00B4	PADCTRL_REG45	Drive capability register for the I2S1_SD_RX pin	2-142
0x00B8	PADCTRL_REG46	Drive capability register for the I2S2_BCLK_TX pin	2-142
0x00BC	PADCTRL_REG47	Drive capability register for the I2S2_WS_TX pin	2-143
0x00C0	PADCTRL_REG48	Drive capability register for the I2S2_SD_TX pin	2-144
0x00C4	PADCTRL_REG49	Drive capability register for the SPI_SCLK pin	2-144
0x00C8	PADCTRL_REG50	Drive capability register for the SPI_SDO pin	2-145
0x00CC	PADCTRL_REG51	Drive capability register for the SPI_SDI pin	2-146
0x00D0	PADCTRL_REG52	Drive capability register for the SPI_CSN0 pin	2-146
0x00D4	PADCTRL_REG53	Drive capability register for the SPI_CSN1 pin	2-147
0x00D8	PADCTRL_REG54	Drive capability register for the PWM_OUT0 pin	2-148
0x00DC	PADCTRL_REG55	Drive capability register for the PWM_OUT1 pin	2-148
0x00E0	PADCTRL_REG56	Drive capability register for the I2C_SDA	2-149

Offset Address	Register	Description	Page
		pin	
0x00E4	PADCTRL_REG57	Drive capability register for the I2C_SCL pin	2-150
0x00E8	PADCTRL_REG58	Drive capability register for the UART0_RXD pin	2-150
0x00EC	PADCTRL_REG59	Drive capability register for the UART0_TXD pin	2-151
0x00F0	PADCTRL_REG60	Drive capability register for the UART0_CTSN pin	2-152
0x00F4	PADCTRL_REG61	Drive capability register for the UART0_RTSN pin	2-152
0x00F8	PADCTRL_REG62	Drive capability register for the UART1_RXD pin	2-153
0x00FC	PADCTRL_REG63	Drive capability register for the UART1_TXD pin	2-154
0x0100	PADCTRL_REG64	Drive capability register for the UART2_RXD pin	2-154
0x0104	PADCTRL_REG65	Drive capability register for the UART2_TXD pin	2-155
0x0108	PADCTRL_REG66	Drive capability register for the RGMII_RXDV pin	2-156
0x010C	PADCTRL_REG67	Drive capability register for the RGMII_RXD3 pin	2-156
0x0110	PADCTRL_REG68	Drive capability register for the RGMII_RXD2 pin	2-157
0x0114	PADCTRL_REG69	Drive capability register for the RGMII_RXD1 pin	2-158
0x0118	PADCTRL_REG70	Drive capability register for the RGMII_RXD0 pin	2-158
0x011C	PADCTRL_REG71	Drive capability register for the RGMII_RXCK pin	2-159
0x0120	PADCTRL_REG72	Drive capability register for the RGMII_TXEN pin	2-160
0x0124	PADCTRL_REG73	Drive capability register for the RGMII_TXD3 pin	2-161
0x0128	PADCTRL_REG74	Drive capability register for the RGMII_TXD2 pin	2-161
0x012C	PADCTRL_REG75	Drive capability register for the	2-162

Offset Address	Register	Description	Page
		RGMII_TXD1 pin	
0x0130	PADCTRL_REG76	Drive capability register for the RGMII_TXD0 pin	2-163
0x0134	PADCTRL_REG77	Drive capability register for the RGMII_TXCKOUT pin	2-164
0x0138	PADCTRL_REG78	Drive capability register for the RGMII_CRS pin	2-164
0x013C	PADCTRL_REG79	Drive capability register for the RGMII_COL pin	2-165
0x0140	PADCTRL_REG80	Drive capability register for the RGMII_RXER pin	2-166
0x0144	PADCTRL_REG81	Drive capability register for the RGMII_TXER pin	2-166
0x0148	PADCTRL_REG82	Drive capability register for the EPHY_CLK pin	2-167
0x014C	PADCTRL_REG83	Drive capability register for the EPHY_RSTN pin	2-168
0x0150	PADCTRL_REG84	Drive capability register for the MDCK pin	2-169
0x0154	PADCTRL_REG85	Drive capability register for the MDIO pin	2-169
0x0158	PADCTRL_REG86	Drive capability register for the IR_IN pin	2-170
0x015C	PADCTRL_REG87	Drive capability register for the SFC_CLK pin	2-170
0x0160	PADCTRL_REG88	Drive capability register for the SFC_DIO pin	2-171
0x0164	PADCTRL_REG89	Drive capability register for the SFC_WP_IO2 pin	2-172
0x0168	PADCTRL_REG90	Drive capability register for the SFC_DOI pin	2-172
0x016C	PADCTRL_REG91	Drive capability register for the SFC_HOLD_IO3 pin	2-173
0x0170	PADCTRL_REG92	Drive capability register for the SFC_CS0N pin	2-174
0x0174	PADCTRL_REG93	Drive capability register for the SFC_CS1N pin	2-174
0x0178	PADCTRL_REG94	Drive capability register for the JTAG_EN pin	2-175
0x017C	PADCTRL_REG95	Drive capability register for the	2-176

Offset Address	Register	Description	Page
		JTAG_TRSTN pin	
0x0180	PADCTRL_REG96	Drive capability register for the JTAG_TCK pin	2-176
0x0184	PADCTRL_REG97	Drive capability register for the JTAG_TMS pin	2-177
0x0188	PADCTRL_REG98	Drive capability register for the JTAG_TDO pin	2-178
0x018C	PADCTRL_REG99	Drive capability register for the JTAG_TDI pin	2-178
0x0190	PADCTRL_REG100	Drive capability register for the POR_ENABLE pin	2-179
0x0194	PADCTRL_REG101	Drive capability register for the RSTN pin	2-180
0x0198	PADCTRL_REG102	Drive capability register for the WDG_RSTN pin	2-180
0x019C	PADCTRL_REG103	Drive capability register for the TEST_MODE pin	2-181
0x01A0	PADCTRL_REG104	Drive capability register for the USB2_OVRCUR0 pin	2-182
0x01A4	PADCTRL_REG105	Drive capability register for the USB2_PWREN0 pin	2-182
0x01A8	PADCTRL_REG106	Drive capability register for the USB2_OVRCUR1 pin	2-183
0x01AC	PADCTRL_REG107	Drive capability register for the USB2_PWREN1 pin	2-184
0x01B0	PADCTRL_REG108	Drive capability register for the HDMI_HOTPLUG pin	2-184
0x01B4	PADCTRL_REG109	Drive capability register for the HDMI_CEC pin	2-185
0x01B8	PADCTRL_REG110	Drive capability register for the HDMI_SDA pin	2-186
0x01BC	PADCTRL_REG111	Drive capability register for the HDMI_SCL pin	2-186
0x01C0	PADCTRL_REG112	Drive capability register for the SATA_LED_N0 pin	2-187
0x01C4	PADCTRL_REG113	Drive capability register for the SATA_LED_N1 pin	2-188
0x01C8	PADCTRL_REG114	Drive capability register for the GPIO0_0 pin	2-188

Offset Address	Register	Description	Page
0x01CC	PADCTRL_REG115	Drive capability register for the GPIO0_1 pin	2-189
0x01D0	PADCTRL_REG116	Drive capability register for the GPIO0_2 pin	2-190
0x01D4	PADCTRL_REG117	Drive capability register for the GPIO0_3 pin	2-190
0x01D8	PADCTRL_REG118	Drive capability register for the GPIO0_4 pin	2-191
0x01DC	PADCTRL_REG119	Drive capability register for the GPIO0_5 pin	2-192
0x01E0	PADCTRL_REG120	Drive capability register for the GPIO0_6 pin	2-192
0x01E4	PADCTRL_REG121	Drive capability register for the GPIO0_7 pin	2-193

2.5.2 Register Description

PADCTRL_REG0

PADCTRL_REG0 is a drive capability register for the VI0_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0000	PADCTRL_REG0	0x0000_0078

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2 1 0
Name	reserved						ds	sl	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 1	1	0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the VI0_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG1

PADCTRL_REG1 is a drive capability register for the VI0_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0004	PADCTRL_REG1	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG2

PADCTRL_REG2 is a drive capability register for the VI0_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x0008	PADCTRL_REG2	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG3

PADCTRL_REG3 is a drive capability register for the VI0_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x000C	PADCTRL_REG3	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI0_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG4

PADCTRL_REG4 is a drive capability register for the VI0_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x0010	PADCTRL_REG4	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG5

PADCTRL_REG5 is a drive capability register for the VI0_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0014	PADCTRL_REG5	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG6

PADCTRL_REG6 is a drive capability register for the VI0_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x0018	PADCTRL_REG6	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI0_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG7

PADCTRL_REG7 is a drive capability register for the VI0_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x001C	PADCTRL_REG7	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG8

PADCTRL_REG8 is a drive capability register for the VI0_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x0020	PADCTRL_REG8	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI0_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI0_DAT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG9

PADCTRL_REG9 is a drive capability register for the VI1_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0024	PADCTRL_REG9	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI1_CLK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG10

PADCTRL_REG10 is a drive capability register for the VI1_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0028	PADCTRL_REG10	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG11

PADCTRL_REG11 is a drive capability register for the VI1_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x002C	PADCTRL_REG11	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG12

PADCTRL_REG12 is a drive capability register for the VI1_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x0030	PADCTRL_REG12	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI1_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG13

PADCTRL_REG13 is a drive capability register for the VI1_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x0034	PADCTRL_REG13	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG14

PADCTRL_REG14 is a drive capability register for the VI1_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0038	PADCTRL_REG14	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG15

PADCTRL_REG15 is a drive capability register for the VI1_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x003C	PADCTRL_REG15	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI1_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG16

PADCTRL_REG16 is a drive capability register for the VI1_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x0040	PADCTRL_REG16	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG17

PADCTRL_REG17 is a drive capability register for the VI1_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x0044	PADCTRL_REG17	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI1_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI1_DAT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG18

PADCTRL_REG18 is a drive capability register for the VI_ADC_REFCLK0 pin.

Offset Address	Register Name	Total Reset Value
0x0048	PADCTRL_REG18	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the VI_ADC_REFCLK0 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the VI_ADC_REFCLK0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG19

PADCTRL_REG19 is a drive capability register for the VI2_CLK pin.

Offset Address	Register Name	Total Reset Value
0x004C	PADCTRL_REG19	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ds				sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the VI2_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA

[3]	RW	sl	Level conversion rate of the VI2_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG20

PADCTRL_REG20 is a drive capability register for the VI2_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0050	PADCTRL_REG20	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG21

PADCTRL_REG21 is a drive capability register for the VI2_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x0054	PADCTRL_REG21	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG22

PADCTRL_REG22 is a drive capability register for the VI2_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x0058	PADCTRL_REG22	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI2_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG23

PADCTRL_REG23 is a drive capability register for the VI2_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x005C	PADCTRL_REG23	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG24

PADCTRL_REG24 is a drive capability register for the VI2_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0060	PADCTRL_REG24	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG25

PADCTRL_REG25 is a drive capability register for the VI2_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x0064	PADCTRL_REG25	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI2_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG26

PADCTRL_REG26 is a drive capability register for the VI2_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x0068	PADCTRL_REG26	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG27

PADCTRL_REG27 is a drive capability register for the VI2_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x006C	PADCTRL_REG27	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI2_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI2_DAT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG28

PADCTRL_REG28 is a drive capability register for the VI3_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0070	PADCTRL_REG28	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI3_CLK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG29

PADCTRL_REG29 is a drive capability register for the VI3_DAT7 pin.

Offset Address	Register Name	Total Reset Value
0x0074	PADCTRL_REG29	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG30

PADCTRL_REG30 is a drive capability register for the VI3_DAT6 pin.

Offset Address	Register Name	Total Reset Value
0x0078	PADCTRL_REG30	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG31

PADCTRL_REG31 is a drive capability register for the VI3_DAT5 pin.

Offset Address	Register Name	Total Reset Value
0x007C	PADCTRL_REG31	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI3_DAT5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG32

PADCTRL_REG32 is a drive capability register for the VI3_DAT4 pin.

Offset Address	Register Name	Total Reset Value
0x0080	PADCTRL_REG32	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG33

PADCTRL_REG33 is a drive capability register for the VI3_DAT3 pin.

Offset Address	Register Name	Total Reset Value
0x0084	PADCTRL_REG33	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG34

PADCTRL_REG34 is a drive capability register for the VI3_DAT2 pin.

Offset Address	Register Name	Total Reset Value
0x0088	PADCTRL_REG34	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the VI3_DAT2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG35

PADCTRL_REG35 is a drive capability register for the VI3_DAT1 pin.

Offset Address	Register Name	Total Reset Value
0x008C	PADCTRL_REG35	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG36

PADCTRL_REG36 is a drive capability register for the VI3_DAT0 pin.

Offset Address	Register Name	Total Reset Value
0x0090	PADCTRL_REG36	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the VI3_DAT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the VI3_DAT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG37

PADCTRL_REG37 is a drive capability register for the VI_ADC_REFCLK1 pin.

Offset Address	Register Name	Total Reset Value
0x0094	PADCTRL_REG37	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the VI_ADC_REFCLK1 pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the VI_ADC_REFCLK1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG38

PADCTRL_REG38 is a drive capability register for the VGA_HS pin.

Offset Address	Register Name	Total Reset Value
0x0098	PADCTRL_REG38	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ds				sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the VGA_HS pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA

[3]	RW	sl	Level conversion rate of the VGA_HS pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG39

PADCTRL_REG39 is a drive capability register for the VGA_VS pin.

Offset Address	Register Name	Total Reset Value
0x009C	PADCTRL_REG39	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the VGA_VS pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the VGA_VS pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG40

PADCTRL_REG40 is a drive capability register for the I2S0_BCLK_RX pin.

Offset Address	Register Name	Total Reset Value
0x00A0	PADCTRL_REG40	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S0_BCLK_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S0_BCLK_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG41

PADCTRL_REG41 is a drive capability register for the I2S0_WS_RX pin.

Offset Address	Register Name	Total Reset Value
0x00A4	PADCTRL_REG41	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the I2S0_WS_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S0_WS_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG42

PADCTRL_REG42 is a drive capability register for the I2S0_SD_RX pin.

Offset Address	Register Name	Total Reset Value
0x00A8	PADCTRL_REG42	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S0_SD_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S0_SD_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG43

PADCTRL_REG43 is a drive capability register for the I2S1_BCLK_RX pin.

Offset Address	Register Name	Total Reset Value
0x00AC	PADCTRL_REG43	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S1_BCLK_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S1_BCLK_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG44

PADCTRL_REG44 is a drive capability register for the I2S1_WS_RX pin.

Offset Address	Register Name	Total Reset Value
0x00B0	PADCTRL_REG44	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the I2S1_WS_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S1_WS_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG45

PADCTRL_REG45 is a drive capability register for the I2S1_SD_RX pin.

Offset Address	Register Name	Total Reset Value
0x00B4	PADCTRL_REG45	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S1_SD_RX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S1_SD_RX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG46

PADCTRL_REG46 is a drive capability register for the I2S2_BCLK_TX pin.

Offset Address	Register Name	Total Reset Value
0x00B8	PADCTRL_REG46	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S2_BCLK_TX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S2_BCLK_TX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG47

PADCTRL_REG47 is a drive capability register for the I2S2_WS_TX pin.

Offset Address	Register Name	Total Reset Value
0x00BC	PADCTRL_REG47	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the I2S2_WS_TX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S2_WS_TX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG48

PADCTRL_REG48 is a drive capability register for the I2S2_SD_TX pin.

Offset Address	Register Name	Total Reset Value
0x00C0	PADCTRL_REG48	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2S2_SD_TX pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2S2_SD_TX pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG49

PADCTRL_REG49 is a drive capability register for the SPI_SCLK pin.

Offset Address	Register Name	Total Reset Value
0x00C4	PADCTRL_REG49	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the SPI_SCLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_SCLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG50

PADCTRL_REG50 is a drive capability register for the SPI_SDO pin.

Offset Address	Register Name	Total Reset Value
0x00C8	PADCTRL_REG50	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SPI_SDO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_SDO pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG51

PADCTRL_REG51 is a drive capability register for the SPI_SDI pin.

Offset Address	Register Name	Total Reset Value
0x00CC	PADCTRL_REG51	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SPI_SDI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_SDI pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG52

PADCTRL_REG52 is a drive capability register for the SPI_CSN0 pin.

Offset Address	Register Name	Total Reset Value
0x00D0	PADCTRL_REG52	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SPI_CSN0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_CSN0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG53

PADCTRL_REG53 is a drive capability register for the SPI_CSN1 pin.

Offset Address	Register Name	Total Reset Value
0x00D4	PADCTRL_REG53	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SPI_CSN1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SPI_CSN1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG54

PADCTRL_REG54 is a drive capability register for the PWM_OUT0 pin.

Offset Address	Register Name	Total Reset Value
0x00D8	PADCTRL_REG54	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the PWM_OUT0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the PWM_OUT0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG55

PADCTRL_REG55 is a drive capability register for the PWM_OUT1 pin.

Offset Address	Register Name	Total Reset Value
0x00DC	PADCTRL_REG55	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the PWM_OUT1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the PWM_OUT1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG56

PADCTRL_REG56 is a drive capability register for the I2C_SDA pin.

Offset Address	Register Name	Total Reset Value
0x00E0	PADCTRL_REG56	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the I2C_SDA pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2C_SDA pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG57

PADCTRL_REG57 is a drive capability register for the I2C_SCL pin.

Offset Address	Register Name	Total Reset Value
0x00E4	PADCTRL_REG57	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the I2C_SCL pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the I2C_SCL pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG58

PADCTRL_REG58 is a drive capability register for the UART0_RXD pin.

Offset Address	Register Name	Total Reset Value
0x00E8	PADCTRL_REG58	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART0_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART0_RXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG59

PADCTRL_REG59 is a drive capability register for the UART0_TXD pin.

Offset Address	Register Name	Total Reset Value
0x00EC	PADCTRL_REG59	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the UART0_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART0_TXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG60

PADCTRL_REG60 is a drive capability register for the UART0_CTSN pin.

Offset Address	Register Name	Total Reset Value
0x00F0	PADCTRL_REG60	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART0_CTSN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART0_CTSN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG61

PADCTRL_REG61 is a drive capability register for the UART0_RTSN pin.

Offset Address	Register Name	Total Reset Value
0x00F4	PADCTRL_REG61	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART0_RTSN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART0_RTSN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG62

PADCTRL_REG62 is a drive capability register for the UART1_RXD pin.

Offset Address	Register Name	Total Reset Value
0x00F8	PADCTRL_REG62	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the UART1_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART1_RXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG63

PADCTRL_REG63 is a drive capability register for the UART1_TXD pin.

Offset Address	Register Name	Total Reset Value
0x00FC	PADCTRL_REG63	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART1_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART1_TXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG64

PADCTRL_REG64 is a drive capability register for the UART2_RXD pin.

Offset Address	Register Name	Total Reset Value
0x0100	PADCTRL_REG64	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the UART2_RXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART2_RXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG65

PADCTRL_REG65 is a drive capability register for the UART2_TXD pin.

Offset Address	Register Name	Total Reset Value
0x0104	PADCTRL_REG65	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the UART2_TXD pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the UART2_TXD pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG66

PADCTRL_REG66 is a drive capability register for the RGMII_RXDV pin.

Offset Address	Register Name	Total Reset Value
0x0108	PADCTRL_REG66	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXDV pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXDV pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG67

PADCTRL_REG67 is a drive capability register for the RGMII_RXD3 pin.

Offset Address	Register Name	Total Reset Value
0x010C	PADCTRL_REG67	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXD3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXD3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG68

PADCTRL_REG68 is a drive capability register for the RGMII_RXD2 pin.

Offset Address	Register Name	Total Reset Value
0x0110	PADCTRL_REG68	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the RGMII_RXD2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXD2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG69

PADCTRL_REG69 is a drive capability register for the RGMII_RXD1 pin.

Offset Address	Register Name	Total Reset Value
0x0114	PADCTRL_REG69	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXD1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXD1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG70

PADCTRL_REG70 is a drive capability register for the RGMII_RXD0 pin.

Offset Address	Register Name	Total Reset Value
0x0118	PADCTRL_REG70	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXD0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXD0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG71

PADCTRL_REG71 is a drive capability register for the RGMII_RXCK pin.

Offset Address	Register Name	Total Reset Value
0x011C	PADCTRL_REG71	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the RGMII_RXCK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXCK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG72

PADCTRL_REG72 is a drive capability register for the RGMII_TXEN pin.

Offset Address	Register Name	Total Reset Value
0x0120	PADCTRL_REG72	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ds				sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXEN pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXEN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG73

PADCTRL_REG73 is a drive capability register for the RGMII_TXD3 pin.

Offset Address	Register Name	Total Reset Value
0x0124	PADCTRL_REG73	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXD3 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXD3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG74

PADCTRL_REG74 is a drive capability register for the RGMII_TXD2 pin.

Offset Address	Register Name	Total Reset Value
0x0128	PADCTRL_REG74	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXD2 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXD2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG75

PADCTRL_REG75 is a drive capability register for the RGMII_TXD1 pin.

Offset Address	Register Name	Total Reset Value
0x012C	PADCTRL_REG75	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the RGMII_TXD1 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXD1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG76

PADCTRL_REG76 is a drive capability register for the RGMII_TXD0 pin.

Offset Address	Register Name	Total Reset Value
0x0130	PADCTRL_REG76	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ds				sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXD0 pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA

[3]	RW	sl	Level conversion rate of the RGMII_TXD0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG77

PADCTRL_REG77 is a drive capability register for the RGMII_TXCKOUT pin.

Offset Address	Register Name	Total Reset Value
0x0134	PADCTRL_REG77	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the RGMII_TXCKOUT pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXCKOUT pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG78

PADCTRL_REG78 is a drive capability register for the RGMII_CRS pin.

Offset Address	Register Name	Total Reset Value
0x0138	PADCTRL_REG78	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_CRS pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_CRS pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG79

PADCTRL_REG79 is a drive capability register for the RGMII_COL pin.

Offset Address	Register Name	Total Reset Value
0x013C	PADCTRL_REG79	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the RGMII_COL pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_COL pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG80

PADCTRL_REG80 is a drive capability register for the RGMII_RXER pin.

Offset Address	Register Name	Total Reset Value
0x0140	PADCTRL_REG80	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_RXER pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_RXER pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG81

PADCTRL_REG81 is a drive capability register for the RGMII_TXER pin.

Offset Address	Register Name	Total Reset Value
0x0144	PADCTRL_REG81	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RGMII_TXER pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RGMII_TXER pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG82

PADCTRL_REG82 is a drive capability register for the EPHY_CLK pin.

Offset Address	Register Name	Total Reset Value
0x0148	PADCTRL_REG82	0x0000_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved

[6:4]	RW	ds	Drive current of the EPHY_CLK pin 000: 12 mA 001: 11 mA 010: 9 mA 011: 8 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the EPHY_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG83

PADCTRL_REG83 is a drive capability register for the EPHY_RSTN pin.

Offset Address	Register Name	Total Reset Value
0x014C	PADCTRL_REG83	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the EPHY_RSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the EPHY_RSTN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG84

PADCTRL_REG84 is a drive capability register for the MDCK pin.

Offset Address	Register Name	Total Reset Value
0x0150	PADCTRL_REG84	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the MDCK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the MDCK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG85

PADCTRL_REG85 is a drive capability register for the MDIO pin.

Offset Address	Register Name	Total Reset Value
0x0154	PADCTRL_REG85	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the MDIO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the MDIO pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG86

PADCTRL_REG86 is a drive capability register for the IR_IN pin.

Offset Address	Register Name	Total Reset Value
0x0158	PADCTRL_REG86	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the IR_IN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the IR_IN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG87

PADCTRL_REG87 is a drive capability register for the SFC_CLK pin.

Offset Address	Register Name	Total Reset Value
0x015C	PADCTRL_REG87	0x0000_0058

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									ds			sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	ds	Drive current of the SFC_CLK pin 000: 18 mA 001: 16 mA 010: 14 mA 011: 12 mA 100: 5 mA 101: 4 mA 110: 2 mA 111: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_CLK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG88

PADCTRL_REG88 is a drive capability register for the SFC_DIO pin.

Offset Address	Register Name	Total Reset Value
0x0160	PADCTRL_REG88	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SFC_DIO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_DIO pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG89

PADCTRL_REG89 is a drive capability register for the SFC_WP_IO2 pin.

Offset Address	Register Name	Total Reset Value
0x0164	PADCTRL_REG89	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SFC_WP_IO2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_WP_IO2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG90

PADCTRL_REG90 is a drive capability register for the SFC_DOI pin.

Offset Address	Register Name	Total Reset Value
0x0168	PADCTRL_REG90	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SFC_DOI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_DOI pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG91

PADCTRL_REG91 is a drive capability register for the SFC_HOLD_IO3 pin.

Offset Address	Register Name	Total Reset Value
0x016C	PADCTRL_REG91	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SFC_HOLD_IO3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_HOLD_IO3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG92

PADCTRL_REG92 is a drive capability register for the SFC_CS0N pin.

Offset Address	Register Name	Total Reset Value
0x0170	PADCTRL_REG92	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SFC_CS0N pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_CS0N pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG93

PADCTRL_REG93 is a drive capability register for the SFC_CS1N pin.

Offset Address	Register Name	Total Reset Value
0x0174	PADCTRL_REG93	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SFC_CS1N pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SFC_CS1N pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG94

PADCTRL_REG94 is a drive capability register for the JTAG_EN pin.

Offset Address	Register Name	Total Reset Value
0x0178	PADCTRL_REG94	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the JTAG_EN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_EN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG95

PADCTRL_REG95 is a drive capability register for the JTAG_TRSTN pin.

Offset Address	Register Name	Total Reset Value
0x017C	PADCTRL_REG95	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the JTAG_TRSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TRSTN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG96

PADCTRL_REG96 is a drive capability register for the JTAG_TCK pin.

Offset Address	Register Name	Total Reset Value
0x0180	PADCTRL_REG96	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the JTAG_TCK pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TCK pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG97

PADCTRL_REG97 is a drive capability register for the JTAG_TMS pin.

Offset Address	Register Name	Total Reset Value
0x0184	PADCTRL_REG97	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the JTAG_TMS pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TMS pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG98

PADCTRL_REG98 is a drive capability register for the JTAG_TDO pin.

Offset Address	Register Name	Total Reset Value
0x0188	PADCTRL_REG98	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the JTAG_TDO pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TDO pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG99

PADCTRL_REG99 is a drive capability register for the JTAG_TDI pin.

Offset Address	Register Name	Total Reset Value
0x018C	PADCTRL_REG99	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the JTAG_TDI pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the JTAG_TDI pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG100

PADCTRL_REG100 is a drive capability register for the POR_ENABLE pin.

Offset Address	Register Name	Total Reset Value
0x0190	PADCTRL_REG100	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the POR_ENABLE pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the POR_ENABLE pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG101

PADCTRL_REG101 is a drive capability register for the RSTN pin.

Offset Address	Register Name	Total Reset Value
0x0194	PADCTRL_REG101	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the RSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the RSTN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG102

PADCTRL_REG102 is a drive capability register for the WDG_RSTN pin.

Offset Address	Register Name	Total Reset Value
0x0198	PADCTRL_REG102	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the WDG_RSTN pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the WDG_RSTN pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG103

PADCTRL_REG103 is a drive capability register for the TEST_MODE pin.

Offset Address	Register Name	Total Reset Value
0x019C	PADCTRL_REG103	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the TEST_MODE pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the TEST_MODE pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG104

PADCTRL_REG104 is a drive capability register for the USB2_OVRCUR0 pin.

Offset Address	Register Name	Total Reset Value
0x01A0	PADCTRL_REG104	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the USB2_OVRCUR0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the USB2_OVRCUR0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG105

PADCTRL_REG105 is a drive capability register for the USB2_PWREN0 pin.

Offset Address	Register Name	Total Reset Value
0x01A4	PADCTRL_REG105	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the USB2_PWREN0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the USB2_PWREN0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG106

PADCTRL_REG106 is a drive capability register for the USB2_OVRCUR1 pin.

Offset Address	Register Name	Total Reset Value
0x01A8	PADCTRL_REG106	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the USB2_OVRCUR1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the USB2_OVRCUR1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG107

PADCTRL_REG107 is a drive capability register for the USB2_PWREN1 pin.

Offset Address	Register Name	Total Reset Value
0x01AC	PADCTRL_REG107	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the USB2_PWREN1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the USB2_PWREN1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG108

PADCTRL_REG108 is a drive capability register for the HDMI_HOTPLUG pin.

Offset Address	Register Name	Total Reset Value
0x01B0	PADCTRL_REG108	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the HDMI_HOTPLUG pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the HDMI_HOTPLUG pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG109

PADCTRL_REG109 is a drive capability register for the HDMI_CEC pin.

Offset Address	Register Name	Total Reset Value
0x01B4	PADCTRL_REG109	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the HDMI_CEC pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the HDMI_CEC pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG110

PADCTRL_REG110 is a drive capability register for the HDMI_SDA pin.

Offset Address	Register Name	Total Reset Value
0x01B8	PADCTRL_REG110	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the HDMI_SDA pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the HDMI_SDA pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG111

PADCTRL_REG111 is a drive capability register for the HDMI_SCL pin.

Offset Address	Register Name	Total Reset Value
0x01BC	PADCTRL_REG111	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the HDMI_SCL pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the HDMI_SCL pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG112

PADCTRL_REG112 is a drive capability register for the SATA_LED_N0 pin.

Offset Address	Register Name	Total Reset Value
0x01C0	PADCTRL_REG112	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the SATA_LED_N0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SATA_LED_N0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG113

PADCTRL_REG113 is a drive capability register for the SATA_LED_N1 pin.

Offset Address	Register Name	Total Reset Value
0x01C4	PADCTRL_REG113	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the SATA_LED_N1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the SATA_LED_N1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG114

PADCTRL_REG114 is a drive capability register for the GPIO0_0 pin.

Offset Address	Register Name	Total Reset Value
0x01C8	PADCTRL_REG114	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the GPIO0_0 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_0 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG115

PADCTRL_REG115 is a drive capability register for the GPIO0_1 pin.

Offset Address	Register Name	Total Reset Value
0x01CC	PADCTRL_REG115	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the GPIO0_1 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_1 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG116

PADCTRL_REG116 is a drive capability register for the GPIO0_2 pin.

Offset Address	Register Name	Total Reset Value
0x01D0	PADCTRL_REG116	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the GPIO0_2 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_2 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG117

PADCTRL_REG117 is a drive capability register for the GPIO0_3 pin.

Offset Address	Register Name	Total Reset Value
0x01D4	PADCTRL_REG117	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the GPIO0_3 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_3 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG118

PADCTRL_REG118 is a drive capability register for the GPIO0_4 pin.

Offset Address	Register Name	Total Reset Value
0x01D8	PADCTRL_REG118	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the GPIO0_4 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_4 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG119

PADCTRL_REG119 is a drive capability register for the GPIO0_5 pin.

Offset Address	Register Name	Total Reset Value
0x01DC	PADCTRL_REG119	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the GPIO0_5 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_5 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG120

PADCTRL_REG120 is a drive capability register for the GPIO0_6 pin.

Offset Address	Register Name	Total Reset Value
0x01E0	PADCTRL_REG120	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	ds	Drive current of the GPIO0_6 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_6 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

PADCTRL_REG121

PADCTRL_REG121 is a drive capability register for the GPIO0_7 pin.

Offset Address	Register Name	Total Reset Value
0x01E4	PADCTRL_REG121	0x0000_0038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										ds		sl	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved

[5:4]	RW	ds	Drive current of the GPIO0_7 pin 00: 4 mA 01: 3 mA 10: 2 mA 11: 1 mA
[3]	RW	sl	Level conversion rate of the GPIO0_7 pin 0: fast edge 1: slow edge
[2:0]	RO	reserved	Reserved

2.6 Software Multiplexed Pins

VI

Table 2-30 lists the software multiplexed pins of VI.

Table 2-30 Software multiplexed pins of VI

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
V21	VI0_CLK	muxctrl_reg0	GPIO5_7	VI0_CLK	VI_ADC_REFCLK0
W23	VI0_DAT7	muxctrl_reg1	GPIO1_0	VI0_DAT7	-
V22	VI0_DAT6	muxctrl_reg2	GPIO1_1	VI0_DAT6	-
V23	VI0_DAT5	muxctrl_reg3	GPIO1_2	VI0_DAT5	-
U22	VI0_DAT4	muxctrl_reg4	GPIO1_3	VI0_DAT4	-
T21	VI0_DAT3	muxctrl_reg5	GPIO1_4	VI0_DAT3	-
T22	VI0_DAT2	muxctrl_reg6	GPIO1_5	VI0_DAT2	-
T23	VI0_DAT1	muxctrl_reg7	GPIO1_6	VI0_DAT1	-
R23	VI0_DAT0	muxctrl_reg8	GPIO1_7	VI0_DAT0	-
R22	VI1_CLK	muxctrl_reg9	GPIO10_6	VI1_CLK	VI0_CLK
R19	VI1_DAT7	muxctrl_reg10	GPIO2_0	VI1_DAT7	-

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
R20	VI1_DAT6	muxctrl_reg11	GPIO2_1	VI1_DAT6	-
P19	VI1_DAT5	muxctrl_reg12	GPIO2_2	VI1_DAT5	-
P20	VI1_DAT4	muxctrl_reg13	GPIO2_3	VI1_DAT4	-
P22	VI1_DAT3	muxctrl_reg14	GPIO2_4	VI1_DAT3	-
P21	VI1_DAT2	muxctrl_reg15	GPIO2_5	VI1_DAT2	-
N22	VI1_DAT1	muxctrl_reg16	GPIO2_6	VI1_DAT1	-
N23	VI1_DAT0	muxctrl_reg17	GPIO2_7	VI1_DAT0	-
M23	VI_ADC_REFCLK0	muxctrl_reg18	GPIO6_0	VI_ADC_REFCLK0	VI1_CLK
M21	VI2_CLK	muxctrl_reg19	GPIO11_7	VI2_CLK	VI_ADC_REFCLK1
N20	VI2_DAT7	muxctrl_reg20	GPIO3_0	VI2_DAT7	-
N19	VI2_DAT6	muxctrl_reg21	GPIO3_1	VI2_DAT6	-
M20	VI2_DAT5	muxctrl_reg22	GPIO3_2	VI2_DAT5	-
M19	VI2_DAT4	muxctrl_reg23	GPIO3_3	VI2_DAT4	-
L19	VI2_DAT3	muxctrl_reg24	GPIO3_4	VI2_DAT3	-
L20	VI2_DAT2	muxctrl_reg25	GPIO3_5	VI2_DAT2	-
L22	VI2_DAT1	muxctrl_reg26	GPIO3_6	VI2_DAT1	-
L21	VI2_DAT0	muxctrl_reg27	GPIO3_7	VI2_DAT0	-
K22	VI3_CLK	muxctrl_reg28	GPIO10_5	VI3_CLK	VI2_CLK
K19	VI3_DAT7	muxctrl_reg29	GPIO4_0	VI3_DAT7	-
K21	VI3_DAT6	muxctrl_reg30	GPIO4_1	VI3_DAT6	-
J20	VI3_DAT5	muxctrl_reg31	GPIO4_2	VI3_DAT5	-
J19	VI3_DAT4	muxctrl_reg32	GPIO4_3	VI3_DAT4	-
J22	VI3_DAT3	muxctrl_reg33	GPIO4_4	VI3_DAT3	-
J21	VI3_DAT2	muxctrl_reg34	GPIO4_5	VI3_DAT2	-

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
H22	VI3_DAT1	muxctrl_reg35	GPIO4_6	VI3_DAT1	-
H21	VI3_DAT0	muxctrl_reg36	GPIO4_7	VI3_DAT0	-
G23	VI_ADC_REFCLK1	muxctrl_reg37	GPIO6_1	VI_ADC_REFCLK1	VI3_CLK

Table 2-31 describes the software multiplexed pins of VI.

Table 2-31 Description of the software multiplexed pins of VI

Signal	Direction	Description
GPIO1_0	I/O	GPIO
GPIO1_1	I/O	GPIO
GPIO1_2	I/O	GPIO
GPIO1_3	I/O	GPIO
GPIO1_4	I/O	GPIO
GPIO1_5	I/O	GPIO
GPIO1_6	I/O	GPIO
GPIO1_7	I/O	GPIO
GPIO10_5	I/O	GPIO
GPIO10_6	I/O	GPIO
GPIO11_7	I/O	GPIO
GPIO2_0	I/O	GPIO
GPIO2_1	I/O	GPIO
GPIO2_2	I/O	GPIO
GPIO2_3	I/O	GPIO
GPIO2_4	I/O	GPIO
GPIO2_5	I/O	GPIO
GPIO2_6	I/O	GPIO
GPIO2_7	I/O	GPIO
GPIO3_0	I/O	GPIO
GPIO3_1	I/O	GPIO

Signal	Direction	Description
GPIO3_2	I/O	GPIO
GPIO3_3	I/O	GPIO
GPIO3_4	I/O	GPIO
GPIO3_5	I/O	GPIO
GPIO3_6	I/O	GPIO
GPIO3_7	I/O	GPIO
GPIO4_0	I/O	GPIO
GPIO4_1	I/O	GPIO
GPIO4_2	I/O	GPIO
GPIO4_3	I/O	GPIO
GPIO4_4	I/O	GPIO
GPIO4_5	I/O	GPIO
GPIO4_6	I/O	GPIO
GPIO4_7	I/O	GPIO
GPIO5_7	I/O	GPIO
GPIO6_0	I/O	GPIO
GPIO6_1	I/O	GPIO
VI_ADC_REFCLK0	O	VADC working clock 0
VI_ADC_REFCLK1	O	VADC working clock 1
VI0_CLK	I	VI0 clock signal
VI0_DAT0	I	VI0 data input
VI0_DAT1	I	VI0 data input
VI0_DAT2	I	VI0 data input
VI0_DAT3	I	VI0 data input
VI0_DAT4	I	VI0 data input
VI0_DAT5	I	VI0 data input
VI0_DAT6	I	VI0 data input
VI0_DAT7	I	VI0 data input
VI1_CLK	I	VI1 clock signal
VI1_DAT0	I	VI1 data input
VI1_DAT1	I	VI1 data input

Signal	Direction	Description
VI1_DAT2	I	VI1 data input
VI1_DAT3	I	VI1 data input
VI1_DAT4	I	VI1 data input
VI1_DAT5	I	VI1 data input
VI1_DAT6	I	VI1 data input
VI1_DAT7	I	VI1 data input
VI2_CLK	I	VI2 clock signal
VI2_DAT0	I	VI2 data input
VI2_DAT1	I	VI2 data input
VI2_DAT2	I	VI2 data input
VI2_DAT3	I	VI2 data input
VI2_DAT4	I	VI2 data input
VI2_DAT5	I	VI2 data input
VI2_DAT6	I	VI2 data input
VI2_DAT7	I	VI2 data input
VI3_CLK	I	VI3 clock signal
VI3_DAT0	I	VI3 data input
VI3_DAT1	I	VI3 data input
VI3_DAT2	I	VI3 data input
VI3_DAT3	I	VI3 data input
VI3_DAT4	I	VI3 data input
VI3_DAT5	I	VI3 data input
VI3_DAT6	I	VI3 data input
VI3_DAT7	I	VI3 data input

VGA

Table 2-32 lists the software multiplexed pins of VGA.

Table 2-32 Software multiplexed pins of VGA

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
C20	VGA_HS	muxctrl_reg38	GPIO11_6	VGA_HS
B20	VGA_VS	muxctrl_reg39	GPIO11_3	VGA_VS

Table 2-33 describes the software multiplexed pins of VGA.

Table 2-33 Description of the software multiplexed pins of VGA

Signal	Direction	Description
GPIO11_3	I/O	GPIO
GPIO11_6	I/O	GPIO
VGA_HS	O	VGA row sync output
VGA_VS	O	VGA field sync output

I2S

Table 2-34 lists the software multiplexed pins of I^2S.

Table 2-34 Software multiplexed pins of I^2S

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
T19	I2S0_BCLK_RX	muxctrl_reg40	GPIO9_0	I2S0_BCLK_RX	-
U20	I2S0_WS_RX	muxctrl_reg41	GPIO9_1	I2S0_WS_RX	-
U19	I2S0_SD_RX	muxctrl_reg42	GPIO9_2	I2S0_SD_RX	-
V19	I2S1_BCLK_RX	muxctrl_reg43	GPIO9_3	I2S1_BCLK_RX	I2S2_MCLK
W21	I2S1_WS_RX	muxctrl_reg44	GPIO9_4	I2S1_WS_RX	-
W20	I2S1_SD_RX	muxctrl_reg45	GPIO9_5	I2S1_SD_RX	-
Y22	I2S2_BCLK_TX	muxctrl_reg46	GPIO9_6	I2S2_BCLK_TX	-
Y21	I2S2_WS_TX	muxctrl_reg47	GPIO9_7	I2S2_WS_TX	-
AA23	I2S2_SD_TX	muxctrl_reg48	GPIO5_4	I2S2_SD_TX	-

Table 2-35 describes the software multiplexed pins of I^2S.

Table 2-35 Description of the software multiplexed pins of I^2S

Signal	Direction	Description
GPIO5_4	I/O	GPIO
GPIO9_0	I/O	GPIO
GPIO9_1	I/O	GPIO
GPIO9_2	I/O	GPIO
GPIO9_3	I/O	GPIO
GPIO9_4	I/O	GPIO
GPIO9_5	I/O	GPIO
GPIO9_6	I/O	GPIO
GPIO9_7	I/O	GPIO
I2S0_BCLK_RX	I/O	I^2S0/PCM0 RX clock
I2S0_SD_RX	I	Data input of the I^2S0/PCM0 interface
I2S0_WS_RX	I/O	I^2S0 RX audio channel select signal or PCM0 RX frame sync signal
I2S1_BCLK_RX	I/O	I^2S1/PCM1 RX clock
I2S1_SD_RX	I	Data input of the I^2S1/PCM1 interface
I2S1_WS_RX	I/O	I^2S1 RX audio channel select signal or PCM1 RX frame sync signal
I2S2_BCLK_TX	I/O	I^2S2/PCM2 TX clock
I2S2_MCLK	O	Main clock of the I^2S2/PCM2 interface. It can act as the working clock of the audio CODEC.
I2S2_SD_TX	O	Data output of the I^2S2/PCM2 interface
I2S2_WS_TX	I/O	I^2S2 TX audio channel select signal or PCM2 TX frame sync signal

SPI

Table 2-36 lists the software multiplexed pins of SPI.

Table 2-36 Software multiplexed pins of SPI

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
G21	SPI_SCLK	muxctrl_reg49	TEST_CLK	SPI_SCLK	GPIO5_0
H20	SPI_SDO	muxctrl_reg50	GPIO5_1	SPI_SDO	-
G20	SPI_SDI	muxctrl_reg51	GPIO5_2	SPI_SDI	-
F22	SPI_CSN0	muxctrl_reg52	GPIO5_3	SPI_CSN0	-
F23	SPI_CSN1	muxctrl_reg53	GPIO8_7	SPI_CSN1	-

Table 2-37 describes the software multiplexed pins of SPI.

Table 2-37 Description of the software multiplexed pins of SPI

Signal	Direction	Description
GPIO5_0	I/O	GPIO
GPIO5_1	I/O	GPIO
GPIO5_2	I/O	GPIO
GPIO5_3	I/O	GPIO
GPIO8_7	I/O	GPIO
SPI_CSN0	O	SPI CS0 output
SPI_CSN1	O	SPI CS1 output
SPI_SCLK	I/O	SPI clock signal
SPI_SDI	I	SPI data input
SPI_SDO	O	SPI data output
TEST_CLK	O	Output of the main test clock

PWM

Table 2-38 lists the software multiplexed pin of PWM.

Table 2-38 Software multiplexed pin of PWM

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
C4	PWM_OUT0	muxctrl_reg54	PWM_OUT0	GPIO5_5

B3	PWM_OUT1	muxctrl_reg55	PWM_OUT1	GPIO5_6

Table 2-39 lists the software multiplexed pin of PWM.

Table 2-39 Software multiplexed pin of PWM

Signal	Direction	Description
GPIO5_5	I/O	GPIO
GPIO5_6	I/O	GPIO
PWM_OUT0	O	PWM output 0
PWM_OUT1	O	PWM output 1

I2C

Table 2-40 lists the software multiplexed pins of I^2C.

Table 2-40 Software multiplexed pins of I^2C

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
G19	I2C_SDA	muxctrl_reg56	GPIO12_6	I2C_SDA
F20	I2C_SCL	muxctrl_reg57	GPIO12_7	I2C_SCL

Table 2-41 describes the software multiplexed pins of I^2C.

Table 2-41 Description of the software multiplexed pins of I^2C

Signal	Direction	Description
GPIO12_6	I/O	GPIO
GPIO12_7	I/O	GPIO
I2C_SCL	I/O	I^2C bus clock
I2C_SDA	I/O	I^2C bus data/address

UART

Table 2-42 lists the software multiplexed pins of UART.

Table 2-42 Software multiplexed pins of UART

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
D1	UART0_RXD	muxctrl_reg58	UART0_RXD	GPIO10_7
E2	UART0_TXD	muxctrl_reg59	UART0_TXD	GPIO12_5
E3	UART0_CTSN	muxctrl_reg60	UART0_CTSN	GPIO6_2
F3	UART0_RTSN	muxctrl_reg61	UART0_RTSN	GPIO6_3
F2	UART1_RXD	muxctrl_reg62	GPIO6_5	UART1_RXD
F1	UART1_TXD	muxctrl_reg63	GPIO6_7	UART1_TXD
W13	UART2_RXD	muxctrl_reg64	GPIO11_4	UART2_RXD
Y14	UART2_TXD	muxctrl_reg65	GPIO11_5	UART2_TXD

Table 2-43 describes the software multiplexed pins of UART.

Table 2-43 Description of the software multiplexed pins of UART

Signal	Direction	Description
GPIO10_7	I/O	GPIO
GPIO11_4	I/O	GPIO
GPIO11_5	I/O	GPIO
GPIO12_5	I/O	GPIO
GPIO6_2	I/O	GPIO
GPIO6_3	I/O	GPIO
GPIO6_5	I/O	GPIO
GPIO6_7	I/O	GPIO
UART0_CTSN	I	UART0 CTS (Clear To Send) signal, active low
UART0_RTSN	O	UART0 RTS (Request To Send) signal, active low
UART0_RXD	I	UART0 RX data
UART0_TXD	O	UART0 TX data
UART1_RXD	I	UART1 RX data
UART1_TXD	O	UART1 TX data
UART2_RXD	I	UART2 RX data

Signal	Direction	Description
UART2_TXD	O	UART2 TX data

RGMII

Table 2-44 lists the software multiplexed pins of RGMII.

Table 2-44 Software multiplexed pins of RGMII

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2	Multiplexed Signal 3
D10	RGMII_RXDV	muxctrl_reg66	GPIO7_0	RGMII_RXDV	-	-
B10	RGMII_RXD3	muxctrl_reg67	GPIO7_1	RGMII_RXD3	-	-
B9	RGMII_RXD2	muxctrl_reg68	GPIO7_2	RGMII_RXD2	-	-
C9	RGMII_RXD1	muxctrl_reg69	GPIO7_3	RGMII_RXD1	-	-
B8	RGMII_RXD0	muxctrl_reg70	GPIO7_4	RGMII_RXD0	-	-
A10	RGMII_RXCK	muxctrl_reg71	GPIO7_5	RGMII_RXCK	-	-
E12	RGMII_TXEN	muxctrl_reg72	GPIO7_6	RGMII_TXEN	-	-
C13	RGMII_TXD3	muxctrl_reg73	GPIO7_7	RGMII_TXD3	-	-
B13	RGMII_TXD2	muxctrl_reg74	GPIO8_0	RGMII_TXD2	-	-
B12	RGMII_TXD1	muxctrl_reg75	GPIO8_1	RGMII_TXD1	-	-
A12	RGMII_TXD0	muxctrl_reg76	GPIO8_2	RGMII_TXD0	-	-
B11	RGMII_TXCKOUT	muxctrl_reg77	GPIO8_3	RGMII_TXCKOUT	MII_TXCK	RMII_CLK
D12	RGMII_CRS	muxctrl_reg78	GPIO8_4	RGMII_CRS	-	-
D11	RGMII_COL	muxctrl_reg79	GPIO8_5	RGMII_COL	-	-
E11	RGMII_RXER	muxctrl_reg80	GPIO8_6	RGMII_RXER	-	-
E14	EPHY_CLK	muxctrl_reg81	GPIO6_6	EPHY_CLK	-	-
D13	EPHY_RSTN	muxctrl_reg82	GPIO6_4	EPHY_RSTN	-	-

Table 2-45 describes the software multiplexed pins of RGMII.

Table 2-45 software multiplexed pins of RGMII

Signal	Direction	Description
EPHY_CLK	O	Working clock of the Ethernet PHY
EPHY_RSTN	O	Reset signal of Ethernet PHY, active low
GPIO6_4	I/O	GPIO
GPIO6_6	I/O	GPIO
GPIO7_0	I/O	GPIO
GPIO7_1	I/O	GPIO
GPIO7_2	I/O	GPIO
GPIO7_3	I/O	GPIO
GPIO7_4	I/O	GPIO
GPIO7_5	I/O	GPIO
GPIO7_6	I/O	GPIO
GPIO7_7	I/O	GPIO
GPIO8_0	I/O	GPIO
GPIO8_1	I/O	GPIO
GPIO8_2	I/O	GPIO
GPIO8_3	I/O	GPIO
GPIO8_4	I/O	GPIO
GPIO8_5	I/O	GPIO
GPIO8_6	I/O	GPIO
MII_TXCK	I	TX clock in MII mode
RGMII_COL	I	Conflict detection signal in MII mode
RGMII_CRS	I	Carrier sense signal in MII mode
RGMII_RXCK	I	RX clock in RGMII or MII mode
RGMII_RXD0	I	RX data 0 in RGMII, MII, or RMII mode
RGMII_RXD1	I	RX data 1 in RGMII, MII, or RMII mode
RGMII_RXD2	I	RX data 2 in RGMII or MII mode
RGMII_RXD3	I	RX data 3 in RGMII or MII mode
RGMII_RXDV	I	RX data validity signal in RGMII or MII mode RX data validity or carrier detection signal in RMII

Signal	Direction	Description
		mode
RGMII_RXER	I	RX error signal in MII or RMII mode
RGMII_TXCKOUT	O	TX clock (active on both edges) in RGMII gigabit mode
RGMII_TXD0	O	TX data 0 in RGMII, MII, or RMII mode
RGMII_TXD1	O	TX data 1 in RGMII, MII, or RMII mode
RGMII_TXD2	O	TX data 2 in RGMII or MII mode
RGMII_TXD3	O	TX data 3 in RGMII or MII mode
RGMII_TXEN	O	TX data validity signal in RGMII, MII, or RMII mode
RMII_CLK	I/O	Reference clock in RMII mode

MDIO

Table 2-46 lists the software multiplexed pins of MDIO.

Table 2-46 Software multiplexed pins of MDIO

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1	Multiplexed Signal 2
A14	MDCK	muxctrl_reg83	GPIO10_0	MDCK	BOOTROM_SEL
D14	MDIO	muxctrl_reg84	GPIO10_1	MDIO	-

Table 2-47 describes the software multiplexed pins of MDIO.

Table 2-47 Description of the software multiplexed pins of MDIO

Signal	Direction	Description
BOOTROM_SEL	I	BOOTROM boot 0: boot from the SPI flash 1: boot from the BOOTROM
GPIO10_0	I/O	GPIO
GPIO10_1	I/O	GPIO
MDCK	O	Clock output of the MDIO0 interface
MDIO	I/O	I/O signal of the MDIO0 interface

IR

Table 2-48 lists the software multiplexed pin of IR.

Table 2-48 Software multiplexed pin of IR

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
AA14	IR_IN	muxctrl_reg85	GPIO10_2	IR_IN

Table 2-49 describes the software multiplexed pins of IR.

Table 2-49 Description of the software multiplexed pins of IR

Signal	Direction	Description
GPIO10_2	I/O	GPIO
IR_IN	I	IR input

SFC

Table 2-50 lists the software multiplexed pins of SFC.

Table 2-50 Software multiplexed pins of SFC

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
AB21	SFC_DIO	muxctrl_reg86	SFC_DIO	GPIO11_0
AB23	SFC_WP_IO2	muxctrl_reg87	SFC_WP_IO2	GPIO11_1
AB22	SFC_DOI	muxctrl_reg88	SFC_DOI	GPIO11_2

Table 2-51 describes the software multiplexed pins of SFC.

Table 2-51 Description of the software multiplexed pins of SFC

Signal	Direction	Description
GPIO11_0	I/O	GPIO
GPIO11_1	I/O	GPIO
GPIO11_2	I/O	GPIO
SFC_DIO	I/O	Data output signal in standard SPI mode

Signal	Direction	Description
		Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode
SFC_DOI	I/O	Data input signal in standard SPI mode Data I/O signal in dual-SPI mode Data I/O signal in quad-SPI mode
SFC_WP_IO2	I/O	Write protection function in standard SPI mode, active low Write protection function in dual-SPI mode, active low Data I/O signal in quad-SPI mode

USB2

Table 2-52 lists the software multiplexed pins of USB 2.0.

Table 2-52 Software multiplexed pins of USB 2.0

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
A5	USB2_OVRCUR0	muxctrl_reg89	GPIO13_0	USB2_OVRCUR0
B5	USB2_PWREN0	muxctrl_reg90	GPIO13_1	USB2_PWREN0
A4	USB2_OVRCUR1	muxctrl_reg91	GPIO13_2	USB2_OVRCUR1
B4	USB2_PWREN1	muxctrl_reg92	GPIO13_3	USB2_PWREN1

Table 2-53 describes the software multiplexed pins of USB 2.0..

Table 2-53 Description of the software multiplexed pins of USB 2.0

Signal	Direction	Description
GPIO13_0	I/O	GPIO
GPIO13_1	I/O	GPIO
GPIO13_2	I/O	GPIO
GPIO13_3	I/O	GPIO
USB2_OVRCUR0	I	Overcurrent indicator of USB port 0, configurable level, and active high by default
USB2_OVRCUR1	I	Overcurrent indicator of USB port 1, configurable level, and active high by default

Signal	Direction	Description
USB2_PWREN0	O	Power control output signal of USB port 0, configurable level, and active low by default
USB2_PWREN1	O	Power control output signal of USB port 1, configurable level, and active low by default

HDMI

Table 2-54 lists the software multiplexed pins of HDMI.

Table 2-54 Software multiplexed pins of HDMI

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
D19	HDMI_HOTPLUG	muxctrl_reg93	GPIO13_4	HDMI_HOTPLUG
A19	HDMI_CEC	muxctrl_reg94	GPIO13_5	HDMI_CEC
C19	HDMI_SDA	muxctrl_reg95	GPIO13_6	HDMI_SDA
B19	HDMI_SCL	muxctrl_reg96	GPIO13_7	HDMI_SCL

Table 2-55 describes the software multiplexed pins of HDMI.

Table 2-55 Description of the software multiplexed pins of HDMI

Signal	Direction	Description
GPIO13_4	I/O	GPIO
GPIO13_5	I/O	GPIO
GPIO13_6	I/O	GPIO
GPIO13_7	I/O	GPIO
HDMI_CEC	I/O	CEC (Consumer Electronic Control) channel signal of the HDMI
HDMI_HOTPLUG	I	Hot plug detection signal of the HDMI
HDMI_SCL	I/O	DDC (Display Data Channel) clock signal of the HDMI
HDMI_SDA	I/O	DDC (Display Data Channel) data/address signal of the HDMI

SATA

Table 2-56 lists the software multiplexed pins of SATA.

Table 2-56 Software multiplexed pins of SATA

Pin	Pad Signal	Multiplexing Control Register	Multiplexed Signal 0	Multiplexed Signal 1
W14	SATA_LED_N0	muxctrl_reg97	GPIO10_3	SATA_LED_N0
Y15	SATA_LED_N1	muxctrl_reg98	GPIO10_4	SATA_LED_N1

Table 2-57 describes the software multiplexed pins of SATA

Table 2-57 Description of the software multiplexed pins of SATA

Signal	Direction	Description
GPIO10_3	I/O	GPIO
GPIO10_4	I/O	GPIO
SATA_LED_N0	O	LED indicator signal of SATA port 0, active low
SATA_LED_N1	O	LED indicator signal of SATA port 1, active low

2.7 Hardware Multiplexed Pins

RGMII

Table 2-58 lists the hardware multiplexed pin of the RGMII.

Table 2-58 Hardware multiplexed pin of the RGMII

Pin	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
E15	RGMII_TXER	SFC_DEVICE_MODE

Table 2-59 describes the hardware multiplexed pin of the RGMII.

Table 2-59 Description of the hardware multiplexed pin of the RGMII

Signal	Direction	Description
SFC_DEVICE_MODE	I	SPI flash select 0: SPI NOR flash

		1: SPI NAND flash

SFC

Table 2-60 lists the hardware multiplexed pin of the SFC.

Table 2-60 Hardware multiplexed pin of the SFC

Pin	Pad Signal	Multiplexed Signal 1 (power_on == 1'b1)
AA20	SFC_CLK	SFC_BOOT_MODE

Table 2-61 describes the hardware multiplexed pin of the SFC.

Table 2-61 Description of the hardware multiplexed pin of the SFC

Signal	Direction	Description
SFC_BOOT_MODE	I	Boot address mode of the SPI NOR flash when **SFC_DEVICE_MODE** is 0 0: 3-byte address mode 1: 4-byte address mode Boot mode of the SPI NAND flash when **SFC_DEVICE_MODE** is 1 0: 1-wire boot mode 1: 4-wire boot mode

JTAG

Table 2-62 lists the hardware multiplexed pins of the JTAG.

Table 2-62 Hardware multiplexed pins of the JTAG

Pin	Pad Signal	Multiplexed Signal 1 (jtag_en == 1'b0)
AB13	JTAG_TRSTN	GPIO12_0
AC13	JTAG_TCK	GPIO12_1
Y13	JTAG_TMS	GPIO12_2
AB12	JTAG_TDO	GPIO12_3
AA13	JTAG_TDI	GPIO12_4

Table 2-63 describes the hardware multiplexed pin of the JTAG.

Table 2-63 Description of the hardware multiplexed pin of the JTAG

Signal	Direction	Description
GPIO12_0	I/O	GPIO
GPIO12_1	I/O	GPIO
GPIO12_2	I/O	GPIO
GPIO12_3	I/O	GPIO
GPIO12_4	I/O	GPIO

SYS

Table 2-64 lists the hardware multiplexed pin of the SYS.

Table 2-64 Hardware multiplexed pin of the SYS

Pin	Pad Signal	Multiplexed Signal 1 (por_bypass == 1'b0)
AB19	WDG_RSTN	SYS_RSTN_OUT

Table 2-65 describes the hardware multiplexed pin of the SYS.

Table 2-65 Description of the hardware multiplexed pin of the SYS

Signal	Direction	Description
SYS_RSTN_OUT	O	System reset output, active low

2.8 Electrical Specifications

2.8.1 Power Consumption Parameters

Table 2-66 describes power consumption parameters.

CAUTION

- The values of power consumption parameters are provided based on typical application scenarios.

- Design board power supplies by following the *Hi3521AHardware Design User Guide*.

Table 2-66 Power consumption parameters

Parameter	Description	Typ	Max	Unit
Core power	Core power	1178	1549	mA
CPU power	CPU power	111	223	mA
3.3 V power	Interface current	158	168	mA
1.5 V power	DDR interface current	269	313	mA

NOTE

The typical application scenarios are as follows:

- 8x720p@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4x720p@30 fps H.264 decoding+8x720p@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

2.8.2 Temperature and Thermal Resistance Parameters

Table 2-67 describes temperature and thermal resistance parameters.

NOTE

- The thermal resistance is provided in compliance with the JEDEC JESD51-2 standard. The actual system design and environment may be different.
- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.
- Design heat dissipation by following the *Hi3521A Hardware Design User Guide*.
- The chip can be stored in the sealed packaging bag for up to 12 months when the temperature is below 40ºC (104ºF) and the relative humidity (RH) is below 90%.
- After the packaging bag is opened, the following conditions must be met before the component is used in the reflow soldering process or other high-temperature processes:

  a. The process is complete within 168 hours at 30ºC (86ºF) or lower and at most 60% RH.

  b. The component is stored at the RH lower than 10%.
- The soldering temperature curve is based on the J-STD-020D.1 standard.

Table 2-67 Temperature and thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature	T_A	0	None	70	ºC
Rated temperature	T_{JMAX}	–20	None	110	ºC
Junction-to-ambient thermal resistance	θ_{JA}	None	23	None	ºC/W
Junction-to-board thermal resistance	θ_{JB}	None	9.62	None	ºC/W
Junction-to-case thermal resistance	θ_{JC}	None	5.53	None	ºC/W

CAUTION

The ambient temperature is used in chip operating conditions, while the junction temperature only serves as a reference during thermal simulation.

2.8.3 Operating Conditions

CAUTION

The voltage ranges in Table 2-68 are applicable on the condition that the SVB circuit is used on the demo board of the customer and the resistance-capacitance parameters of the SVB circuit must be designed by completely following table 1-3 and table 1-4 in section 1.1.6 "SVB Dynamic Voltage Scaling" in the *Hi3521A Hardware Design User Guide*.

Table 2-68 and Table 2-69 describe operating conditions.

Table 2-68 Operating conditions for the SVB related power supply

Symbol	Description	Min	Typ	Max	power supply noise Vpp	Unit
DVDD_CORE	Core power	1.05	1.1	1.15	0.055	V
DVDD_CPU	CPU core power	1.15	1.25	1.30	0.06	V
AVDD_VP_SATA0 AVDD_VP_SATA1	SATA core analog power	1.05	1.1	1.15	0.055	V
AVDD_VPTX_SATA0 AVDD_VPTX_SATA1	SATA core analog power	1.05	1.1	1.15	0.055	V
AVDD_PLL	PLL core analog power	1.05	1.1	1.15	0.055	V
AVCC__HDMITX	HDMI TX core analog power	1.05	1.1	1.15	0.055	V
AVCC_USB	USB core analog power	1.05	1.1	1.15	0.055	V

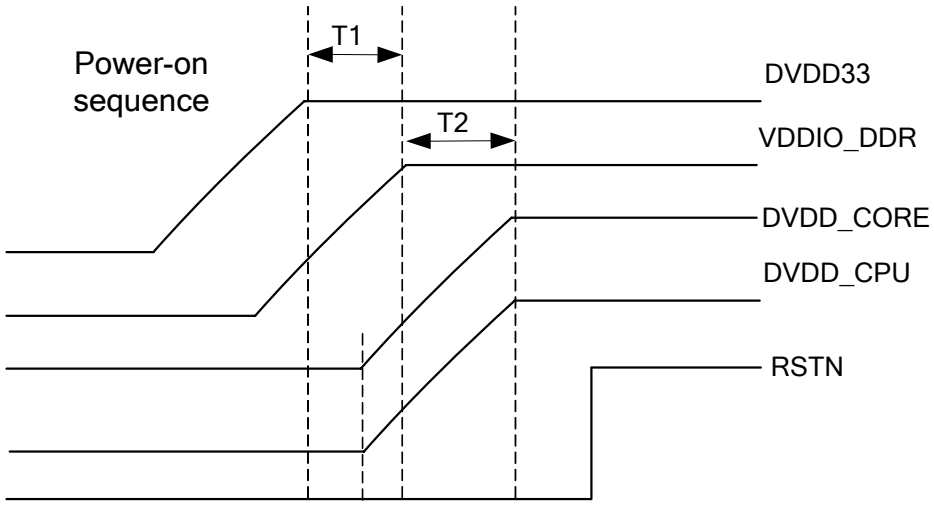
Table 2-69 Operating conditions for the power supply under normal voltage

Symbol	Description	Min	Typ	Max	Unit
DVDD33	I/O power	2.97	3.3	3.63	V
AVDD33_VPH_SATA0 AVDD33_VPH_SATA1	3.3 V SATA analog power	3.125	3.3	3.6	V
DVDD3318_SFC	SFC I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
DVDD3318_I2S	I^2S1/I^2S2 I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
DVDD3318_VI	I^2S0/VI/SPI I/O power	2.97/1.62	3.3/1.8	3.63/1.98	V
AVDD_EFUSE	2.5 V eFUSE analog power	2.25	2.5	2.75	V
DVDDIO_RGMII	RGMII power	2.97/2.25	3.3/2.5	3.63/2.75	V
AVDD33_PLL	3.3 V PLL analog power	3.135	3.3	3.465	V
AVDD33_RTC	RTC analog power	3.0	3.3	3.63	V
AVDD33_VDAC	3.3 V VDAC RGB analog power	3.125	3.3	3.465	V
DVDD33_VDAC	3.3 V VDAC digital power	2.97	3.3	3.63	V
AVDD33_HDMITX	3.3 V HDMI TX analog power	3.125	3.3	3.465	V
AVDD33_USB	3.3 V USB analog power	3.125	3.3	3.6	V
AVDD_DDRPLL_0 AVDD_DDRPLL_1 AVDD_DDRPLL_2	3.3 V DDR3 PLL analog power	3.125	3.3	3.465	V
VDDIO_DDR	DDR3 interface power	1.425	1.5	1.575	V
VDDIO_DDR_CK	DDR3 clock interface power	1.425	1.5	1.575	V

2.8.4 Power-On and Power-Off Sequences

Figure 2-9 shows the power-on sequence.

Figure 2-9 Power-on sequence

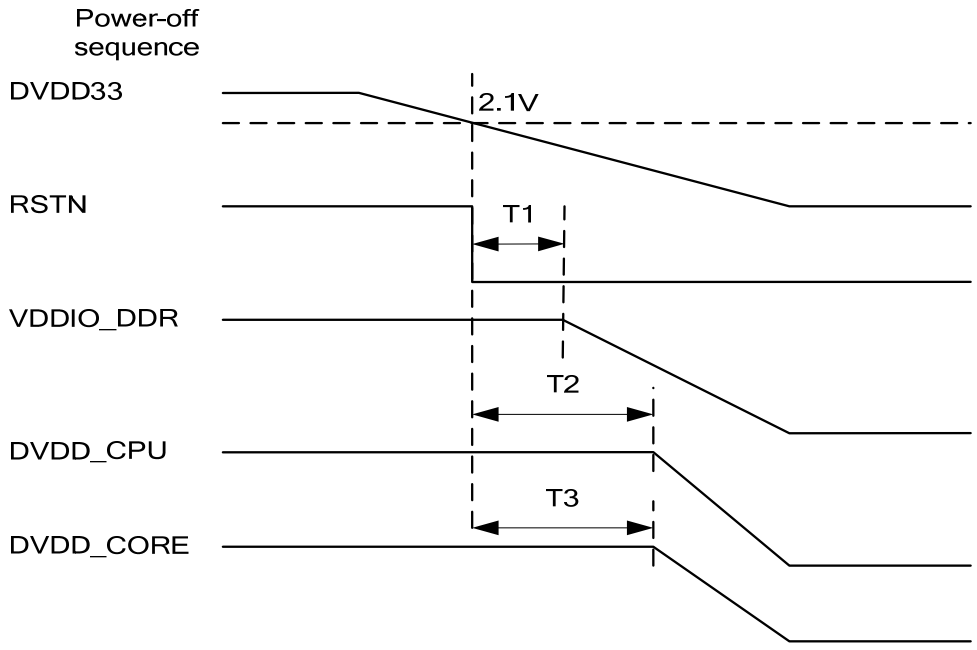


NOTE

T1 + T2 ≤ 100 ms; T2 > 0; T1 > 0. DVDD_CORE and DVDD_CPU are powered on at the same time.

Figure 2-10 shows the power-on sequence.

Figure 2-10 Power-off sequence



NOTE

T1 > 0, T2 > 0, T3 > 0.

2.8.5 DC and AC Electrical Parameters

Table 2-70 to Table 2-72 describe DC electrical parameters.

Table 2-70 DC electrical parameters (DVDD33 = 3.3 V, some interfaces support the 5 V input voltage)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD33	Interface voltage	3.125	3.3	3.6	V	-
V_{IH}	High-level input voltage	2.0	-	DVDD33 +0.3	V	Incompatible with the 5 V input voltage. Some interfaces support the 5 V input voltage, and the maximum input voltage is 5.5 V.
V_{IL}	Low-level input voltage	–0.3	-	0.8	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	2.4	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.4	V	-
R_{PU}	Internal pull-up resistor	80	90	100	kΩ	-
R_{PD}	Internal pull-down resistor	80	90	100	kΩ	-
R_{PU8k}	8 kΩ pull-up resistor	7.1	8.5	10	kΩ	-
R_{PD8k}	8 kΩ pull-down resistor	7.1	8.4	10	kΩ	-

Table 2-71 DC electrical parameters (DVDD332518 = 2.5 V, some interfaces support the 5 V input voltage)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD332518	Interface voltage	2.25	2.5	2.75	V	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{IH}	High-level input voltage	1.7	-	DVDD 332518 + 0.3	V	Incompatible with the 5 V input voltage. Some interfaces support the 5 V input voltage, and the maximum input voltage is 5.5 V.
V_{IL}	Low-level input voltage	–0.3	-	0.7	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	1.8	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.5	V	-
R_{PU}	Internal pull-up resistor	80	90	100	kΩ	-
R_{PD}	Internal pull-down resistor	80	90	100	kΩ	-
R_{PU8k}	8 kΩ pull-up resistor	6.7	8.56	10.63	kΩ	-
R_{PD8k}	8 kΩ pull-down resistor	6.49	8.3	10.3	kΩ	-

Table 2-72 DC electrical parameters (DVDD3318 = 1.8 V, some interfaces support the 5 V input voltage)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD3318	Interface voltage	1.71	1.8	1.98	V	1.8 V NAND flash interface
V_{IH}	High-level input voltage	0.65 x DVDD3318	-	DVDD 3318 + 0.3	V	
V_{IL}	Low-level input voltage	–0.3	-	0.35 x DVDD 3318	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
V_{OH}	High-level output voltage	DVDD3318 − 0.45	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.45	V	-
R_{PU}	Internal pull-up resistor	80	90	100	kΩ	-
R_{PD}	Internal pull-down resistor	80	90	100	kΩ	-
R_{PU8k}	8 kΩ pull-up resistor	7.4	9	11	kΩ	
R_{PD8k}	8 kΩ pull-down resistor	7.1	8.9	11	kΩ	

Table 2-73 describes DC electrical parameters in DDR3 mode.

Table 2-73 DC electrical parameters in DDR3 mode (VDDIO_DDR = 1.5 V, DDR3 mode)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.425	1.5	1.575	V	-
Vref	Reference voltage	0.49 x VDDIO_DDR	0.5 x VDDIO_DDR	0.51 x VDDIO_DDR	-	(0.49−0.51) x DDR_DVDDIO
VTT	Termination voltage	Vref − 40	Vref	Vref + 40	mV	-
$V_{IH(DC)}$	High-level input voltage	Vref + 0.1	-	VDDIO_DDR + 0.3	V	-
$V_{IL(DC)}$	Low-level input voltage	–0.3	-	Vref − 0.1	V	-
V_{OH}	High-level output voltage	0.8 x VDDIO_DDR	-	(1 + 0.1) x VDDIO_DDR	V	The drive voltage is configurable.
V_{OL}	Low-level output voltage	0	-	0.2 x VDDIO_DDR	V	The drive voltage is configurable.
Output impedance	-	34	-	80	Ω	

Table 2-74 describes AC electrical parameters in DDR3 mode.

Table 2-74 AC electrical parameters in DDR3 mode (DDR_VDDQ = 1.5 V, DDR3 mode)

Symbol	Description	Min	Max	Unit	Remarks
$V_{IH(AC)}$	High-level input voltage	Vref + 0.15	VDDIO_DDR + 0.3	V	-
$V_{IL(AC)}$	Low-level input voltage	-	Vref − 0.15	V	-
V_{OH}	High-level output voltage	VTT + 0.1 x VDDIO_DDR	-	V	-
V_{OL}	Low-level output voltage	-	VTT − 0.1 x VDDIO_DDR	V	-

2.9 PCB Design Recommendations

For details about printed circuit board (PCB) design recommendations, see the *Hi3521A Hardware Design User Guide*.

2.10 Interface Timings

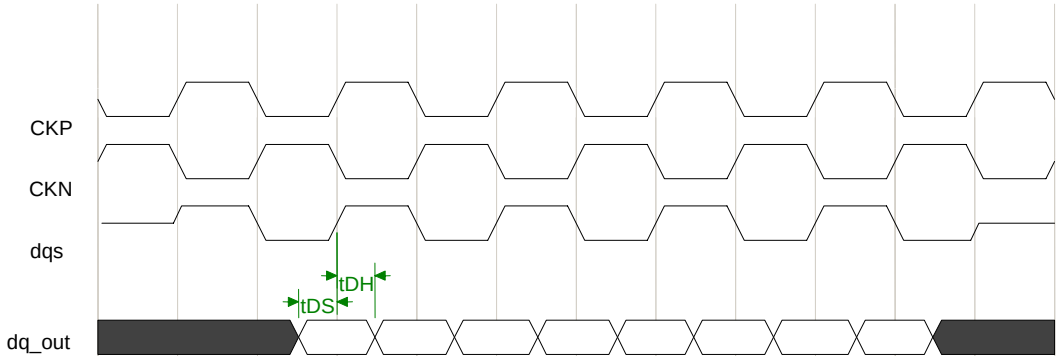
2.10.1 DDR Interface Timings

2.10.1.1 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are tDS and tDH.

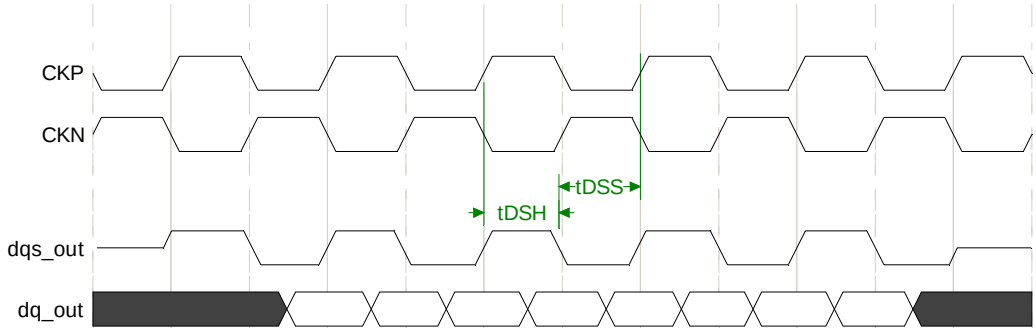
Figure 2-11 Write timing of dqs_out relative to dq_out for the DDR3



Write Timings of dqs_out Relative to CK

Figure 2-4 shows the write timing of dqs_out relative to CK for the DDR3.

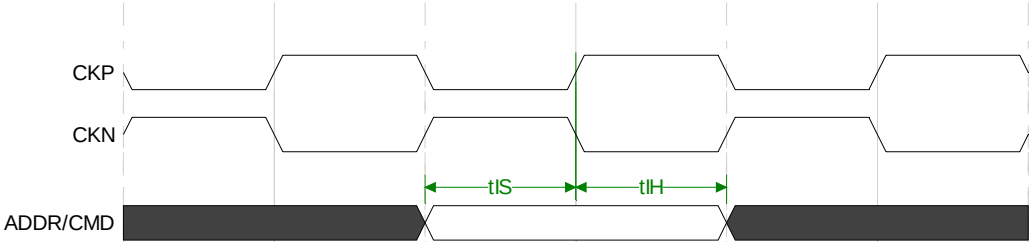
Figure 2-12 Write timing of dqs_out relative to CK for the DDR3



Write Timing of CMD/ADDR Relative to CK

Figure 2-5 shows the write timing of CMD/ADDR relative to CK.

Figure 2-13 Write timing of CMD/ADDR relative to CK



2.10.1.2 Read Timings

Read Timing of CMD/ADDR Relative to CK

The read timing of CMD/ADDR relative to CK is the same as the "Write Timing of CMD/ADDR Relative to CK".

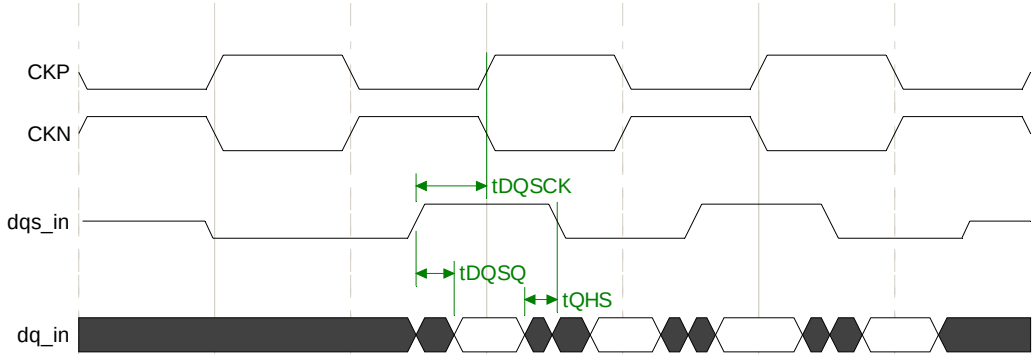
Read Timings of dqs_in Relative to dq_in

The read timings of dqs_in relative to dq_in are classified into the DDRn SDRAM output timing, dqs_in timing on the DDR PHY side, and dq_in timing on the DDR PHY side.

For the DDR SDRAM output timing, the phases of DQS and CK are the same in the ideal condition; however, there is a tDQSCK skew between DQS and CK. The value of tDQSCK is 0.35 ns. tDQSQ is the jitter of the last valid DQ relative to DQS and its value is 0.2 ns; tQHS is the jitter of the first valid DQ relative to DQS and its value is 0.3 ns.

Figure 2-6 shows the output timing of the DDRn SDRAM.

Figure 2-14 Output timing of the DDRn SDRAM



2.10.1.3 Timing Parameters

The timings of the DDR interface comply with the JEDEC standards including JESD79-2E and JESD79-3B standards. All the timings in this document are output on the DDR PHY side.

The Hi3521A is based on the timing parameters of the DDR3-1600 SDRAMs.

Table 2-75 and Table 2-76 describe the clock parameters of the DDR3-1600 SDRAM.

Table 2-75 DDR3 clock parameters

Parameter	Typ	Unit
DDR clock frequency	800.00	MHz
PLL jitter	0.200	ns
PLL duty ratio	47.000	%
Clock skew	0.100	ns

Table 2-76 Parameters for the DDR3-1600 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.2	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.2	tCK
Setup time, DQ/DM to DQS	tDS	0.025	ns
Hold time, DQ/DM to DQS	tDH	0.100	ns
Skew between DQS and DQ	tDQSQ	0.150	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.125	ns
Hold time, ADDR/CMD to DDR clock	tIH	0.200	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.300	ns

2.10.2 SFC Interface Timings

Figure 2-7 shows the SFC input timing.

Figure 2-15 SFC input timing

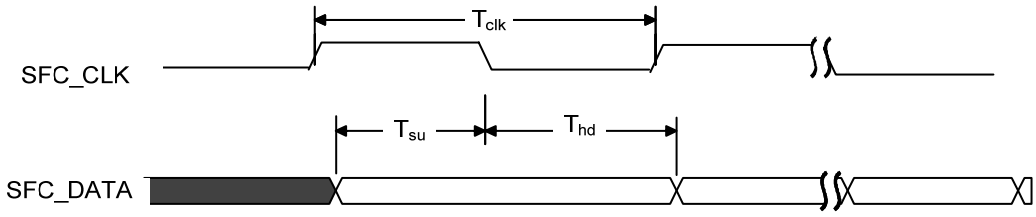


Table 2-77 describes the SFC input timing parameters.

Table 2-77 SFC input timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK	T_{clk}	13	None	83.2	ns
Input signal setup time	T_{su}	6	None	None	ns
Input signal hold time	T_{hd}	1.1	None	None	ns

Figure 2-8 shows the SFC output timing.

Figure 2-16 SFC output timing

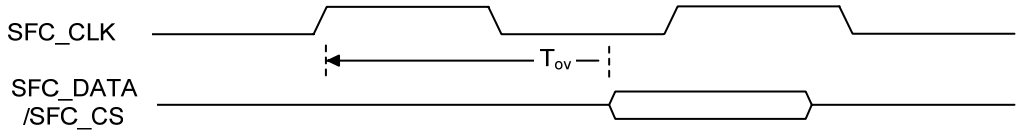


Table 2-78 describes the SFC output timing parameters.

Table 2-78 SFC output timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFCCLK	T	13.3	None	83.2	ns
Output data signal delay	T_{ov}	0	None	6.3	ns
Output CS signal delay	T_{ov}	0	None	6.3	ns

2.10.3 Ethernet MAC Port Timings

2.10.3.1 MII Timings

The Hi3521A provides standard MIIs that comply with the MII timing standard. These interfaces are used to connect to the physical layer (PHY).

Figure 2-9 shows the 100 Mbit/s RX timing of the MII.

Figure 2-17 100 Mbit/s RX timing of the MII

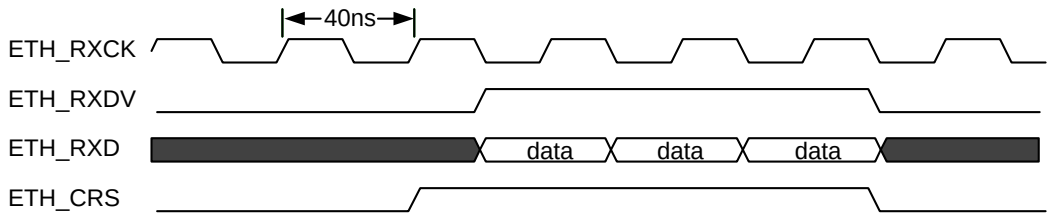


Figure 2-10 shows the 100 Mbit/s TX timing of the MII.

Figure 2-18 100 Mbit/s TX timing of the MII

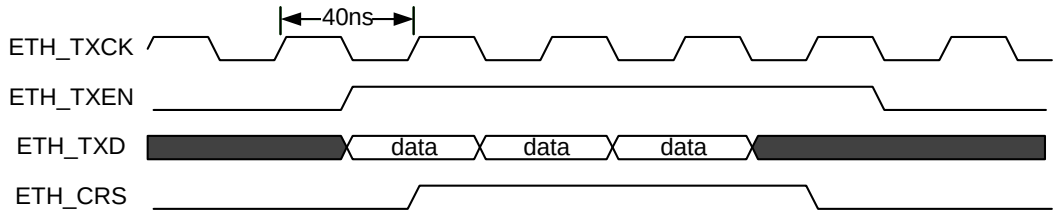


Figure 2-11 shows the 10 Mbit/s RX timing of the MII.

Figure 2-19 10 Mbit/s RX timing of the MII

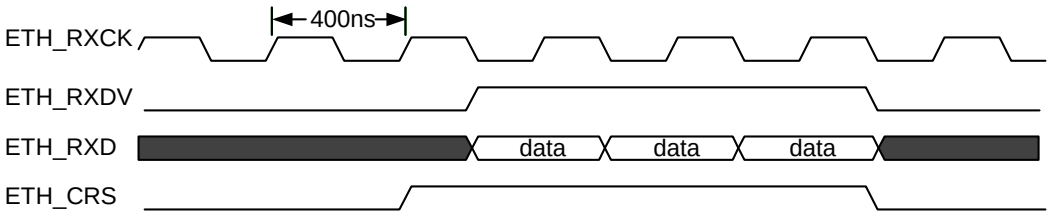


Figure 2-12 shows the 10 Mbit/s TX timing of the MII.

Figure 2-20 10 Mbit/s TX timing of the MII

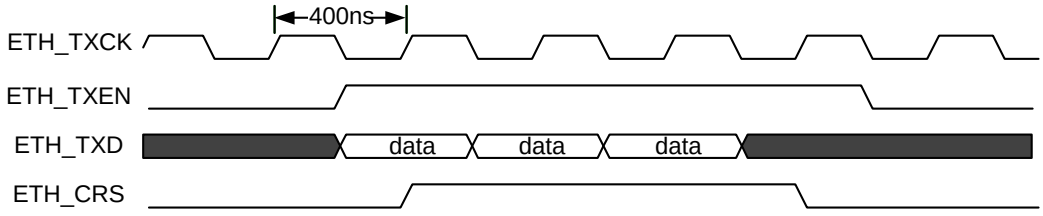


Figure 2-13 shows the RX timing parameters of the MII.

Figure 2-21 RX timing parameters of the MII

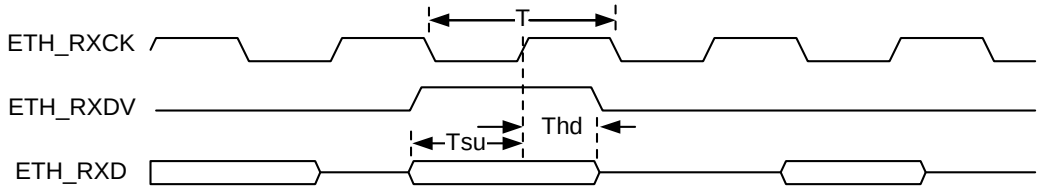


Figure 2-14 shows the TX timing parameters of the MII.

Figure 2-22 TX timing parameters of the MII

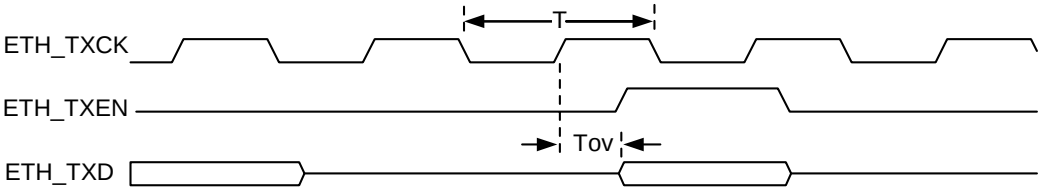


Table 2-79 describes the MII timing parameters.

Table 2-79 MII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
MII clock cycle	T	RGMII_RXC, RGMII_TXCK	400 (10 Mbit/s)	400	ns
			40 (100 Mbit/s)	40	
MII signal setup time	Tsu (RX)	RGMII_RXE, RGMII_RXD, RGMII_RXD[3:0], RGMII_RGMII_CRS, RGMII_RGMII_COL	10	None	ns

Parameter	Symbol	Signal	Min	Max	Unit
MII signal hold time	Thd (RX)	RGMII_RXE, RGMII_RXDV, RGMII_RXD[3:0], RGMII_RGMII_CRS, RGMII_RGMII_COL	10	None	ns
MII output signal delay	Tov (MIITX)	RGMII_TXD[3:0], RGMII_TXE, RGMII_TXER	0	25	ns

2.10.3.2 RMII Timings

Figure 2-15 shows the 100 Mbit/s RX timing of the RMII.

Figure 2-23 100 Mbit/s RX timing of the RMII

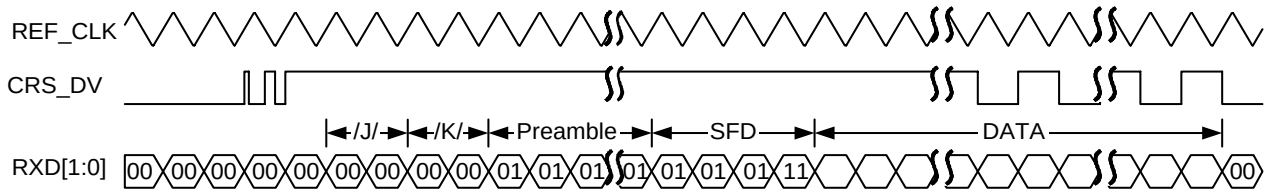


Figure 2-16 shows the 100 Mbit/s TX timing of the RMII interface.

Figure 2-24 100 Mbit/s TX timing of the RMII

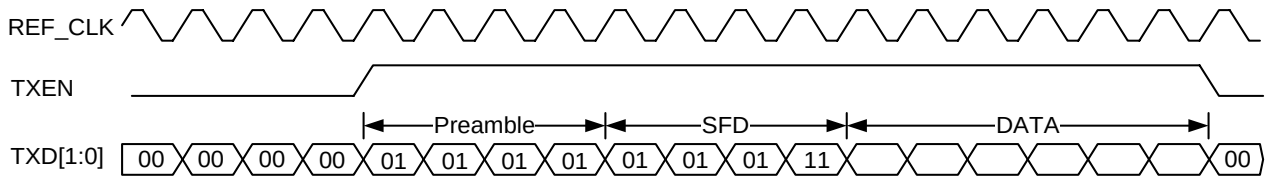


Figure 2-17 shows the 10 Mbit/s RX timing of the RMII.

Figure 2-25 10 Mbit/s RX timing of the RMII

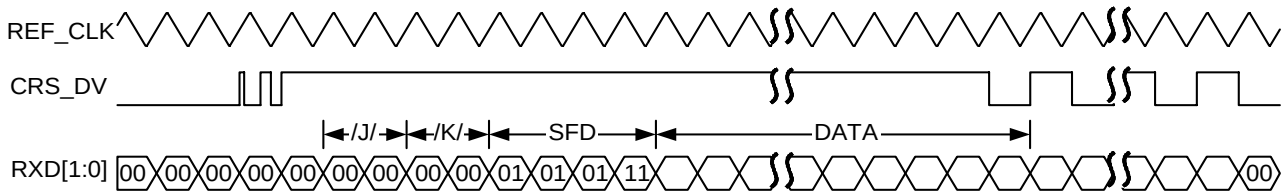


Figure 2-18 shows the 10 Mbit/s TX timing of the RMII.

Figure 2-26 10 Mbit/s TX timing of the RMII

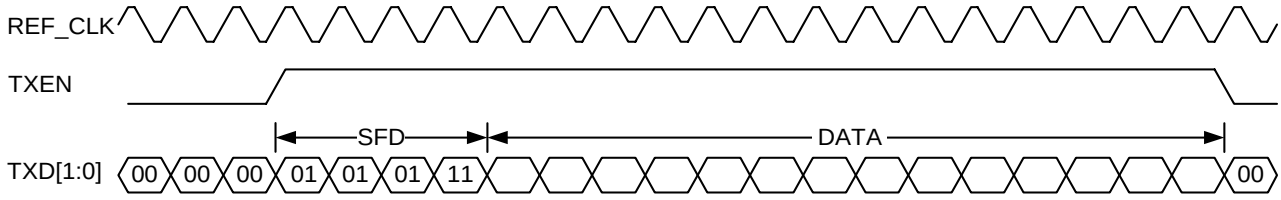


Figure 2-19 shows the timing parameters of the RMII.

Figure 2-27 Timing parameters of the RMII

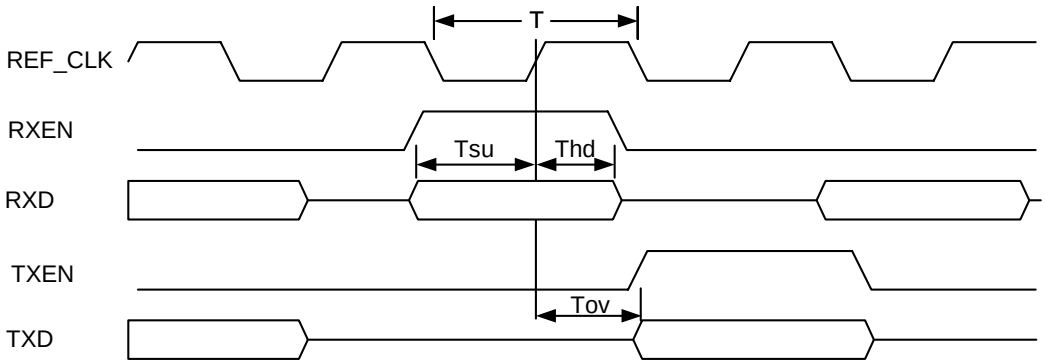


Table 2-80 describes the RMII timing parameters of the RMII.

Table 2-80 Timing parameters of the RMII

Parameter	Symbol	Signal	Min	Max	Unit
RMII clock cycle	T	RGMII_TXCKOUT	20	20	ns
Setup time of RMII signal	Tsu (RX)	RGMII_RXDV, RGMII_RXD[1:0], RGMII_RXER	4	None	ns
Hold time of RMII signal	Thd (RX)	RGMII_RXDV, RGMII_RXD[1:0], RGMII_RXER	2	None	ns

Parameter	Symbol	Signal	Min	Max	Unit
RMII output signal delay	Tov (TX)	RGMII_TXEN, RGMII_TXD[1:0]	3	16	ns

2.10.3.3 RGMII Timings

Figure 2-20 shows the 1000 Mbit/s RX timing of the RGMII.

Figure 2-28 1000 Mbit/s RX timing of the RGMII

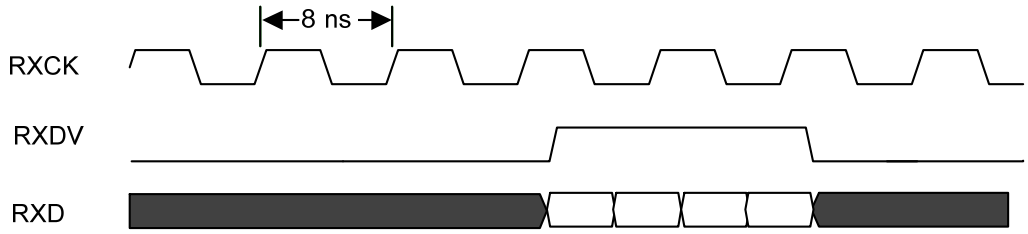


Figure 2-21 shows the 1000 Mbit/s TX timing of the RGMII.

Figure 2-29 1000 Mbit/s TX timing of the RGMII

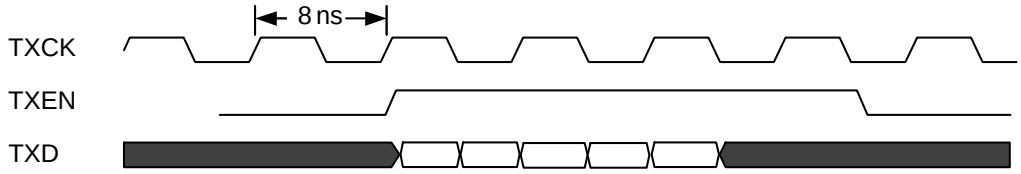


Table 2-81 describes the timing parameters of the RGMII.

Table 2-81 Timing parameters of the RGMII

Parameter	Symbol	Signal	Min	Max	Unit
RGMII clock cycle	T	RGMII_RXCK, RGMII_TXCK	8	8	ns
RGMII signal setup time	Tsu (RX)	RGMII_RXDV, RGMII_RXD[3:0]	1	None	ns
RGMII signal hold time	Thd (RX)	RGMII_RXDV, RGMII_RXD[3:0]	1	None	ns
RGMII output signal delay	Tov (TX)	RGMII_TXD[3:0], RGMII_TXEN	-0.5	0.5	ns

2.10.3.4 MDIO Interface Timings

Figure 2-22 shows the read timing of the MDIO interface.

Figure 2-30 Read timing of the MDIO interface

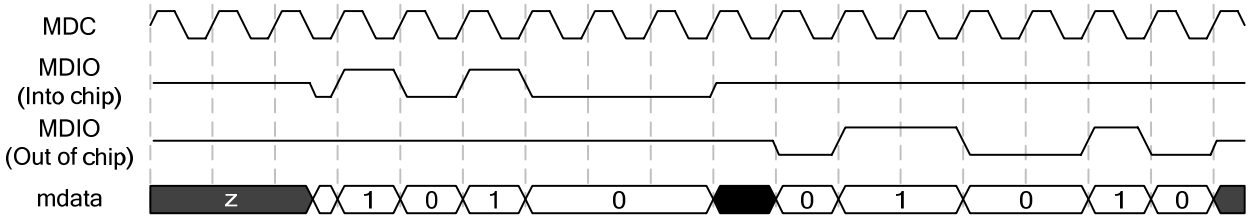


Figure 2-23 shows the write timing of the MDIO interface.

Figure 2-31 Write timing of the MDIO interface

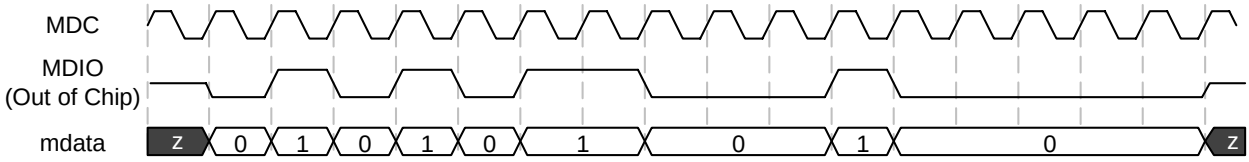


Figure 2-24 shows the RX timing parameters of the MDIO interface.

Figure 2-32 RX timing parameters of the MDIO interface

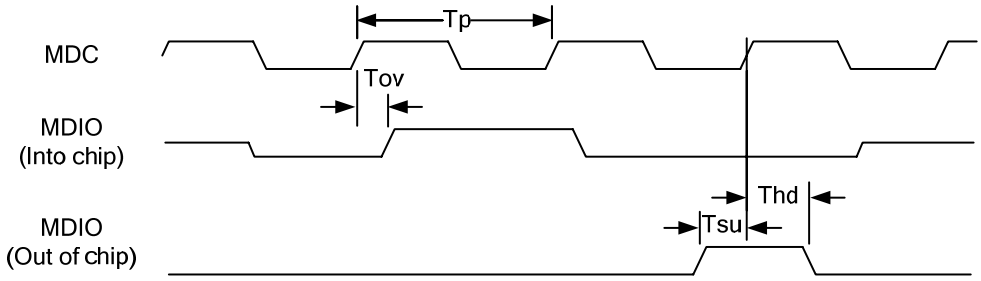


Table 2-82 describes the timing parameters of the MDIO interface.

Table 2-82 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data RX delay	Tov	MDIO	0	300	ns
MDIO clock cycle	Tp	MDCK	400	400	ns
MDIO data TX setup time	Tsu	MDIO	10	None	ns
MDIO data TX hold time	Thd	MDIO	10	None	ns

2.10.4 VI Interface Timing

Figure 2-25 shows the VI interface timing in single-edge mode.

Figure 2-33 VI interface timing in single-edge mode

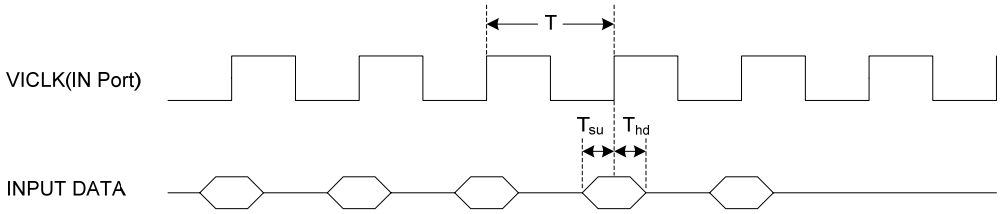


Table 2-83 describes the VI interface timing parameters.

Table 2-83 VI interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.73	None	None	ns
Input signal setup time	T_{su}	4.43	None	None	ns
Input signal hold time	T_{hd}	0.5	None	None	ns

Table 2-84 describes the VI interface timing parameters in dual-edge mode.

Table 2-84 VI interface timing parameters in dual-edge mode

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.73	-	-	ns
Input signal setup time	T_{su}	1	-	-	ns
Input signal hold time	T_{hd}	0.5	-	-	ns
duty cycle requirement	-	47.5	50	52.5	%

2.10.5 AIAO Interface Timings

2.10.5.1 I²S Interface Timing

Figure 2-26 shows the RX timing of the I^2S interface.

Figure 2-34 RX timing of the I²S interface

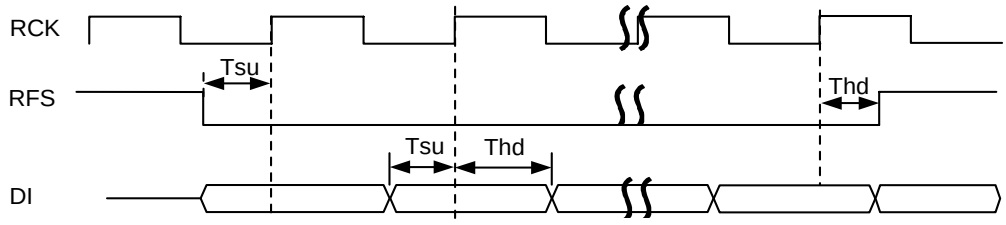


Figure 2-27 shows the TX timing of the I²S interface.

Figure 2-35 TX timing of the I²S interface

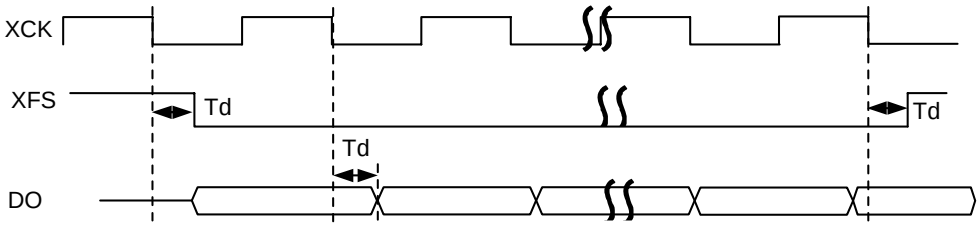


Table 2-85 describes the timing parameters of the I²S interface.

Table 2-85 Timing parameters of the I²S interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

2.10.5.2 PCM Interface Timings

Figure 2-28 shows the RX timing of the PCM interface.

Figure 2-36 RX timing of the PCM interface

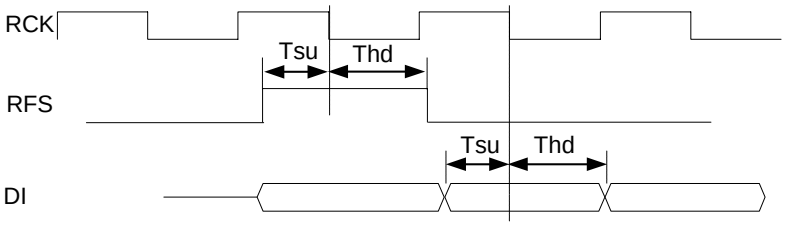


Figure 2-29 shows the TX timing of the PCM interface

Figure 2-37 TX timing of the PCM interface

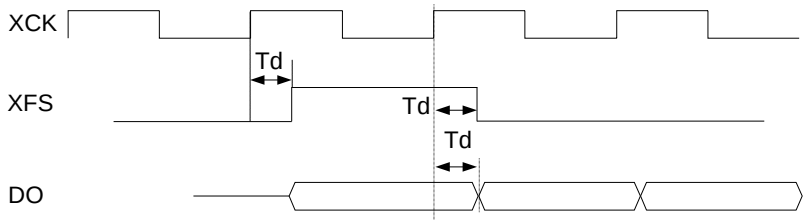


Table 2-86 describes the timing parameters of the PCM interface.

Table 2-86 Timing parameters of the PCM interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	None	None	ns
Input signal hold time	T_{hd}	10	None	None	ns
Output signal delay	T_d	0	None	8	ns

2.10.6 I²C Interface Timing

Figure 2-30 shows the I²C transfer timing.

Figure 2-38 I²C transfer timing

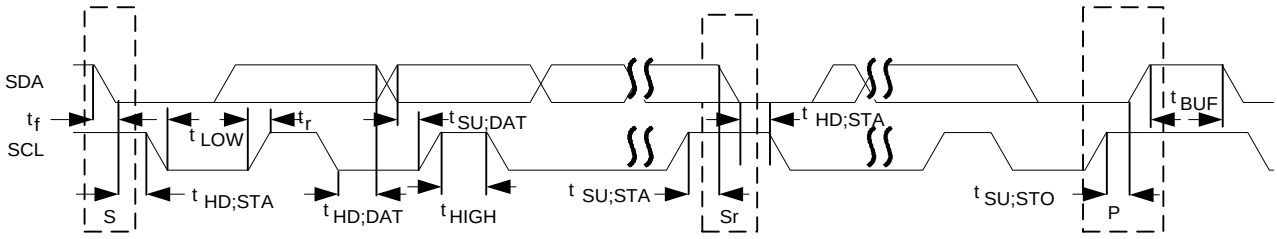


Table 2-87 describes the timing parameters of the I²C interface.

Table 2-87 Timing parameters of the I²C interface

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz
Start hold time	$t_{HD;STA}$	4.0	None	0.6	None	µs
SCL low-level cycle	t_{LOW}	4.7	None	1.3	None	µs

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL high-level cycle	t_{HIGH}	4.0	None	0.6	None	µs
Start setup time	$t_{SU;STA}$	4.7	None	0.6	None	µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU;DAT}$	250	None	100	None	ns
Serial data (SDA) and SCL rising time	t_r	None	1000	20 + 0.1 x C_b	300	ns
SDA and SCL falling time	t_f	None	300	20 + 0.1 x C_b	300	ns
End setup time	$t_{SU;STO}$	4.0	None	0.6	None	µs
Bus release time from start to end	t_{BUF}	4.7	None	1.3	None	µs
Bus load	C_b	None	400	None	400	pF
Low-level noise tolerance	V_{nL}	0.1 x V_{DD}	None	0.1 x V_{DD}	None	V
High-level noise tolerance	V_{nH}	0.2 x V_{DD}	None	0.2 x V_{DD}	None	V

2.10.7 SPI Timings

NOTE

In Figure Figure 2-31 to Figure 2-33, the conventions are as follows:

- MSB = most significant bit
- LSB = least significant bit
- SPI_CK(0):spo = 0
- SPI_CK(1):spo = 1

Figure 2-31 shows the SPI clock (SPICK) timing.

Figure 2-39 SPICK timing

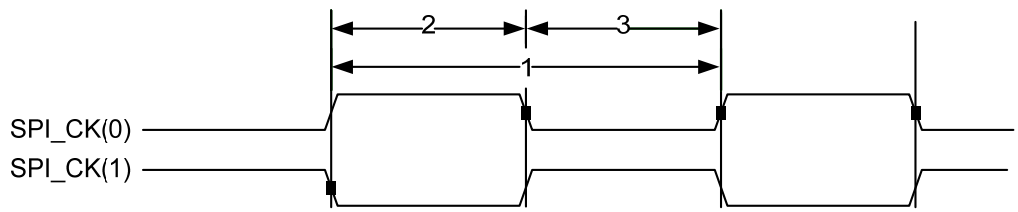


Figure 2-32 and Figure 2-33 show the SPI timings in master mode.

Figure 2-40 SPI timing in master mode (sph = 0)

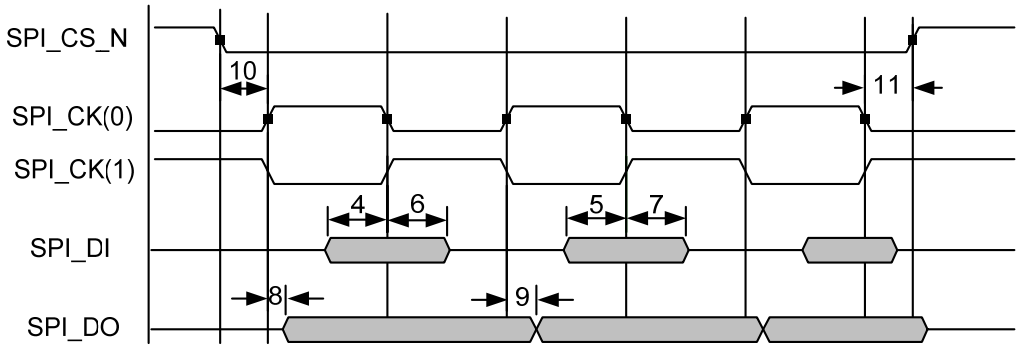


Figure 2-41 SPI timing in master mode (sph = 1)

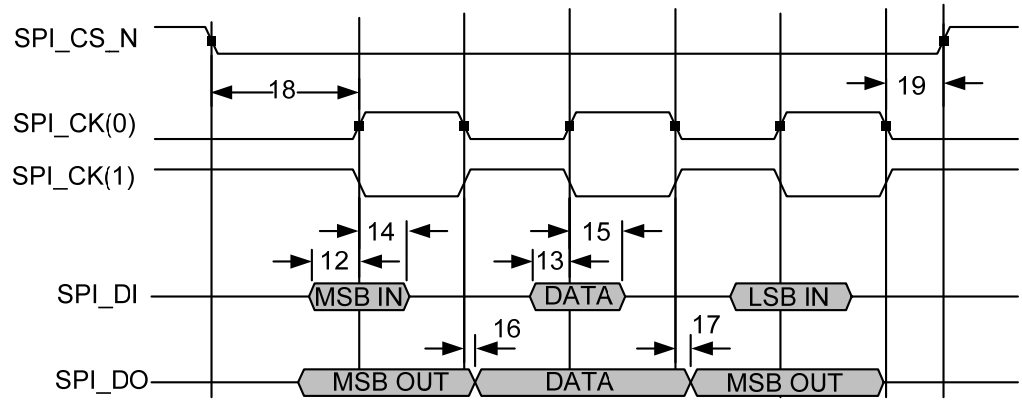


Table 2-88 describes the SPI timing parameters.

Table 2-88 SPI timing parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_CK	tc	None	None	None	ns
2	Pulse duration, SPI_CK high (all master modes)	tw1	None	None	None	ns
3	Pulse duration. SPI_CK low (all master modes)	tw2	None	None	None	ns
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	None	None	None	ns
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	None	None	None	ns
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	None	None	None	ns
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	None	None	None	ns

No.	Parameter	Symbol	Min	Typ	Max	Unit
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	None	None	None	ns
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	None	None	None	ns
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	None	None	None	ns
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	None	None	None	ns
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	None	None	None	ns
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	None	None	None	ns
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	None	None	None	ns
15	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th4	None	None	None	ns
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	None	None	None	ns
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	None	None	None	ns
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	None	None	None	ns
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	None	None	None	ns

Contents

Figures

Tables

3 System

3.1 Reset

3.1.1 Overview

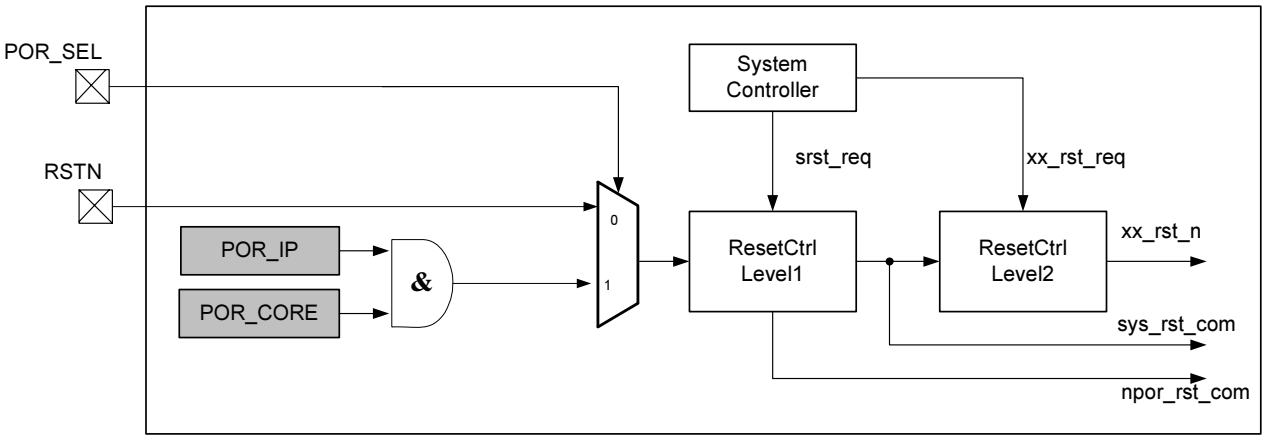
The reset management module resets the entire chip and all functional modules in a unified manner as follows:

- Manages and controls power-on reset (POR).
- Controls the system soft reset and the separate soft reset of each functional module.
- Synchronizes reset signals to the clock domain corresponding to each module.
- Generates reset signals for each internal functional module.

3.1.2 Reset Control

Figure 3-1 shows the diagram of controlling reset signals.

Figure 3-1 Diagram of controlling reset signals



NOTE

- RSTN: POR signal. This signal is derived from the input pin RSTN of the chip.
- POR_CORE, POR_IP: internal POR module

- POR_SEL: POR selection
- srst_req: global soft reset request signal. This signal is derived from the system controller.
- xx_rst_req: separate soft reset request signal of each submodule. This signal is derived from the clock and reset generator (CRG) system controller.
- xx_rst_n, sys_rst_com, and npor_rst_com: reset signals.

Table 3-1 Types of reset signals

Type	Generation Mode	Function
Global hard reset signal (npor)	Derived from RSTN or the internal POR module.	Globally resets the entire Hi3521A.
Global soft reset signal (sys_rst_n)	Derived from the global soft reset register of the software configuration system controller.	Globally resets all the modules of the Hi3521A, excluding the clock reset circuits, test circuits, and registers that do not support soft reset
Submodule reset signal (xx_rst_n)	Derived from the submodule reset control register of the CRG system controller.	Separately resets each submodule of the Hi3521A.

3.1.3 Reset Configuration

POR

To implement POR, the following conditions must be met:

- The POR input pin or internal POR module generates a low-level pulse, and the low pulse duration is greater than 130 ms.
- The clock input by the XIN pin of the crystal oscillator clock works properly.

System Reset

The system is reset in either of the following ways:

- POR
- Global soft reset, controlled by the system controller

Soft Reset

The soft reset is controlled by configuring the corresponding system controller. For details about configurations, see the description of the reset register for each module.

CAUTION

- After a system soft reset request is sent, the circuit reset is deasserted after at least 130 system clock cycles.
- The separate soft reset of each module is not automatically deasserted. For example, if a module is reset after 1 is written to the related bit, the reset of this module is deasserted only when the related bit is set to 0.

3.2 Clock

3.2.1 Overview

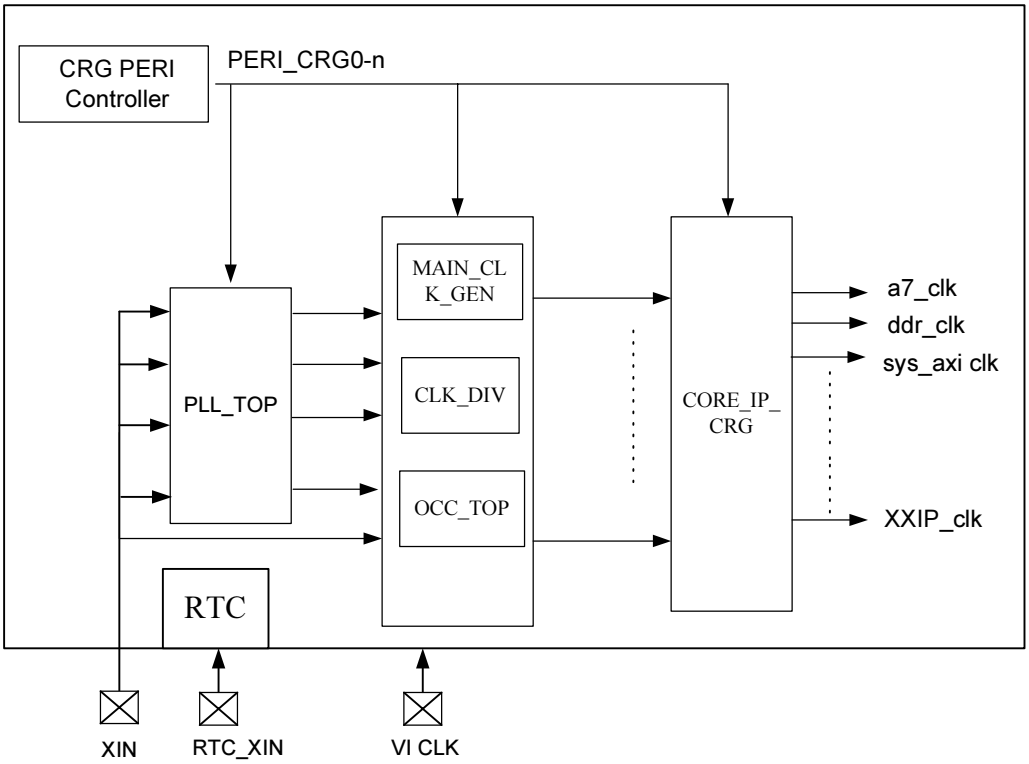
The CRG manages clock input, clock generation, and clock control in a unified manner as follows:

- Manages and controls clock inputs
- Divides and controls clock frequencies
- Generates working clocks for each module

3.2.2 Clock Control Block Diagram

Figure 3-2 shows the functional block diagram of the CRG.

Figure 3-2 Functional block diagram of the CRG



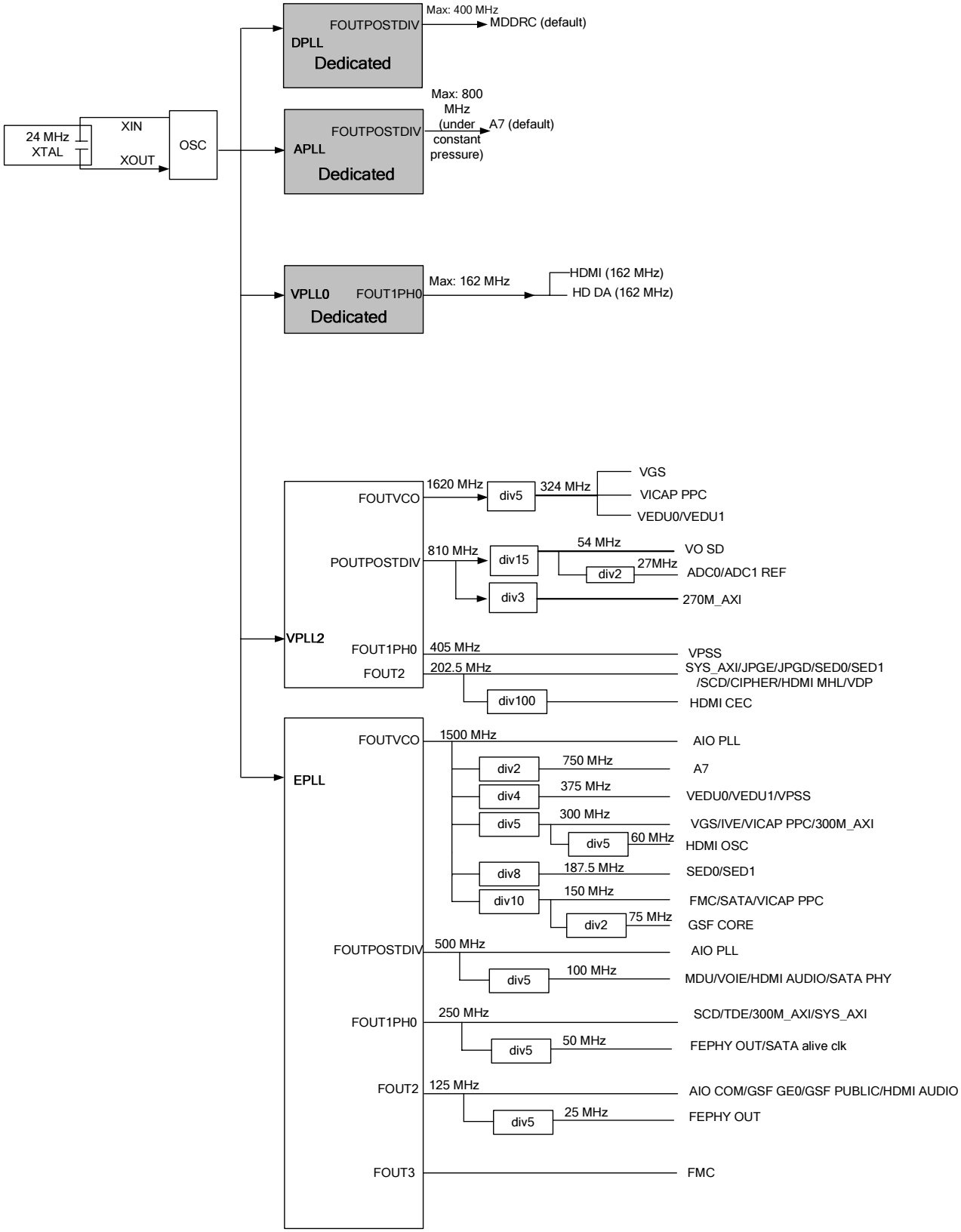
NOTE

XIN is the PLL input clock and is always connected to a 24 MHz crystal, whereas RTC_XIN is the RTC input clock and is always connected to a 32.768 kHz crystal.

3.2.3 Clock Distribution

The CRG configures, controls, and manages the internal PLLs and input clocks from pins. It also generates the clocks required by each module. Figure 3-3 shows the clock distribution diagram.

Figure 3-3 Clock distribution diagram



NOTE

The frequencies of APLL, VPLL0, and DPLL in gray can be configured by programming, whereas the frequencies of other PLLs are fixed. The frequencies marked with "Default" indicate default PLL frequencies.

3.2.4 PLL Configuration

The Hi3521A has five internal PLLs. Each PLL uses two configuration registers. See Table 3-2.

Table 3-2 Configuration registers corresponding to PLLs

PLL	Configuration Register 1	Configuration Register 0
APLL	PERI_CRG_PLL0	PERI_CRG_PLL 1
VPLL0	PERI_CRG_PLL 2	PERI_CRG_PLL 3
VPLL2	PERI_CRG_PLL 4	PERI_CRG_PLL 5
EPLL	PERI_CRG_PLL 6	PERI_CRG_PLL 7
DPLL	PERI_CRG_PLL 8	PERI_CRG_PLL 9

All PLLs use the input crystal oscillator clock of the XIN pin as the input clock. For details on how to calculate PLL output frequencies, see Table 3-3.

Table 3-3 Methods of calculating PLL output frequencies

PLL Pin	Formula	Remarks
FREF	PLL input reference clock	The input clock must be 24 MHz.
FOUTVCO	FREF x (fbdiv + frac/2^24)/refdiv	
FOUTPOSTDIV	FOUTVCO/(pstdiv1 x pstdiv2)	None
FOUT1ph0	FOUTVCO/(pstdiv1 x pstdiv2 x 2)	None
FOUT2	FOUTVCO/(pstdiv1 x pstdiv2 x 4)	None
FOUT3	FOUTVCO/(pstdiv1 x pstdiv2 x 6)	None

PLL Pin	Formula	Remarks
FOUT4	FOUTVCO/(pstdiv1 x pstdiv2 x 8)	None

NOTE

- fbdiv: integral frequency multiplier
- frac: decimal frequency multiplier
- refdiv: frequency divider of the reference clock
- pstdiv1: level-1 output frequency divider
- pstdiv2: level-2 output frequency divider

For details about the frequency multiplier and divider of each PLL, see Table 3-2.

The following uses VPLL0 as an example. If VPLL0 outputs the 162 MHz FOUT1PH0 clock to the VDP module, the configured values of the register are calculated as follows:

- If postdiv2 is 5 and postdiv1 is 1, the value of FOUTVCO is 1620 MHz based on the following formula:

  FOUT1PH0 = FOUTVCO/(pstdiv1 x pstdiv2 x 2)
- If refdiv is 2, fbdiv and frac can be calculated based on the following formula:

  FOUTVCO = FREF x (fbdiv + frac/2^24)/refdiv = 24 x (fbdiv + frac/2^24)/2 = 1620 MHz

  That is, fbdiv = 135 and frac = 000000

3.2.5 Frequency Configurations

Frequency Configurations of A7/DDR/Bus Clocks

Table 3-4 describes the frequency configurations of A7/DDR/graphics processing unit /bus clocks.

Table 3-4 Frequency configurations of A7/DDR/bus clocks

Signal	Description
ddr_cksel	PERI_CRG13 bit[1:0]
cpu_cksel	PERI_CRG13 bit[3:2]
bus_cksel	PERI_CRG13 bit[13:8]

Frequency Configurations of Module Clocks

Table 3-5 describes the frequency configurations of clocks for each module.

Table 3-5 Frequency configurations of clocks for each module

Signal	Description
Frequency configurations of VICAP	
vi0_pctrl	PERI_CRG11 bit[1]

Signal	Description
vi0_ch_cksel	PERI_CRG11 bit[2]
vi1_pctrl	PERI_CRG11 bit[5]
vi1_ch_cksel	PERI_CRG11 bit[6]
vi2_pctrl	PERI_CRG11 bit[9]
vi2_ch_cksel	PERI_CRG11 bit[10]
vi3_pctrl	PERI_CRG11 bit[13]
vi3_ch_cksel	PERI_CRG11 bit[14]
vi_ppc_cksel	PERI_CRG11 bit[30:29]
Frequency configurations of VDP	
vohd_out_pctrl	PERI_CRG12 bit[12]
vosd_out_pctrl	PERI_CRG12 bit[13]
vohd_cksel	PERI_CRG12 bit[14]
vosd_cksel	PERI_CRG12 bit[15]
Frequency configurations of HDMI TX	
hdmitx_ctrl_cec_clk_sel	PERI_CRG14 bit[12]
hdmitx_asin_cksel	PERI_CRG14 bit[13]
hdmitx_ctrl_asclk_sel	PERI_CRG14 bit[14]
Frequency configurations of VEDU0	
vedu0_cksel	PERI_CRG15 bit[2]
sed0_cksel	PERI_CRG15 bit[3]
vedu0clk_skipcfg	PERI_CRG15 bit[8:4]
vedu0clk_loaden	PERI_CRG15 bit[9]
Frequency configurations of VEDU1	
vedu1_cksel	PERI_CRG16 bit[2]
sed1_cksel	PERI_CRG16 bit[3]
vedu1clk_skipcfg	PERI_CRG16 bit[8:4]
vedu1clk_loaden	PERI_CRG16 bit[9]
Frequency configurations of video processing subsystem (VPSS)	
vps_cksel	PERI_CRG17 bit[3:2]
vpsclk_loaden	PERI_CRG17 bit[9]
vpsclk_skipcfg	PERI_CRG17 bit[8:4]

Signal	Description
Frequency configurations of two-dimensional engine (TDE)	
tdeclk_loaden	PERI_CRG18 bit[9]
tdeclk_skipcfg	PERI_CRG18 bit[8:4]
Frequency configurations of video graphics subsystem (VGS)	
vgs_cksel	PERI_CRG19 bit[2]
vgsclk_loaden	PERI_CRG19 bit[9]
vgsclk_skipcfg	PERI_CRG19 bit[8:4]
Frequency configurations of JPGE/VOIE	
jpgeclk_loaden	PERI_CRG20 bit[9]
jpgeclk_skipcfg	PERI_CRG20 bit[8:4]
voieclk_loaden	PERI_CRG20 bit[25]
voieclk_skipcfg	PERI_CRG20 bit[24:20]
Frequency configurations of JPGD	
jpgdclk_loaden	PERI_CRG21 bit[9]
jpgdclk_skipcfg	PERI_CRG21 bit[8:4]
Frequency configurations of MDU	
mduclk_loaden	PERI_CRG22 bit[9]
mduclk_skipcfg	PERI_CRG22 bit[8:4]
Frequency configurations of AIAO	
aiao_cksel	PERI_CRG25 bit[3:2]
Frequency configurations of SATA PHY	
sata_phy0_refclk_sel	PERI_CRG26 bit[1]
sata_phy1_refclk_sel	PERI_CRG26 bit[3]
Frequency configurations of FMC	
fmc_cksel	PERI_CRG29 bit[3:2]
Frequency configurations of GMAC	
rmii_cksel	PERI_CRG30 bit[4]
ext_fephy_cksel	PERI_CRG30 bit[6]
gsf_cksel	PERI_CRG30 bit[7]
Frequency configurations of UART	
uart_cksel	PERI_CRG33 bit[19:18]

Signal	Description
Frequency configurations of VPLL0 spread spectrum configuration register	
vpll0_ssmod_cfg	PERI_CRG37 bit[11:0]
Frequency configurations of VPLL2 spread spectrum configuration register	
vpll2_ssmod_cfg	PERI_CRG38 bit[11:0]
Frequency configurations of APLL spread spectrum configuration register	
apll_ssmod_cfg	PERI_CRG39 bit[11:0]
Frequency configurations of EPLL spread spectrum configuration register	
epll_ssmod_cfg	PERI_CRG40 bit[11:0]
Frequency configurations of DPLL spread spectrum configuration register	
dpll_ssmod_cfg	PERI_CRG46 bit[11:0]
Frequency configurations of ADC REF0/REF1	
adc_ref0_cksel	PERI_CRG45 bit[1:0]
adc_ref1_cksel	PERI_CRG45 bit[3:2]

Precautions

Take the following precautions when configuring clocks:

- By default, the A7/DDR/bus working clock is in crystal oscillator mode after power-on. That is, the crystal oscillator clock input by the XIN pin is selected.
- If the frequency of the PLL is changed, the PLL can output a stable clock 0.1 ms later. The frequency of the PLL can be changed only when the system working clock is in crystal oscillator mode.
- If the PLL output clock is not stable, the system mode cannot be switched to PLL mode. You can view the PLL lock bit to check whether the PLL is locked. The status of the PLL lock bit can be obtained by reading PERI_CRG34 bit[4:0].

3.2.6 CRG Register Summary

Table 3-6 describes CRG registers.

Table 3-6 Summary of CRG registers (base address: 0x1204_0000)

Offset Address	Register	Description	Page
0x0000	PERI_CRG_PLL0	APLL configuration register 0	3-13
0x0004	PERI_CRG_PLL1	APLL configuration register 1	3-13

Offset Address	Register	Description	Page
0x0008	PERI_CRG_PLL2	VPLL0 configuration register 0	3-14
0x000C	PERI_CRG_PLL3	VPLL0 configuration register 1	3-15
0x0010	PERI_CRG_PLL4	VPLL2 configuration register 0	3-16
0x0014	PERI_CRG_PLL5	VPLL2 configuration register 1	3-16
0x0018	PERI_CRG_PLL6	EPLL1 configuration register 0	3-18
0x001C	PERI_CRG_PLL7	EPLL1 configuration register 1	3-18
0x0020	PERI_CRG_PLL8	DPLL configuration register 0	3-19
0x0024	PERI_CRG_PLL9	DPLL configuration register 1	3-20
0x0028	PERI_CRG10	A7 frequency mode and reset configuration register	3-21
0x002C	PERI_CRG11	VICAP clock and reset configuration register	3-23
0x0030	PERI_CRG12	Video output unit (VOU) clock and reset control register	3-25
0x0034	PERI_CRG13	SoC/DDR clock configuration register	3-27
0x0038	PERI_CRG14	HDMI clock and reset control register	3-28
0x003C	PERI_CRG15	VEDU0 clock and soft reset control register	3-30
0x0040	PERI_CRG16	VEDU1 clock and soft reset control register	3-31
0x0044	PERI_CRG17	VPSS clock and soft reset control register	3-33
0x0048	PERI_CRG18	TDE clock and soft reset control register	3-34
0x004C	PERI_CRG19	VGS clock and soft reset control register	3-34
0x0050	PERI_CRG20	JPGE/VOIE clock and soft reset control register	3-35
0x0054	PERI_CRG21	JPGD clock and soft reset control register	3-37
0x0058	PERI_CRG22	MDU clock and soft reset control register	3-38
0x005C	PERI_CRG23	IVE clock and soft reset control register	3-38
0x0060	PERI_CRG24	Cipher clock and soft reset control register	3-39

Offset Address	Register	Description	Page
0x0064	PERI_CRG25	AIAO clock and reset control register	3-40
0x0068	PERI_CRG26	SATA PHY clock and reset control register	3-40
0x006C	PERI_CRG27	SATA controller clock and reset control register	3-41
0x0070	PERI_CRG28	USB clock and soft reset control register	3-43
0x0074	PERI_CRG29	FMC clock and soft reset control register	3-44
0x0078	PERI_CRG30	GSF/GMAC/FEPHY clock and soft reset control register	3-45
0x007C	PERI_CRG31	SCD clock and soft reset control register	3-46
0x0080	PERI_CRG32	DMA/DDRTEST clock and soft reset control register	3-47
0x0084	PERI_CRG33	APB peripheral clock and reset control register	3-47
0x0088	PERI_CRG34	CRG status register	3-49
0x008C	PERI_CRG35	GMAC interface control register	3-50
0x0090	PERI_CRG36	GMAC interface status register	3-52
0x0094	PERI_CRG37	VPLL0 spread spectrum configuration register	3-52
0x0098	PERI_CRG38	VPLL2 spread spectrum configuration register	3-53
0x009C	PERI_CRG39	APLL spread spectrum configuration register	3-54
0x00A0	PERI_CRG40	EPLL spread spectrum configuration register	3-55
0x00A4	PERI_CRG41	DLL0 control and status register	3-56
0x00A8	PERI_CRG42	DLL1 control and status register	3-58
0x00AC	PERI_CRG43	DLL2 control and status register	3-59
0x00B0	PERI_CRG44	DLL3 control and status register	3-60
0x00B4	PERI_CRG45	ADC REF0/REF1 clock configuration register	3-62
0x00B8	PERI_CRG46	DPLL spread spectrum configuration register	3-63

3.2.7 Register Description

PERI_CRG_PLL0

PERI_CRG_PLL0 is APLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_CRG_PLL0	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	apll_postdiv2			reserved	apll_postdiv1			apll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	apll_postdiv2	Level-2 output divider of the APLL
[27]	RO	reserved	Reserved
[26:24]	RW	apll_postdiv1	Level-1 output divider of the APLL
[23:0]	RW	apll_frac	Decimal divider of the APLL

PERI_CRG_PLL1

PERI_CRG_PLL1 is APLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_CRG_PLL1	0x0200_3064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				apll_bypass	apll_dacpd	apll_dsmpd	apll_pd	apll_foutvcopd	apll_postdivpd	apll_fout4phasepd	reserved				apll_refdiv					apll_fbdiv											
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26]	RW	apll_bypass	APLL clock frequency-division bypass control 0: not bypassed 1: bypassed
[25]	RW	apll_dacpd	APLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	apll_dsmpd	APLL decimal frequency-division control 0: decimal frequency-division mode 1: integer frequency-division mode
[23]	RW	apll_pd	APLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	apll_foutvcopd	Power-down control for the APLL VCO output 0: normal output clock 1: no output clock
[21]	RW	apll_postdivpd	Power-down control for the APLL POSTDIV output 0: normal output clock 1: no output clock
[20]	RW	apll_fout4phasepd	Power-down control for the APLL FOUT output 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	apll_refdiv	Divider of the APLL reference clock
[11:0]	RW	apll_fbdiv	Integral multiplier of the APLL

PERI_CRG_PLL2

PERI_CRG_PLL2 is VPLL0 configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0008	PERI_CRG_PLL2	0x5100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	vpll0_postdiv2			reserved	vpll0_postdiv1			vpll0_frac																							

Reset	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	vpll0_postdiv2	Level-2 output divider of the VPLL0
[27]	RO	reserved	Reserved
[26:24]	RW	vpll0_postdiv1	Level-1 output divider of the VPLL0
[23:0]	RW	vpll0_frac	Decimal divider of the VPLL0

PERI_CRG_PLL3

PERI_CRG_PLL3 is VPLL0 configuration register 1.

Offset Address	Register Name	Total Reset Value
0x000C	PERI_CRG_PLL3	0x0200_2087

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					vpll0_bypass	vpll0_dacpd	vpll0_dsmpd	vpll0_pd	vpll0_foutvcopd	vpll0_postdivpd	vpll0_fout4phasepd	reserved				vpll0_refdiv				vpll0_fbdiv											
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RW	vpll0_bypass	VPLL0 clock frequency-division bypass control 0: not bypassed 1: bypassed
[25]	RW	vpll0_dacpd	VPLL0 test signal control 0: normal operating mode 1: power-down mode
[24]	RW	vpll0_dsmpd	VPLL0 decimal frequency-division control 0: decimal frequency-division mode 1: integer frequency-division mode
[23]	RW	vpll0_pd	VPLL0 power-down control 0: normal operating mode 1: power-down mode

[22]	RW	vpll0_foutvcopd	Power-down control for the VPLL0 VCO output 0: normal output clock 1: no output clock
[21]	RW	vpll0_postdivpd	Power-down control for the VPLL0 POSTDIV output 0: normal output clock 1: no output clock
[20]	RW	vpll0_fout4phasepd	Power-down control for the VPLL0 FOUT output 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	vpll0_refdiv	Divider of the VPLL0 reference clock
[11:0]	RW	vpll0_fbdiv	Integral multiplier of the VPLL0

PERI_CRG_PLL4

PERI_CRG_PLL4 is VPLL2 configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_CRG_PLL4	0x2100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	vpll2_postdiv2			reserved	vpll2_postdiv1			vpll2_frac																							
Reset	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	vpll2_postdiv2	Level-2 output divider of VPLL2
[27]	RO	reserved	Reserved
[26:24]	RW	vpll2_postdiv1	Level-1 output divider of VPLL2
[23:0]	RW	vpll2_frac	Decimal divider of VPLL2

PERI_CRG_PLL5

PERI_CRG_PLL5 is VPLL2 configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_CRG_PLL5	0x0200_2087

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					vpll2_bypass	vpll2_dacpd	vpll2_dsmpd	vpll2_pd	vpll2_foutvcopd	vpll2_postdivpd	vpll2_fout4phasepd	reserved				vpll2_fbdiv				reserved											
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RW	vpll2_bypass	VPLL2 clock frequency-division bypass control 0: not bypassed 1: bypassed
[25]	RW	vpll2_dacpd	VPLL2 test signal control 0: normal operating mode 1: power-down mode
[24]	RW	vpll2_dsmpd	VPLL2 decimal frequency-division control 0: decimal frequency-division mode 1: integer frequency-division mode
[23]	RW	vpll2_pd	VPLL2 power-down control 0: normal operating mode 1: power-down mode
[22]	RW	vpll2_foutvcopd	Power-down control for the VPLL2 VCO output 0: normal output clock 1: no output clock
[21]	RW	vpll2_postdivpd	Power-down control for the VPLL2 POSTDIV output 0: normal output clock 1: no output clock
[20]	RW	vpll2_fout4phasepd	Power-down control for the VPLL2 FOUT output 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	vpll2_refdiv	Divider of the VPLL2 reference clock
[11:0]	RW	vpll2_fbdiv	Integral multiplier of VPLL2

PERI_CRG_PLL6

PERI_CRG_PLL6 is EPLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0018	PERI_CRG_PLL6	0x3100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	epll_postdiv2			reserved	epll_postdiv1			epll_frac																							
Reset	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	epll_postdiv2	Level-2 output divider of EPLL
[27]	RO	reserved	Reserved
[26:24]	RW	epll_postdiv1	Level-1 output divider of EPLL
[23:0]	RW	epll_frac	Decimal divider of EPLL

PERI_CRG_PLL7

PERI_CRG_PLL7 is EPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x001C	PERI_CRG_PLL7	0x0200_207D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				epll_bypass	epll_dacpd	epll_dsmpd	epll_pd	epll_foutvcopd	epll_postdivpd	epll_fout4phasepd	reserved	epll_refdiv				epll_fbdiv															
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	0	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26]	RW	epll_bypass	EPLL clock frequency-division bypass control 0: not bypassed 1: bypassed
[25]	RW	epll_dacpd	EPLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	epll_dsmpd	EPLL decimal frequency-division control 0: decimal frequency-division mode 1: integer frequency-division mode
[23]	RW	epll_pd	EPLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	epll_foutvcopd	Power-down control for the EPLL VCO output 0: normal output clock 1: no output clock
[21]	RW	epll_postdivpd	Power-down control for the EPLL POSTDIV output 0: normal output clock 1: no output clock
[20]	RW	epll_fout4phasepd	Power-down control for the EPLL FOUT output 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	epll_refdiv	Divider of the EPLL reference clock
[11:0]	RW	epll_fbdiv	Integral multiplier of the EPLL

PERI_CRG_PLL8

PERI_CRG_PLL8 is DPLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_CRG_PLL8	0x1100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		dpll_postdiv2		reserved		dpll_postdiv1		dpll_frac																							

Reset	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	dpll_postdiv2	Level-2 output divider of the DPLL
[27]	RO	reserved	Reserved
[26:24]	RW	dpll_postdiv1	Level-1 output divider of the DPLL
[23:0]	RW	dpll_frac	Decimal divider of the DPLL

PERI_CRG_PLL9

PERI_CRG9 is DPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0024	PERI_CRG_PLL9	0x0200_3032

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					dpll_bypass	dpll_dacpd	dpll_dsmpd	dpll_pd	dpll_foutvcopd	dpll_postdivpd	dpll_fout4phasepd	reserved				dpll_refdiv				dpll_fbdiv											
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RW	dpll_bypass	DPLL clock frequency-division bypass control 0: not bypassed 1: bypassed
[25]	RW	dpll_dacpd	DPLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	dpll_dsmpd	DPLL decimal frequency-division control 0: decimal frequency-division mode 1: integer frequency-division mode
[23]	RW	dpll_pd	DPLL power-down control 0: normal operating mode 1: power-down mode

[22]	RW	dpll_foutvcopd	Power-down control for the DPLL VCO output 0: normal output clock 1: no output clock
[21]	RW	dpll_postdivpd	Power-down control for the EPLL POSTDIV output 0: normal output clock 1: no output clock
[20]	RW	dpll_fout4phasepd	Power-down control for the DPLL FOUT output 0: normal output clock 1: no output clock
[19:18]	RO	reserved	Reserved
[17:12]	RW	dpll_refdiv	Divider of the DPLL reference clock
[11:0]	RW	dpll_fbdiv	Integral multiplier of the DPLL

PERI_CRG10

PERI_CRG10 is an A7 frequency mode and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_CRG10	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				a7_sm_cnt_cfg						a7_sm_bypass_pos	a7_sm_bypass_pre	a7_sm_step_sel		a7clk_loaden		a7clk_skipcfg				reserved	cs_srst_req	socdbg_srst_req	l2_srst_req	etm_srst_req	arm_dbg_srst_req	arm_core_srst_req	reserved				pclkdbg_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:22]	RW	a7_sm_cnt_cfg	Initial value of the SM counter
[21]	RW	a7_sm_bypass_pos	Frequency gradient bypass after clock switching 0: The frequency gradient takes effect. 1: The frequency gradient is bypassed.
[20]	RW	a7_sm_bypass_pre	Frequency gradient bypass before clock switching 0: The frequency gradient takes effect. 1: The frequency gradient is bypassed.

[19:18]	RW	a7_sm_step_sel	Decreasing step select for the SM counter 00: The decreasing step is 1. 01: The decreasing step is 2. 10: The decreasing step is 3. 11: The decreasing step is 4.
[17]	RW	a7clk_loaden	Skip configuration enable for the CPU clock To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to a7clk_loaden. 3. Write 1 to a7clk_loaden.
[16:12]	RW	a7clk_skipcfg	Skip configuration of the CPU clock. N: *N*-beat clocks are disabled every 32-beat CPU clocks.
[11]	RO	reserved	Reserved
[10]	RW	cs_srst_req	Chip select (CS) soft reset 0: deassert reset 1: reset
[9]	RW	socdbg_srst_req	SOCDBG soft reset 0: deassert reset 1: reset
[8]	RW	l2_srst_req	L2 soft reset 0: deassert reset 1: reset
[7]	RW	etm_srst_req	ETM soft reset 0: deassert reset 1: reset
[6]	RW	arm_dbg_srst_req	ARM DBG soft reset 0: deassert reset 1: reset
[5]	RW	arm_core_srst_req	ARM core soft reset 0: deassert reset 1: reset
[4:1]	RO	reserved	Reserved
[0]	RW	pclkdbg_cken	A7 PCLKDBG clock gating 0: The clock is disabled. 1: The clock is enabled.

PERI_CRG11

PERI_CRG11 is a VICAP clock and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_CRG11	0x1FFE_9999

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	vi_ppc_cksel		vi_apb_cken	vi_axi_cken	vi_ppc_cken	vi_bus_srst_req	reserved								vi_ppc_srst_req	vi3_srst_req	vi3_ch_cksel		vi3_pctrl	vi3_cken	vi2_srst_req	vi2_ch_cksel		vi2_pctrl	vi2_cken	vi1_srst_req	vi1_ch_cksel		vi1_pctrl	vi1_cken	vi0_srst_req	vi0_ch_cksel		vi0_pctrl	vi0_cken
Reset	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:29]	RW	vi_ppc_cksel	Frequency select for the VI working clock 0: 300 MHz 1: reserved 2: 150 MHz 3: reserved
[28]	RW	vi_apb_cken	VI APB bus gating 0: The clock is disabled. 1: The clock is enabled.
[27]	RW	vi_axi_cken	VI AXI bus gating 0: The clock is disabled. 1: The clock is enabled.
[26]	RW	vi_ppc_cken	VI PPC gating 0: The clock is disabled. 1: The clock is enabled.
[25]	RW	vi_bus_srst_req	VI PPC bus soft reset 0: deassert reset 1: reset
[24:17]	RO	reserved	Reserved
[16]	RW	vi_ppc_srst_req	VI PPC soft reset 0: deassert reset 1: reset

[15]	RW	vi3_srst_req	VI CH3 soft reset 0: deassert reset 1: reset
[14]	RW	vi3_ch_cksel	VI CH3 clock select 0: VI3 PAD input clock 1: VI3 2-multiplier clock
[13]	RW	vi3_pctrl	Phase of the VI CH3 interface clock 0 (default): positive phase 1: negative phase
[12]	RW	vi3_cken	VI CH3 clock gating 0: The clock is disabled. 1: The clock is enabled.
[11]	RW	vi2_srst_req	VI CH2 soft reset 0: deassert reset 1: reset
[10]	RW	vi2_ch_cksel	VI CH2 clock select 0: VI2 PAD input clock 1: VI2 2-multiplier clock
[9]	RW	vi2_pctrl	Phase of the VI CH2 interface clock 0 (default): positive phase 1: negative phase
[8]	RW	vi2_cken	VI CH2 clock gating 0: The clock is disabled. 1: The clock is enabled.
[7]	RW	vi1_srst_req	VI CH1 soft reset 0: deassert reset 1: reset
[6]	RW	vi1_ch_cksel	VI CH1 clock select 0: VI1 PAD input clock 1: VI1 2-multiplier clock
[5]	RW	vi1_pctrl	Phase of the VI CH1 interface clock 0 (default): positive phase 1: negative phase
[4]	RW	vi1_cken	VI CH1 clock gating 0: The clock is disabled. 1: The clock is enabled.

[3]	RW	vi0_srst_req	VI CH0 soft reset 0: deassert reset 1: reset
[2]	RW	vi0_ch_cksel	VI CH0 clock select 0: VI0 PAD input clock 1: VI0 2-multiplier clock
[1]	RW	vi0_pctrl	Phase of the VI CH0 interface clock 0 (default): positive phase 1: negative phase
[0]	RW	vi0_cken	VI CH0 clock gating 0: The clock is disabled. 1: The clock is enabled.

PERI_CRG12

PERI_CRG12 is a VOU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_CRG12	0x0000_0CFC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vosd_cksel	vohd_cksel	vosd_out_pctrl	vohd_out_pctrl	vo_hd_dac_cken	vo_sd_dac_cken	reserved		vo_dac_cken	vo_acken	vo_pcken	vo_sd_cken	vo_hd_cken	vo_cken	reserved	vo_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	vosd_cksel	VO SD frequency divider 0: 4 1: 2
[14]	RW	vohd_cksel	VO HD frequency divider 0: 1 1: 2

[13]	RW	vosd_out_pctrl	Phase of the VDAC clock 0: positive phase 1 (default): negative phase
[12]	RW	vohd_out_pctrl	Phase of the VOU HD output associate clock 0: positive phase 1 (default): negative phase
[11]	RW	vo_hd_dac_cken	VOU HD DAC clock gating 0: The clock is disabled. 1: The clock is enabled.
[10]	RW	vo_sd_dac_cken	VOU SD DAC clock gating 0: The clock is disabled. 1: The clock is enabled.
[9:8]	RO	reserved	Reserved
[7]	RW	vo_dac_cken	VOU DAC clock gating 0: The clock is disabled. 1: The clock is enabled.
[6]	RW	vo_acken	VOU AXI bus clock gating 0: The clock is disabled. 1: The clock is enabled.
[5]	RW	vo_pcken	VO APB clock gating 0: The clock is disabled. 1: The clock is enabled.
[4]	RW	vo_sd_cken	VO SD clock gating 0: The clock is disabled. 1: The clock is enabled.
[3]	RW	vo_hd_cken	VOU HD clock gating 0: The clock is disabled. 1: The clock is enabled.
[2]	RW	vo_cken	VO PPC/CFG clock gating (internally configured) 0: The clock is disabled. 1: The clock is enabled.
[1]	RO	reserved	Reserved
[0]	RW	vo_srst_req	VOU soft reset 0: deassert reset 1: reset

PERI_CRG13

PERI_CRG13 is an SoC/DDR clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_CRG13	0x0700_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			ddr_hipack_srst_req	ddr_apb_srst_req	ddr_cfg_cken	ddr_hipack_cken	ddr_apb_cken	reserved								bus_cksel								reserved		vedu1_cksel1	vedu0_cksel1	cpu_cksel		ddr_cksel	
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28]	RW	ddr_hipack_srst_req	DDR HIPACK soft reset 0: deassert reset 1: reset
[27]	RW	ddr_apb_srst_req	DDR APB soft reset 0: deassert reset 1: reset
[26]	RW	ddr_cfg_cken	DDR CFG clock gating 0: The clock is disabled. 1: The clock is enabled.
[25]	RW	ddr_hipack_cken	DDR HIPACK clock gating 0: The clock is disabled. 1: The clock is enabled.
[24]	RW	ddr_apb_cken	DDR APB clock gating 0: The clock is disabled. 1: The clock is enabled.
[23:14]	RO	reserved	Reserved

[13:8]	RW	bus_cksel	BUS clock configuration [9:8]: MDA_300_AXI clock configuration 00: XTAL clock 01: 250 MHz clock 10: 300 MHz clock 11: reserved [10]: MDA_270M_AXI clock configuration 0: XTAL clock 1: 270 MHz clock [13:12]: SYS AXI clock configuration 00: XTAL clock 01: 250 MHz clock 10: 202.5 MHz clock 11: reserved
[7:6]	RO	reserved	Reserved
[5]	RW	vedu1_cksel1	VEDU1 clock frequency select. This bit works with PERI_CRG16[vedu1_cksel] for selecting the clock. {vedu1_cksel1, vedu1_cksel} x0: 324 MHz 01: 405 MHz 11: reserved
[4]	RW	Vedu0_cksel1	VEDU0 clock frequency select. This bit works with PERI_CRG15[vedu0_cksel] for selecting the clock. {vedu0_cksel1, vedu0_cksel} x0: 324 MHz 01: 405 MHz 11: reserved
[3:2]	RW	cpu_cksel	CPU clock configuration 00: XTAL clock 01: APLL POSTDIV 10: 750 MHZ (internal frequency division) 11: reserved
[1:0]	RW	ddr_cksel	DDR clock configuration 00: XTAL clock 01: DDR POSTDIV 1x: reserved

PERI_CRG14

PERI_CRG14 is an HDMI clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0038	PERI_CRG14	0x0000_003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	hdmitx_ctrl_asclk_sel	hdmitx_asin_cksel	hdmitx_ctrl_cec_clk_sel	reserved		hdmitx_ctrl_srst_req	hdmitx_ctrl_bus_srst_req	reserved				hdmitx_ctrl_as_cken	hdmitx_ctrl_os_cken	hdmitx_ctrl_mhl_cken	hdmitx_ctrl_id_cken	hdmitx_ctrl_cec_cken	hdmitx_ctrl_bus_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	hdmitx_ctrl_asclk_sel	HDMI TX asclk clock select 1: internal CRG clock 0: HDMI TX PHY clock
[13]	RW	hdmitx_asin_cksel	HDMI TX asclk internal clock select 0: 125 MHz clock 1: 100 MHz clock
[12]	RW	hdmitx_ctrl_cec_clk_sel	HDMI TX cec clock select 0: 2 MHz clock 1: 2.02 MHz clock
[11:10]	RO	reserved	Reserved
[9]	RW	hdmitx_ctrl_srst_req	HDMI TX soft reset 0: deassert reset 1: reset
[8]	RW	hdmitx_ctrl_bus_srst_req	HDMI TX bus soft reset 0: deassert reset 1: reset
[7:6]	RO	reserved	Reserved
[5]	RW	hdmitx_ctrl_as_cken	HDMI TX AS clock gating 0: disabled 1: enabled

[4]	RW	hdmitx_ctrl_os_cken	HDMI TX OS clock gating 0: disabled 1: enabled
[3]	RW	hdmitx_ctrl_mhl_cken	HDMI TX clock gating 0: disabled 1: enabled
[2]	RW	hdmitx_ctrl_id_cken	HDMI TX ID clock gating 0: disabled 1: enabled
[1]	RW	hdmitx_ctrl_cec_cken	HDMI TX CEC clock gating 0: disabled 1: enabled
[0]	RW	hdmitx_ctrl_bus_cken	HDMI TX bus clock gating 0: disabled 1: enabled

PERI_CRG15

PERI_CRG15 is a VEDU0 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x003C	PERI_CRG15	0x0000_0802

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sed0_cken	sed0_srst_req	vedu0clk_loaden	vedu0clk_skipcfg					sed0_cksel	vedu0_cksel	vedu0_cken	vedu0_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	sed0_cken	SED0 clock gating 0: The clock is disabled. 1: The clock is enabled.

[10]	RW	sed0_srst_req	SED0 soft reset 0: deassert reset 1: reset
[9]	RW	vedu0clk_loaden	VEDU0 clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to vedu0clk_loaden. 3. Write 1 to vedu0clk_loaden.
[8:4]	RW	vedu0clk_skipcfg	VEDU0 clock skip configuration N: *N*-beat clocks are disabled every 32-beat VEDU clocks.
[3]	RW	sed0_cksel	SED0 clock frequency select 0: 187 MHz 1: reserved
[2]	RW	vedu0_cksel	VEDU0 clock frequency select. This bit works with PERI_CRG13[vedu0_cksel1] for selecting the clock. {vedu0_cksel1, vedu0_cksel} x0: 324MHz 01: 405MHz 11: reserved
[1]	RW	vedu0_cken	VEDU0 clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	vedu0_srst_req	VEDU0 soft reset 0: deassert reset 1: reset

PERI_CRG16

PERI_CRG16 is a VEDU1 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_CRG16	0x0000_0802

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sed1_cken	sed1_srst_req	vedu1clk_loaden	vedu1clk_skipcfg					sed1_cksel	vedu1_cksel	vedu1_cken	vedu1_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	sed1_cken	SED1 clock gating 0: The clock is disabled. 1: The clock is enabled.
[10]	RW	sed1_srst_req	SED1 soft reset 0: deassert reset 1: reset
[9]	RW	vedu1clk_loaden	VEDU1 clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to vedu1clk_loaden. 3. Write 1 to vedu1clk_loaden.
[8:4]	RW	vedu1clk_skipcfg	VEDU1 clock skip configuration. N: *N*-beat clocks are disabled every 32-beat VEDU clocks.
[3]	RW	sed1_cksel	SED1 clock frequency select 0: 187 MHz 1: reserved
[2]	RW	vedu1_cksel	VEDU1 clock frequency select. This bit works with PERI_CRG13[vedu1_cksel1] for selecting the clock. {vedu1_cksel1, vedu1_cksel} x0: 324 MHz 01: 405 MHz 11: reserved
[1]	RW	vedu1_cken	VEDU1 clock gating 0: The clock is disabled. 1: The clock is enabled.

[0]	RW	vedu1_srst_req	VEDU1 soft reset 0: deassert reset 1: reset

PERI_CRG17

PERI_CRG17 is a VPSS clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0044	PERI_CRG17	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vpsclk_loaden		vpsclk_skipcfg					vps_cksel		vps_cken	vps_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	vpsclk_loaden	VPSS clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to vpsclk_loaden. 3. Write 1 to vpsclk_loaden.
[8:4]	RW	vpsclk_skipcfg	VPSS clock skip configuration N: *N*-beat clocks are disabled every 32-beat VPS clocks.
[3:2]	RW	vps_cksel	Frequency select for the VPSS working clock 00: 375 MHz 01: 405 MHz 10: reserved 11: reserved
[1]	RW	vps_cken	VPSS clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	vps_srst_req	VPSS soft reset 0: deassert reset 1: reset

PERI_CRG18

PERI_CRG18 is a TDE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tdeclk_loaden	tdeclk_skipcfg					reserved		tde_cken	tde_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	tdeclk_loaden	TDE clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to tdeclk_loaden. 3. Write 1 to tdeclk_loaden.
[8:4]	RW	tdeclk_skipcfg	TDE clock skip configuration N: *N*-beat clocks are disabled every 32-beat TDE clocks.
[3:2]	RO	reserved	Reserved
[1]	RW	tde_cken	TDE clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	tde_srst_req	TDE soft reset 0: deassert reset 1: reset

PERI_CRG19

PERI_CRG19 is a VGS clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x004C	PERI_CRG19	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						vgsclk_loaden	vgsclk_skipcfg					reserved	vgs_cksel	vgs_cken	vgs_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	vgsclk_loaden	VGS clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to vgsclk_loaden. 3. Write 1 to vgsclk_loaden.
[8:4]	RW	vgsclk_skipcfg	VGS clock skip configuration N: *N*-beat clocks are disabled every 32-beat TDE clocks.
[3]	RO	reserved	Reserved
[2]	RW	vgs_cksel	Frequency select for the VGS clock 0: 300 MHz 1: reserved
[1]	RW	vgs_cken	VGS clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	vgs_srst_req	VGS soft reset 0: deassert reset 1: reset

PERI_CRG20

PERI_CRG20 is a JPGE/VOIE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0050	PERI_CRG20	0x0002_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						voieclk_loaden	voieclk_skipcfg					reserved		voie_cken	voie_srst_req	reserved						jpgeclk_loaden	jpgeclk_skipcfg					reserved		jpge_cken	jpge_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	voieclk_loaden	VOIE clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to voieclk_loaden. 3. Write 1 to voieclk_loaden.
[24:20]	RW	voieclk_skipcfg	VOIE clock skip configuration N: *N*-beat clocks are disabled every 32-beat TDE clocks.
[19:18]	RO	reserved	Reserved
[17]	RW	voie_cken	VOIE clock gating 0: The clock is disabled. 1: The clock is enabled.
[16]	RW	voie_srst_req	VOIE soft reset 0: deassert reset 1: reset
[15:10]	RO	reserved	Reserved
[9]	RW	jpgeclk_loaden	JPGE clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to jpgeclk_loaden. 3. Write 1 to jpgeclk_loaden.
[8:4]	RW	jpgeclk_skipcfg	JPGE clock skip configuration N: *N*-beat clocks are disabled every 32-beat TDE clocks.
[3:2]	RO	reserved	Reserved

[1]	RW	jpge_cken	JPGE clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	jpge_srst_req	JPGE soft reset 0: deassert reset 1: reset

PERI_CRG21

PERI_CRG21 is a JPGD clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0054	PERI_CRG21	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						jpgdclk_loaden	jpgdclk_skipcfg					reserved		jpgd_cken	jpgd_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	jpgdclk_loaden	JPGD clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to jpgdclk_loaden. 3. Write 1 to jpgdclk_loaden.
[8:4]	RW	jpgdclk_skipcfg	JPGD clock skip configuration N: *N*-beat clocks are disabled every 32-beat TDE clocks.
[3:2]	RO	reserved	Reserved
[1]	RW	jpgd_cken	JPGD clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	jpgd_srst_req	JPGD soft reset 0: deassert reset 1: reset

PERI_CRG22

PERI_CRG22 is an MDU clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0058	PERI_CRG22	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						mduclk_loaden		mduclk_skipcfg					reserved		mdu_cken	mdu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	mduclk_loaden	MDU clock skip configuration enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to mduclk_loaden. 3. Write 1 to mduclk_loaden.
[8:4]	RW	mduclk_skipcfg	MDU clock skip configuration N: *N*-beat clocks are disabled every 32-beat TDE clocks.
[3:2]	RO	reserved	Reserved
[1]	RW	mdu_cken	MDU clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	mdu_srst_req	MDU soft reset 0: deassert reset 1: reset

PERI_CRG23

PERI_CRG23 is an IVE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_CRG23	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ive_cken	ive_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	ive_cken	IVE clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	ive_srst_req	IVE soft reset 0: deassert reset 1: reset

PERI_CRG24

PERI_CRG24 is a cipher clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_CRG24	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cipher_cken	cipher_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved

[1]	RW	cipher_cken	Cipher clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	cipher_srst_req	Cipher soft reset 0: deassert reset 1: reset

PERI_CRG25

PERI_CRG25 is an AIAO clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0064	PERI_CRG25	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												aio_cksel		aiao_cken	aio_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:2]	RW	aio_cksel	AIAO MCLK PLL source select 00: 500 MHz 01: EPLL_FOUTVCO 1x: reserved
[1]	RW	aiao_cken	AIAO clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	aio_srst_req	AIAO soft reset 0: deassert reset 1: reset

PERI_CRG26

PERI_CRG26 is an SATA PHY clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0068	PERI_CRG26	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												sata_phy1_refclk_sel	sata_phy1_ref_cken	sata_phy0_refclk_sel	sata_phy0_ref_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	sata_phy1_refclk_sel	SATA PHY1 refclk select 0: 100 MHz 1: 24 MHz
[2]	RW	sata_phy1_ref_cken	SATA PHY1 refclk clock gating 0: disabled 1: enabled
[1]	RW	sata_phy0_refclk_sel	SATA PHY0 refclk select 0: 100 MHz 1: 24 MHz
[0]	RW	sata_phy0_ref_cken	SATA PHY0 refclk clock gating 0: disabled 1: enabled

PERI_CRG27

PERI_CRG27 is an SATA controller clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x006C	PERI_CRG27	0x0003_0770

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														sata_refclk1_cken	sata_mpll_dword1_cken	reserved		sata_cko_alive_srst_req	sata_bus_srst_req	reserved		sata_refclk0_cken	sata_mpll_dword0_cken	sata_cko_alive_cken	reserved			sata_rx1_cken	sata_rx0_cken	sata_bus_cken	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	sata_refclk1_cken	SATA CTRL port 1 refclk clock gating 0: disabled 1: enabled
[16]	RW	sata_mpll_dword1_cken	SATA CTRL port 1 mpll_dword clock gating 0: disabled 1: enabled
[15:14]	RO	reserved	Reserved
[13]	RW	sata_cko_alive_srst_req	SATA CTRL cko_alive soft reset 0: deassert reset 1: reset
[12]	RW	sata_bus_srst_req	SATA CTRL bus soft reset 0: deassert reset 1: reset
[11]	RO	reserved	Reserved
[10]	RW	sata_refclk0_cken	SATA CTRL port 0 refclk clock gating 0: disabled 1: enabled
[9]	RW	sata_mpll_dword0_cken	SATA CTRL port 0 mpll_dword clock gating 0: disabled 1: enabled

[8]	RW	sata_cko_alive_cken	SATA CTRL cko_alive clock gating 0: disabled 1: enabled
[7]	RO	reserved	Reserved
[6]	RW	sata_rx1_cken	SATA CTRL RX1 clock gating 0: disabled 1: enabled
[5]	RW	sata_rx0_cken	SATA ctrl rx0 clock gating 0: disabled 1: enabled
[4]	RW	sata_bus_cken	SATA CTRL bus clock gating 0: disabled 1: enabled
[3:0]	RO	reserved	Reserved

PERI_CRG28

PERI_CRG28 is a USB clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0070	PERI_CRG28	0x0000_008E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								usb2_cken	usb2_ctrl_utmi1_req	usb2_ctrl_utmi0_req	usb2_ctrl_hub_req	usb2phy_port1_treq	usb2phy_port0_treq	usb2phy_req	usb2_ahb_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	usb2_cken	USB PHY reference clock gating 0: disabled 1: enabled

[6]	RW	usb2_ctrl_utmi1_req	USB controller port 1 soft reset 0: deassert reset 1: reset
[5]	RW	usb2_ctrl_utmi0_req	USB controller port 0 soft reset 0: deassert reset 1: reset
[4]	RW	usb2_ctrl_hub_req	USB controller hub soft reset 0: deassert reset 1: reset
[3]	RW	usb2phy_port1_treq	USB PHY port 1 soft reset 0: deassert reset 1: reset
[2]	RW	usb2phy_port0_treq	USB PHY port 0 soft reset 0: deassert reset 1: reset
[1]	RW	usb2phy_req	USB PHY soft reset 0: deassert reset 1: reset
[0]	RW	usb2_ahb_srst_req	USB controller bus soft reset 0: deassert reset 1: reset

PERI_CRG29

PERI_CRG29 is an FMC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0074	PERI_CRG29	0x0000_0002

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved							fmc_cksel	fmc_cken	fmc_srst_req
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved

[3:2]	RW	fmc_cksel	FMC clock source select 00: 24 MHz clock 01: 83 MHz clock 10: 150 MHz clock 11: reserved
[1]	RW	fmc_cken	FMC clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	fmc_srst_req	FMC soft reset 0: deassert reset 1: reset

PERI_CRG30

PERI_CRG30 is a GSF/GMAC/FEPHY clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0078	PERI_CRG30	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gsf_cksel	ext_fephy_cksel	ext_fephy_srst_req	rmii_cksel	gmac_if_cken	gmac_if_srst_req	gsf_cken	gsf_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	gsf_cksel	GSF working clock select 0: 125 MHz clock 1: 75 MHz clock
[6]	RW	ext_fephy_cksel	External FEPHY clock select 1: 25 MHz clock 0: 50 MHz clock
[5]	RW	ext_fephy_srst_req	External FEPHY soft reset 0: deassert reset 1: reset

[4]	RW	rmii_cksel	RMII clock select 1: PAD input clock 0: CRG clock
[3]	RW	gmac_if_cken	GMAC clock gating 0: The clock is disabled. 1: The clock is enabled.
[2]	RW	gmac_if_srst_req	GMAC soft reset 0: deassert reset 1: reset
[1]	RW	gsf_cken	GSF clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	gsf_srst_req	GSF soft rest 0: deassert reset 1: reset

PERI_CRG31

PERI_CRG31 is an SCD clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_CRG31	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														scd_cken	scd_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	scd_cken	SCD clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	scd_srst_req	SCD soft reset 0: deassert reset 1: reset

PERI_CRG32

PERI_CRG32 is a DMA/DDRTEST/EFUSE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0080	PERI_CRG32	0x0000_002A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dma_cken	dma_srst_req	ddrtest_cken	ddrtest_srst_req	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	dma_cken	DMA clock gating 0: The clock is disabled. 1: The clock is enabled.
[4]	RW	dma_srst_req	DMA soft reset 0: deassert reset 1: reset
[3]	RW	ddrtest_cken	DDRTEST clock gating 0: The clock is disabled. 1: The clock is enabled.
[2]	RW	ddrtest_srst_req	DDRTEST soft reset 0: deassert reset 1: reset
[1]	RO	reserved	Reserved
[0]	RO	reserved	Reserved

PERI_CRG33

PERI_CRG33 is an APB peripheral clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0084	PERI_CRG33	0x0003_B001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												uart_cksel		uart2_cken	uart1_cken	uart0_cken	reserved	ssp_cken	ir_cken	reserved		uart2_srst_req	uart1_srst_req	uart0_srst_req	reserved	ssp_srst_req	ir_srst_req	rtc_srst_req	reserved	i2c_srst_req	test_clk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:18]	RW	uart_cksel	UART clock select 00: APB clock 01: 2 MHz clock 10: crystal oscillator clock 11: reserved
[17]	RW	uart2_cken	UART2 clock gating 0: The clock is disabled. 1: The clock is enabled.
[16]	RW	uart1_cken	UART1 clock gating 0: The clock is disabled. 1: The clock is enabled.
[15]	RW	uart0_cken	UART0 clock gating 0: The clock is disabled. 1: The clock is enabled.
[14]	RO	reserved	Reserved
[13]	RW	ssp_cken	SSP clock gating 0: The clock is disabled. 1: The clock is enabled.
[12]	RW	ir_cken	IR clock gating 0: The clock is disabled. 1: The clock is enabled.
[11:10]	RO	reserved	Reserved
[9]	RW	uart2_srst_req	UART2 soft reset 0: deassert reset 1: reset

[8]	RW	uart1_srst_req	UART1 soft reset 0: deassert reset 1: reset
[7]	RW	uart0_srst_req	UART0 soft reset 0: deassert reset 1: reset
[6]	RW	reserved	Reserved
[5]	RW	ssp_srst_req	SSP soft reset 0: deassert reset 1: reset
[4]	RW	ir_srst_req	IR soft reset 0: deassert reset 1: reset
[3]	RW	rtc_srst_req	RTC soft reset 0: deassert reset 1: reset
[2]	RW	reserved	Reserved
[1]	RW	i2c_srst_req	I^2C soft reset 0: deassert reset 1: reset
[0]	RW	test_clk_en	Test clock enable 0: All test clocks are disabled. 1: All test clocks are enabled.

PERI_CRG34

PERI_CRG34 is a CRG status register.

Offset Address	Register Name	Total Reset Value
0x0088	PERI_CRG34	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											dpll_lock	epll_lock	vpll2_lock	vpll0_lock	apll_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RO	dpll_lock	DPLL lock status 0: unlocked 1: locked
[3]	RO	epll_lock	EPLL lock status 0: unlocked 1: locked
[2]	RO	vpll2_lock	VPLL2 lock status 0: unlocked 1: locked
[1]	RO	vpll0_lock	VPLL0 lock status 0: unlocked 1: locked
[0]	RO	apll_lock	APLL lock status 0: unlocked 1: locked

PERI_CRG35

PERI_CRG35 is a GMAC interface control register.

Offset Address	Register Name	Total Reset Value
0x008C	PERI_CRG35	0x0000_003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							loopback_mode	phy_select			duplex_mode	tx_config	link_status	mac_speed	port_select
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	loopback_mode	Loopback mode enable 0: disabled 1: enabled
[7:5]	RW	phy_select	PHY interface mode 000: GMII/MII mode 001: RGMII mode 100: RMII mode Other values: reserved
[4]	RW	duplex_mode	PHY duplex mode 0: half-duplex mode 1: full-duplex mode
[3]	RW	tx_config	TX configuration enable 0: disabled 1: enabled
[2]	RW	link_status	PHY connection status control 0: link down 1: link up
[1]	RW	mac_speed	10/100 Mbit/s mode select 0: 10 Mbit/s 1: 100 Mbit/s
[0]	RW	port_select	Gigabit mode select 0: 1000 Mbit/s 1: 10/100 Mbit/s

PERI_CRG36

PERI_CRG36 is a GMAC interface status register.

Offset Address	Register Name	Total Reset Value
0x0090	PERI_CRG36	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																gmac0_if_sys_stat																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	Link_status	Connection status when rxdv and rxer are both 0 in RGMII mode 0: link down 1: link up
[2:1]	RO	Link_speed	Rate status when rxdv and rxer are both 0 in RGMII mode 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: reserved
[0]	RO	Link_mode	Duplex mode when rxdv and rxer are both 0 in RGMII mode 0: half-duplex mode 1: full-duplex mode

PERI_CRG37

PERI_CRG37 is a VPLL0 spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x0094	PERI_CRG37	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vpll0_ssmod_cfg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

[11:0]	RW	vpll0_ssmod_cfg	ssmod divval[11:8] SSMOD divval control ssmod spread[6:4] SSMOD spread control 0: 0 1: 0.049% 2: 0.098% 3: 0.195% 4: 0.391% 5: 0.781% 6: 1.563% 7: 3.125% ssmod downspread[3] SSMOD down spread control 0: central spread spectrum 1: down spread spectrum ssmod_disable[2] SSMOD disable 0: enabled 1: disabled ssmod_rst_req [1] SSMOD reset 0: deassert reset 1: reset ssmod_cken [0] SSMOD clock gating 0 (default): disabled 1: enabled

PERI_CRG38

PERI_CRG38 is a VPLL2 spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x0098	PERI_CRG38	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vpll2_ssmod_cfg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	vpll2_ssmod_cfg	ssmod divval[11:8] SSMOD divval control ssmod spread[6:4] SSMOD spread control 0: 0 1: 0.049% 2: 0.098% 3: 0.195% 4: 0.391% 5: 0.781% 6: 1.563% 7: 3.125% ssmod downspread[3] SSMOD down spread control 0: central spread spectrum 1: down spread spectrum ssmod_disable[2] SSMOD disable control 0: enabled 1: disabled ssmod_rst_req [1] SSMOD reset 0: deassert reset 1: reset ssmod_cken [0] SSMOD clock gating 0 (default): disabled 1: enabled

PERI_CRG39

PERI_CRG39 is an APLL spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x009C	PERI_CRG39	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				apll_ssmod_cfg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	apll_ssmod_cfg	ssmod divval[11:8] SSMOD divval control ssmod spread[6:4] SSMOD spread control 0: 0 1: 0.049% 2: 0.098% 3: 0.195% 4: 0.391% 5: 0.781% 6: 1.563% 7: 3.125% ssmod downspread[3] SSMOD down spread control 0: central spread spectrum 1: down spread spectrum ssmod_disable[2] SSMOD disable 0: enabled 1: disabled ssmod_rst_req [1] SSMOD reset 0: deassert reset 1: reset ssmod_cken [0] SSMOD clock gating 0 (default): disabled 1: enabled

PERI_CRG40

PERI_CRG40 is an EPLL spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	PERI_CRG40	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				epll_ssmod_cfg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	epll_ssmod_cfg	ssmod divval[11:8] SSMOD divval control ssmod spread[6:4] SSMOD spread control 0: 0 1: 0.049% 2: 0.098% 3: 0.195% 4: 0.391% 5: 0.781% 6: 1.563% 7: 3.125% ssmod downspread[3] SSMOD down spread control 0: central spread spectrum 1: down spread spectrum ssmod_disable[2] SSMOD disable 0: enabled 1: disabled ssmod_rst_req [1] SSMOD reset 0: deassert reset 1: reset ssmod_cken [0] SSMOD clock gating 0 (default): disabled 1: enabled

PERI_CRG41

PERI_CRG41 is a DLL0 control and status register.

Offset Address	Register Name	Total Reset Value
0x00A4	PERI_CRG41	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														dll0_dsel		dll0_dllssel								dll0_dllmode	dll0_bypass	dll0_stop	dll0_slave_en	dll0_tune			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17:16]	RW	dll0_dsel	DLL0 DLY_ELEMENT delay step select 00: step 0 01: step 1 10: reserved 11: step 3
[15:8]	RW	dll0_dllssel	Step select for DLL0 slave delay line, valid when dll_dllmode is high
[7]	RW	dll0_dllmode	DLL0 mode select 0: normal mode 1: The slave line is controlled by dll_dllssel.
[6]	RW	dll0_bypass	DLL0 slave line bypass 0: normal mode 1: The slave line is bypassed.
[5]	RW	dll0_stop	Master counting clock cycle disable 0: The clock detection is enabled. 1: The clock detection is disabled.
[4]	RW	dll0_slave_en	DLL0 slave delay line enable 0: disabled 1: enabled

[3:0]	RW	dll0_tune	DLL0 slave tap calibration 0000: no calibration 0001: increase delay by one step 0010: increase delay by two steps 0011: increase delay by three steps … 0111: increase delay by seven steps 1000: no calibration 1001: decrease delay by one step 1010: decrease delay by two steps 1011: decrease delay by three steps … 1111: decrease delay by seven steps

PERI_CRG42

PERI_CRG42 is a DLL1 control and status register.

Offset Address	Register Name	Total Reset Value
0x00A8	PERI_CRG42	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														dll1_dsel		dll1_dllssel								dll1_dllmode	dll1_bypass	dll1_stop	dll1_slave_en	dll1_tune			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17:16]	RW	dll1_dsel	DLL1 DLY_ELEMENT delay step select 00: step 0 01: step 1 10: reserved 11: step 3
[15:8]	RW	dll1_dllssel	Step select for DLL1 slave delay line
[7]	RW	dll1_dllmode	DLL1 mode select 0: normal mode 1: The slave line is controlled by dll_dllssel.

[6]	RW	dll1_bypass	DLL1 slave line bypass 0: normal mode 1: The slave line is bypassed.
[5]	RW	dll1_stop	Master counting clock cycle disable 0: The clock detection is enabled. 1: The clock detection is disabled.
[4]	RW	dll1_slave_en	DLL1 slave delay line enable 0: disabled 1: enabled
[3:0]	RW	dll1_tune	DLL1 slave tap calibration 0000: no calibration 0001: increase delay by one step 0010: increase delay by two steps 0011: increase delay by three steps … 0111: increase delay by seven steps 1000: no calibration 1001: decrease delay by one step 1010: decrease delay by two steps 1011: decrease delay by three steps … 1111: decrease delay by seven steps

PERI_CRG43

PERI_CRG43 is a DLL2 control and status register.

Offset Address	Register Name	Total Reset Value
0x00AC	PERI_CRG43	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														dll2_dsel		dll2_dllssel								dll2_dllmode	dll2_bypass	dll2_stop	dll2_slave_en	dll2_tune			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved

[17:16]	RW	dll2_dsel	DLL2 DLY_ELEMENT delay step select 00: step 0 01: step 1 10: reserved 11: step 3
[15:8]	RW	dll2_dllssel	Step select for DLL2 slave delay line, valid when dll_dllmode is high
[7]	RW	dll2_dllmode	DLL2 mode select 0: normal mode 1: The slave line is controlled by dll_dllssel.
[6]	RW	dll2_bypass	DLL2 slave line bypass 0: normal mode 1: The slave line is bypassed.
[5]	RW	dll2_stop	Master counting clock cycle disable 0: The clock detection is enabled. 1: The clock detection is disabled.
[4]	RW	dll2_slave_en	DLL2 slave delay line enable 0: disabled 1: enabled
[3:0]	RW	dll2_tune	DLL2 slave tap calibration 0000: no calibration 0001: increase delay by one step 0010: increase delay by two steps 0011: increase delay by three steps … 0111: increase delay by seven steps 1000: no calibration 1001: decrease delay by one step 1010: decrease delay by two steps 1011: decrease delay by three steps … 1111: decrease delay by seven steps

PERI_CRG44

PERI_CRG44 is a DLL3 control and status register.

Offset Address	Register Name	Total Reset Value
0x00B0	PERI_CRG44	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														dll3_dsel		dll3_dllssel								dll3_dllmode	dll3_bypass	dll3_stop	dll3_slave_en	dll3_tune			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17:16]	RW	dll3_dsel	DLL3 DLY_ELEMENT delay step select 00: step 0 01: step 1 10: reserved 11: step 3
[15:8]	RW	dll3_dllssel	Step select for DLL3 slave delay line, valid when dll_dllmode is high
[7]	RW	dll3_dllmode	DLL3 mode select 0: normal mode 1: The slave line is controlled by dll_dllssel.
[6]	RW	dll3_bypass	DLL3 slave line bypass 0: normal mode 1: The slave line is bypassed.
[5]	RW	dll3_stop	Master counting clock cycle disable 0: The clock detection is enabled. 1: The clock detection is disabled.
[4]	RW	dll3_slave_en	DLL3 slave delay line enable 0: disabled 1: enabled

[3:0]	RW	dll3_tune	DLL3 slave tap calibration 0000: no calibration 0001: increase delay by one step 0010: increase delay by two steps 0011: increase delay by three steps … 0111: increase delay by seven steps 1000: no calibration 1001: decrease delay by one step 1010: decrease delay by two steps 1011: decrease delay by three steps … 1111: decrease delay by seven steps

PERI_CRG45

PERI_CRG45 is an ADC REF0/REF1 clock configuration register.

Offset Address	Register Name	Total Reset Value
0x00B4	PERI_CRG45	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										adc_ref1_cken	adc_ref0_cken	adc_ref1_cksel		adc_ref0_cksel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	adc_ref1_cken	ADC1 REF clock gating 0: The clock is disabled. 1: The clock is enabled.
[4]	RW	adc_ref0_cken	ADC0 REF clock gating 0: The clock is disabled. 1: The clock is enabled.

[3:2]	RW	adc_ref1_cksel	ADC1 REF clock select 00: 24 MHz clock 01: 27 MHz clock 10: 54 MHz clock 11: reserved
[1:0]	RW	adc_ref0_cksel	ADC0 REF clock select 00: 24 MHz clock 01: 27 MHz clock 10: 54 MHz clock 11: reserved

PERI_CRG46

PERI_CRG46 is a DPLL spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x00B8	PERI_CRG46	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dpll_ssmod_cfg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved

[11:0]	RW	dpll_ssmod_cfg	ssmod divval[11:8] SSMOD divval control ssmod spread[6:4] SSMOD spread control 0: 0 1: 0.049% 2: 0.098% 3: 0.195% 4: 0.391% 5: 0.781% 6: 1.563% 7: 3.125% ssmod downspread[3] SSMOD down spread control 0: central spread spectrum 1: down spread spectrum ssmod_disable[2] SSMOD disable 0: enabled 1: disabled ssmod_rst_req [1] SSMOD reset 0: deassert reset 1: reset ssmod_cken [0] SSMOD clock gating 0 (default): disabled 1: enabled

3.3 Processor Subsystem

The Hi3521A uses the single-core ARM Cortex-A7 MPCore processor with the heterogeneous architecture.

- 1.1 GHz dominant working frequency
- 32 KB I-cache and 32 KB D-cache for the L1 cache
- Integrated 128 KB 8-way set-associative L2 cache. The L2 cache and processor have the same frequency. The cache line is fixed at 64 bytes. The L2 cache is based on the physical address and physical tag and supports the pseudo random cache replacement policy.

- 128-bit ACE bus interface that is compatible with the AXI interface, and asynchronous system bus and processor (including L2)
- Generic interrupt controller (GIC) in the processor that support the processing of 96 interrupt sources, including 64 external interrupts.
- Single-thread structure that supports 1.9 DMIPs/MHz
- 8-stage pipelines, partially dual-issue
- Integrated MMU
- Vxworks or Linux operating system
- Branch prediction with up to 95% precision
- JTAG debugging interface
- Integrated NEON with the FPU coprocessor

NOTE

For details about the principles of the lock-down function in C format, see the *ARM Architecture Reference Manual*.

3.4 Interrupt System

The Hi3521A supports a maximum of 96 interrupt sources. Table 3-7 describes the interrupt sources.

Table 3-7 interrupt sources

Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
0	SGI0	48	GMAC
1	SGI1	49	SATA
2	SGI2	50	USB2_OHCI
3	SGI3	51	USB2_EHCI
4	SGI4	52	-
5	SGI5	53	-
6	SGI6	54	-
7	SGI7	55	-
8	SGI8	56	-
9	SGI9	57	-
10	SGI10	58	-
11	SGI11	59	-
12	SGI12	60	VICAP
13	SGI13	61	HDMI
14	SGI14	62	VDP0

Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
15	SGI15	63	AVC0
16	-	64	TDE
17	-	65	IVE
18	-	66	JPGD
19	-	67	VGS
20	-	68	AVC1
21	-	69	VPSS
22	-	70	VOIE
23	-	71	JPGE
24	-	72	AIAO
25	-	73	SCD
26	-	74	VDP1
27	-	75	MDU
28	-	76	-
29	-	77	-
30	-	78	-
31	-	79	-
32	WDG	80	-
33	Timer0/Timer1	81	-
34	Timer2/Timer3	82	-
35	Timer4/Timer5	83	SOFTWARE_INT
36	Timer6/Timer7	84	A7_COMMTX
37	RTC	85	A7_COMMRX
38	UART0	86	A7_PMUIRQ
39	UART1	87	A7_CTIIRQ
40	UART2	88	-
41	IR	89	GPIO0~GPIO4
42	DMA	90	GPIO5~GPIO9
43	FMC	91	GPIO10~GPIO13
44	I2C	92	DDRC_ERR_INT
45	CIPHER	93	-

Interrupt Bit	Interrupt Source	Interrupt Bit	Interrupt Source
46	SSP	94	-
47	DDRT	95	-

3.5 System Controller

3.5.1 Overview

The system controller controls the operating mode from several aspects. To be specific, it controls the operating mode of the system, monitors the system status, manages the key functions of the system, and configures some functions of peripherals.

3.5.2 Features

The system controller has the following features:

- Controls the system address remap and monitors its status.
- Provides general peripheral registers
- Provides write protection for key registers.
- Provides chip identification (ID) registers.

3.5.3 Function Description

Soft Reset

The system controller can soft-reset the entire chip or some modules.

After the global soft reset register SC_SYSRES is configured, the system controller transmits a reset request to the on-chip reset module for setting the Hi3521A.

System Address Remap Control

For details, see section 1.3 "Boot Modes."

Write Protection for Key Registers

To avoid the entire system being severely affected by the misoperation on the system controller, the system controller provides write protection for key configuration registers. The key configuration registers are as follows:

- Control register for system: SC_CTRL
- Control register for system global soft reset: SC_SYSRES

Before writing to this key registers, you must disable the write protection function by configuring SC_LOCKEN. After write operations, you need to enable the write protection function by configuring SC_LOCKEN, ensuring that these key registers are not incorrectly written by the software.

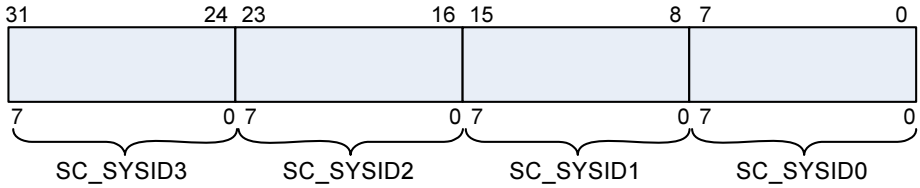
NOTE

By default, write protection is not enabled for key registers after reset. It is recommended that you enable write protection by configuring SC_LOCKEN when the system starts.

System ID Register of the Chip

The system controller provides a chip ID register SC_SYSID. This register is a virtual 32-bit read-only register. It consists of four 8-bit ID registers: SCSYSID3, SCSYSID2, SCSYSID1, and SCSYSID0. After the values of these four registers are read and combined, the value of SC_SYSID, namely, 0X3521_A100, is obtained. Figure 3-4 shows the bit allocation of chip ID registers.

Figure 3-4 Bit allocation of chip ID registers



3.5.4 System Controller Registers

3.5.4.1 Register Summary

Table 3-8 describes system controller registers.

Table 3-8 Summary of system controller registers (base address: 0x1205_0000)

Offset Address	Register	Description	Page
0x000	SC_CTRL	System control register	3-69
0x004	SC_SYSRES	System soft reset register	3-70
0x001C	SOLFINT	Software interrupt register	3-71
0x0020	SOLFTYPE	Software interrupt vector register	3-72
0x0044	SC_LOCKEN	Key register lock register	3-72
0x008C	SYSSTAT	System status register	3-73
0xEE0	SCSYSID0	Chip ID register 0	3-74
0xEE4	SCSYSID1	Chip ID register 1	3-74
0xEE8	SCSYSID2	Chip ID register 2	3-74
0xEEC	SCSYSID3	Chip ID register 3	3-75

3.5.4.2 Register Description

SC_CTRL

SC_CTRL is a system control register. It is used to specify the operations to be performed by the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x000	SC_CTRL	0x0000_0212

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timeren7ov	reserved	timeren6ov	reserved	timeren5ov	reserved	timeren4ov	reserved	wdogenov	timeren3ov	reserved	timeren2ov	reserved	timeren1ov	reserved	timeren0ov	reserved						remapstat	remapclear	reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31]	RW	timeren7ov	Timer 7 count clock select 0: 3 MHz clock 1: bus clock
[30]	RW	reserved	Reserved
[29]	RW	timeren6ov	Timer6 count clock select 0: 3 MHz clock 1: bus clock
[28]	RW	reserved	Reserved
[27]	RW	timeren5ov	Timer 5 count clock select 0: 3 MHz clock 1: bus clock
[26]	RW	reserved	Reserved
[25]	RW	timeren4ov	Timer 4 count clock select 0: 3 MHz clock 1: bus clock
[24]	RW	reserved	Reserved

[23]	RW	wdogenov	Watchdog count clock select 0: 3 MHz clock 1: bus clock
[22]	RW	timeren3ov	Timer 3 count clock select 0: 3 MHz clock 1: bus clock
[21]	RO	reserved	Reserved
[20]	RW	timeren2ov	Timer 2 count clock select 0: 3 MHz clock 1: bus clock
[19]	RW	reserved	Reserved
[18]	RW	timeren1ov	Timer 1 count clock select 0: 3 MHz clock 1: bus clock
[17]	RW	reserved	Reserved
[16]	RW	timeren0ov	Timer 0 count clock select 0: 3 MHz clock 1: bus clock
[15:10]	RW	reserved	Reserved
[9]	RO	remapstat	Address remap status 0: The address is not remapped. 1: The address is remapped. The BOOTROM, NANDC CS 0, or SFC CS 1 is remapped to address 0.
[8]	RW	remapclear	Address remap clear 0: The remap status is retained. 1: The remap status is cleared. For details about the address mappings before and after remapping is cleared, see Table 1-2 "Address space mapping" in chapter 1 "Product Description."
[7:0]	RO	reserved	Reserved. Reading this field returns 0, and writing to this field has no effect.

SC_SYSRES

SC_SYSRES is a system soft reset register. When a value is written to this register, the system controller sends a system soft reset request to the reset module. Then the reset module resets the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x004	SC_SYSRES	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softresreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:0]	WO	softresreq	Writing any value to this register soft-resets the system.

SOLFINT

SOLFINT is a software interrupt register.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x001C	SOLFINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															software_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	software_int	Software interrupt 0: No interrupt is generated. 1: An interrupt is generated.

SOLFTYPE

SOLFTYPE is a software interrupt vector register.

CAUTION

This register is not reset when the system is soft-reset.

Offset Address	Register Name	Total Reset Value
0x0020	SOLFTYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	software_int_vector																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	software_int_vector	Software interrupt vector

SC_LOCKEN

SC_LOCKEN is a key register lock registers.

CAUTION

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0044	SC_LOCKEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scper_lockl																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	scper_lockl	Register for locking key system control registers. The key registers include SC_CTRL, SC_SYSSTAT, SC_PLLCTRL, and SC_PLLFCTRL. When 0x1ACC_E551 is written to SC_LOCKEN, the write permission for all registers is enabled; when any other value is written to SC_LOCKEN, the write permission is disabled. Reading this register returns the lock status but not the written value. 0x0000_0000: The write permission is enabled (unlocked). 0x0000_0001: The write permission is disabled (locked).

SYSSTAT

SYSSTAT is a system status register.

Offset Address	Register Name	Total Reset Value
0x008C	SYSSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bootrom_sel	reserved																						sfc_device_mode	sfc_addr_mode	reserved						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	bootrom_sel	Whether the system boots from the BOOTROM 0: no 1: yes
[30:9]	RO	reserved	Reserved
[8]	RO	sfc_device_mode	SPI flash type 0: SPI NOR flash 1: SPI NAND flash

[7]	RO	sfc_addr_mode	This bit indicates the SPI NOR flash boot address mode when sfc_device_mode is 0. 0: 3-byte address mode 1: 4-byte address mode This bit indicates the SPI NAND flash boot mode when sfc_device_mode is 1. 0: 1-wire mode 1: 4-wire mode
[6:0]	RO	reserved	Reserved

SCSYSID0

SCSYSID0 is chip ID register 0.

Offset Address	Register Name	Total Reset Value
0xEE0	SCSYSID0	0x00

Bit	7	6	5	4	3	2	1	0
Name	sysid0							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	sysid0	Reading this register returns 0x00.

SCSYSID1

SCSYSID1 is chip ID register 1.

Offset Address	Register Name	Total Reset Value
0xEE4	SCSYSID1	0xA1

Bit	7	6	5	4	3	2	1	0
Name	sysid1							
Reset	1	0	1	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid1	Reading this register returns 0xA1.

SCSYSID2

SCSYSID2 is chip ID register 2.

Offset Address	Register Name	Total Reset Value
0xEE8	SCSYSID2	0x21

Bit	7	6	5	4	3	2	1	0
Name	sysid2							
Reset	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid2	Reading this register returns 0x21.

SCSYSID3

SCSYSID3 is chip ID register 3.

Offset Address	Register Name	Total Reset Value
0xEEC	SCSYSID3	0x35

Bit	7	6	5	4	3	2	1	0
Name	sysid3							
Reset	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid3	Reading this register returns 0X35.

3.5.5 Peripheral Control Registers

3.5.5.1 Register Summary

Table 3-9 describes peripheral control registers.

Table 3-9 Summary of peripheral control registers (base address: 0x1212_0000)

Offset Address	Register	Description	Page
0x0000	MISC_CTRL0	A7 CPU control register 0	3-77
0x0004	MISC_CTRL1	A7 CPU control register 1	3-77
0x0008	MISC_CTRL2	A7 CPU status register	3-78
0x0010	MISC_CTRL4	Peripheral function selection register 1	3-78
0x0014	MISC_CTRL5	SSP control register	3-80
0x0018	MISC_CTRL6	System bus arbitration control register 0	3-80
0x0020	MISC_CTRL8	System bus port priority register 0	3-81

Offset Address	Register	Description	Page
0x0024	MISC_CTRL9	System bus port priority register 1	3-82
0x0028	MISC_CTRL10	Media 0 bus arbitration control register 0	3-83
0x002C	MISC_CTRL11	Media 0 bus arbitration control register 1	3-84
0x0030	MISC_CTRL12	Media 0 bus arbitration control register 2	3-84
0x0034	MISC_CTRL13	Media 0 bus priority register	3-85
0x0038	MISC_CTRL14	Media 1 bus arbitration control register 0	3-86
0x003C	MISC_CTRL15	Media 1 bus arbitration control register 1	3-87
0x0040	MISC_CTRL16	Media 1 bus arbitration control register 2	3-87
0x0044	MISC_CTRL17	Media 1 bus priority register	3-88
0x0048	MISC_CTRL18	HP_PERI bus arbitration control register 0	3-89
0x004C	MISC_CTRL19	HP_PERI bus arbitration control register 1	3-90
0x0050	MISC_CTRL20	USB 2.0 control register 0	3-91
0x0054	MISC_CTRL21	USB 2.0 control register 1	3-94
0x0058	MISC_CTRL22	SATA PHY 0 control register 0	3-94
0x005C	MISC_CTRL23	SATA PHY 0 control register 1	3-95
0x0060	MISC_CTRL24	SATA PHY 0 control register 2	3-96
0x0064	MISC_CTRL25	SATA PHY 1 control register 0	3-96
0x0068	MISC_CTRL26	SATA PHY 1 control register 1	3-97
0x006C	MISC_CTRL27	SATA PHY 1 control register 2	3-97
0x0070	MISC_CTRL28	SATA loopback control register	3-97
0x0074	MISC_CTRL29	SATA port 0 loopback configuration register	3-98
0x0078	MISC_CTRL30	SATA port 1 loopback configuration register	3-99
0x007C	MISC_CTRL31	DDQ QoS control register 0	3-99
0x0080	MISC_CTRL32	DDQ QoS control register 1	3-100
0x0084	MISC_CTRL33	DDQ QoS control register 2	3-100
0x0090	MISC_CTRL36	VIVO bus arbitration control register 0	3-101
0x0094	MISC_CTRL37	VIVO bus priority register	3-102

3.5.5.2 Register Description

MISC_CTRL0

MISC_CTRL0 is A7 CPU control register 0.

Offset Address	Register Name	Total Reset Value
0x0000	MISC_CTRL0	0x0000_4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																a7_l2_cache_present				reserved								a7_cp15sdisable			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	a7_l2_cache_present	L2 cache enable 0: disabled 1: enabled
[13:1]	RO	reserved	Reserved
[0]	RW	a7_cp15sdisable	Disable write access to internal secure register of the processor 0: The write access is disabled. 1: The write access is enabled.

MISC_CTRL1

MISC_CTRL1 is A7 CPU control register 1.

Offset Address	Register Name	Total Reset Value
0x0004	MISC_CTRL1	0x0002_5101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				a7_hs_mem_adjust																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27:0]	RW	a7_hs_mem_adjust	A7 CPU high-speed memory speed adjustment control

MISC_CTRL2

MISC_CTRL2 is an A7 CPU status register.

Offset Address	Register Name	Total Reset Value
0x0008	MISC_CTRL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													a7_standbywfi_l2	a7_standbywfi	a7_standbywfe
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RO	a7_standbywfi_l2	Whether the A7 L2 buffer is in wait for interrupt (WFI) status 0: no 1: yes
[1]	RO	a7_standbywfi	Whether the A7 CPU is in WFI status 0: no 1: yes
[0]	RO	a7_standbywfe	Whether the A7 CPU is in wait for event (WFE) status 0: no 1: yes

MISC_CTRL4

MISC_CTRL4 is peripheral function selection register 1.

Offset Address	Register Name	Total Reset Value
0x0010	MISC_CTRL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											phy_test_reg_access	jtag_sel		reserved		test_clk_sel				rom_pgen	reserved							ram0_ck_gt_en			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20]	RW	phy_test_reg_access	Access mode of the USB 2.0 PHY/SATA 3.0 PHY register 0: This register is accessed through the configuration of other registers. 1: This register is accessed through the bus.
[19:18]	RW	jtag_sel	JTAG function select 00: CPU 01: SATA PHY 0 10: SATA PHY 1
[17:16]	RO	reserved	Reserved
[15:12]	RW	test_clk_sel	TSET_CLK_OUT test clock select 0: pll_test_out0 1: pll_test_out1 2: pll_test_out2 3: pll_test_out3 4: pll_test_out4 5: clk_test_out0 6: clk_test_out1 7: clk_test_out2 8: clk_24m 9: clk_rtc_out Other values: reserved
[11]	RW	rom_pgen	SYSROM power supply enable 0: The internal ROM supplies power. 1: The internal ROM does not supply power.
[10:1]	RO	reserved	Reserved

[0]	RW	ram0_ck_gt_en	SYSRAM slice 0 clock gating enable 0: disabled. The internal SYSRAM slice 0 clock is always enabled. 1: enabled. The internal SYSRAM slice 0 clock is dynamically gated.

MISC_CTRL5

MISC_CTRL5 is an SSP control register.

Offset Address	Register Name	Total Reset Value
0x0014	MISC_CTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ssp_cs_pol_ctrl	ssp_cs_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	ssp_cs_pol_ctrl	Polarity control of the SPI CS 0: The SPI CS is active low. 1: The SPI CS is active high.
[0]	RW	ssp_cs_sel	SPI CS select 0: SPI_CSN0 1: SPI_CSN1

MISC_CTRL6

MISC_CTRL6 is system bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0018	MISC_CTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sys_timeout_en_m2	sys_timeout_value_m2															sys_timeout_en_m1	sys_timeout_value_m1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sys_timeout_en_m2	Timeout count enable for the system bus M2 port (AHB_SUBSYS) 0: disabled 1: enabled
[30:16]	RW	sys_timeout_value_m2	Timeout count value of the system bus M2 port (AHB_SUBSYS) Count value = sys_timeout_value_m2 x 2
[15]	RW	sys_timeout_en_m1	Timeout count enable for the system bus M1 port (CPU) 0: disabled 1: enabled
[14:0]	RW	sys_timeout_value_m1	Timeout count value of the system bus M1 port (CPU) Count value = sys_timeout_value_m1 x 2

MISC_CTRL8

MISC_CTRL8 is system bus port priority register 0.

Offset Address	Register Name	Total Reset Value
0x0020	MISC_CTRL8	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									sysaxi_port1_pri_in				reserved			sysaxi_port0_pri_in			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	sysaxi_port1_pri_in	Bus access priority of the system bus M2 port The value 1 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	sysaxi_port0_pri_in	Bus access priority of the system bus M1 port The value 1 indicates the highest priority.

MISC_CTRL9

MISC_CTRL9 is system bus port priority register 1.

Offset Address	Register Name	Total Reset Value
0x0024	MISC_CTRL9	0x0000_1234

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												sysaxi_priority_s5				reserved			sysaxi_priority_s4			reserved			sysaxi_priority_s3			reserved			sysaxi_priority_s2			reserved			sysaxi_priority_s1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved

[18:16]	RW	sysaxi_priority_s5	Bus access priority of the system bus S5 port The value 7 indicates the highest priority.
[15]	RO	reserved	Reserved
[14:12]	RW	sysaxi_priority_s4	Bus access priority of the system bus S4 port The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved
[10:8]	RW	sysaxi_priority_s3	Bus access priority of the system bus S3 port The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved
[6:4]	RW	sysaxi_priority_s2	Bus access priority of the system bus S2 port The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	sysaxi_priority_s1	Bus access priority of the system bus S1 port The value 7 indicates the highest priority.

MISC_CTRL10

MISC_CTRL10 is media 0 bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0028	MISC_CTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media0_timeout_en_m2	media0_timeout_value_m2															media0_timeout_en_m1	media0_timeout_value_m1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media0_timeout_en_m2	Timeout count enable for the media 0 bus M2 port 0: disabled 1: enabled
[30:16]	RW	media0_timeout_value_m2	Timeout count value of the media 0 bus M2 port Count value = media0_timeout_value_m2 x 2

[15]	RW	media0_timeout_en_m1	Timeout count enable for the media 0 bus M1 port 0: disabled 1: enabled
[14:0]	RW	media0_timeout_value_m1	Timeout count value of the media 0 bus M1 port Count value = media0_timeout_value_m1 x 2

MISC_CTRL11

MISC_CTRL11 is media 0 bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x002C	MISC_CTRL11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media0_timeout_en_m4	media0_timeout_value_m4															media0_timeout_en_m3	media0_timeout_value_m3														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media0_timeout_en_m4	Timeout count enable for the media 0 bus M4 port 0: disabled 1: enabled
[30:16]	RW	media0_timeout_value_m4	Timeout count value of the media 0 bus M4 port Count value = media0_timeout_value_m4 x 2
[15]	RW	media0_timeout_en_m3	Timeout count enable for the media 0 bus M3 port 0: disabled 1: enabled
[14:0]	RW	media0_timeout_value_m3	Timeout count value of the media 0 bus M3 port Count value = media0_timeout_value_m3 x 2

MISC_CTRL12

MISC_CTRL12 is media 0 bus arbitration control register 2.

Offset Address	Register Name	Total Reset Value
0x0030	MISC_CTRL12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																media0_timeout_en_m5	media0_timeout_value_m5															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	media0_timeout_en_m5	Timeout count enable for the media 0 bus M5 port 0: disabled 1: enabled
[14:0]	RW	media0_timeout_value_m5	Timeout count value of the media 0 bus M5 port Count value = media0_timeout_value_m5 x 2

MISC_CTRL13

MISC_CTRL13 is a media 0 bus priority register.

Offset Address	Register Name	Total Reset Value
0x0034	MISC_CTRL13	0x0000_1234

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												media0_port4_pri_in				reserved	media0_port3_pri_in			reserved	media0_port2_pri_in			reserved	media0_port1_pri_in			reserved	media0_port0_pri_in		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved

[18:16]	RW	media0_port4_pri_in	Bus access priority of the media 0 bus M5 port The value 7 indicates the highest priority.
[15]	RO	reserved	Reserved
[14:12]	RW	media0_port3_pri_in	Bus access priority of the media 0 bus M4 port The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved
[10:8]	RW	media0_port2_pri_in	Bus access priority of the media 0 bus M3 port The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved
[6:4]	RW	media0_port1_pri_in	Bus access priority of the media 0 bus M2 port The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	media0_port0_pri_in	Bus access priority of the media 0 bus M1 port The value 7 indicates the highest priority.

MISC_CTRL14

MISC_CTRL14 is media 1 bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0038	MISC_CTRL14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media1_timeout_en_m2	media1_timeout_value_m2															media1_timeout_en_m1	media1_timeout_value_m1														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media1_timeout_en_m2	Timeout count enable for the media 1 bus M2 port 0: disabled 1: enabled
[30:16]	RW	media1_timeout_value_m2	Timeout count value of the media 1 bus M2 port Count value = media1_timeout_value_m2 x 2

[15]	RW	media1_timeout_en_m1	Timeout count enable for the media 1 bus M1 port 0: disabled 1: enabled
[14:0]	RW	media1_timeout_value_m1	Timeout count value of the media 1 bus M1 port Count value = media1_timeout_value_m1 x 2

MISC_CTRL15

MISC_CTRL15 is media 1 bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x003C	MISC_CTRL15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media1_timeout_en_m4				media1_timeout_value_m4												media1_timeout_en_m3				media1_timeout_value_m3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media1_timeout_en_m4	Timeout count enable for the media 1 bus M4 port 0: disabled 1: enabled
[30:16]	RW	media1_timeout_value_m4	Timeout count value of the media 1 bus M4 port Count value = media1_timeout_value_m4 x 2
[15]	RW	media1_timeout_en_m3	Timeout count enable for the media 1 bus M3 port 0: disabled 1: enabled
[14:0]	RW	media1_timeout_value_m3	Timeout count value of the media 1 bus M3 port Count value = media1_timeout_value_m3 x 2

MISC_CTRL16

MISC_CTRL16 is media 1 bus arbitration control register 2.

Offset Address	Register Name	Total Reset Value
0x0040	MISC_CTRL16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media1_timeout_en_m6				media1_timeout_value_m6												media1_timeout_en_m5				media1_timeout_value_m5											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media1_timeout_en_m6	Timeout count enable for the media 1 bus M6 port 0: disabled 1: enabled
[30:16]	RW	media1_timeout_value_m6	Timeout count value of the media 1 bus M6 port Count value = media1_timeout_value_m6 x 2
[15]	RW	media1_timeout_en_m5	Timeout count enable for the media 1 bus M5 port 0: disabled 1: enabled
[14:0]	RW	media1_timeout_value_m5	Timeout count value of the media 1 bus M5 port Count value = media1_timeout_value_m5 x 2

MISC_CTRL17

MISC_CTRL17 is a media 1 bus priority register.

Offset Address	Register Name	Total Reset Value
0x0044	MISC_CTRL17	0x0001_2345

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											media1_port5_pri_in	reserved	media1_port4_pri_in			reserved	media1_port3_pri_in			reserved	media1_port2_pri_in			reserved	media1_port1_pri_in			reserved	media1_port0_pri_in		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22:20]	RW	media1_port5_pri_in	Bus access priority of the media 1 bus M6 port (MDU) The value 7 indicates the highest priority.
[19]	RO	reserved	Reserved
[18:16]	RW	media1_port4_pri_in	Bus access priority of the media 1 bus M5 port (AIAO) The value 7 indicates the highest priority.
[15]	RO	reserved	Reserved
[14:12]	RW	media1_port3_pri_in	Bus access priority of the media 1 bus M4 port (JPGE) The value 7 indicates the highest priority.
[11]	RO	reserved	Reserved
[10:8]	RW	media1_port2_pri_in	Bus access priority of the media 1 bus M3 port (VOIE) The value 7 indicates the highest priority.
[7]	RO	reserved	Reserved
[6:4]	RW	media1_port1_pri_in	Bus access priority of the media 1 bus M2 port (VPSS) The value 7 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	media1_port0_pri_in	Bus access priority of the media 1 bus M1 port (ACV1) The value 7 indicates the highest priority.

MISC_CTRL18

MISC_CTRL18 is HP_PERI bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0048	MISC_CTRL18	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hp_peri_timeout_en_m2				hp_peri_timeout_value_m2												hp_peri_timeout_en_m1				hp_peri_timeout_value_m1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hp_peri_timeout_en_m2	Timeout count enable for the HP_PERI bus M2 port 0: disabled 1: enabled
[30:16]	RW	hp_peri_timeout_value_m2	Timeout count value of the HP_PERI bus M2 port Count value = hp_peri_timeout_value_m2 x 2
[15]	RW	hp_peri_timeout_en_m1	Timeout count enable for the HP_PERI bus M1 port 0: disabled 1: enabled
[14:0]	RW	hp_peri_timeout_value_m1	Timeout count value of the HP_PERI bus M1 port Count value = hp_peri_timeout_value_m1 x 2

MISC_CTRL19

MISC_CTRL19 is HP_PERI bus arbitration control register 1.

Offset Address	Register Name	Total Reset Value
0x004C	MISC_CTRL19	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									hp_peri_port1_pri_in				reserved			hp_peri_port0_pri_in			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	hp_peri_port1_pri_in	Bus access priority of the HP_PERI bus M2 port (SATA) The value 1 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	hp_peri_port0_pri_in	Bus access priority of the HP_PERI bus M1 port (GSF) The value 1 indicates the highest priority.

MISC_CTRL20

MISC_CTRL20 is USB 2.0 control register 0.

Offset Address	Register Name	Total Reset Value
0x0050	MISC_CTRL20	0x000C_33E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										usb2_host_ovrcur_merge	usb2_host_pwr_merge	usb2_host_ovrcur_pol	usb2_host_pwren_pol	reserved	usb2_host_p1_ovrcur_en	usb2_host_p0_ovrcur_en	reserved	usb2_host_p1_pwr_en	usb2_host_p0_pwr_en	reserved	reserved	usb2_host_ena_incr16	usb2_host_ena_incr8	usb2_host_ena_incr4	usb2_host_ena_incrx_align	usb2_host_autoppd_on_overcur	reserved	reserved	usb2_host_app_start_clk	usb2_host_ohci_susp_lgcy	usb2_host_word_if
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	usb2_host_ovrcur_merge	One overcurrent enable for two USB 2.0 ports 0: disabled 1: enabled
[20]	RW	usb2_host_pwr_merge	One power supply enable for two USB 2.0 ports 0: disabled 1: enabled
[19]	RW	usb2_host_ovrcur_pol	Overcurrent protection polarity control for the USB 2.0 port 0: active low 1: active high
[18]	RW	usb2_host_pwren_pol	Power enable polarity control for the USB 2.0 port 0: active low 1: active high
[17]	RO	reserved	Reserved
[16]	RW	usb2_host_p1_ovrcur_en	Overcurrent protection enable for USB 2.0 port 1 0: Overcurrent protection is disabled. 1: Overcurrent protection is enabled.
[15]	RW	usb2_host_p0_ovrcur_en	Overcurrent protection enable for USB 2.0 port 0 0: Overcurrent protection is disabled. 1: Overcurrent protection is enabled.
[14]	RO	reserved	Reserved

[13]	RW	usb2_host_p1_pwr_en	Power shutdown control for USB 2.0 port 1 0: The power is shut down. 1: The output power of the USB 2.0 controller is enabled.
[12]	RW	usb2_host_p0_pwr_en	Power shutdown control for USB 2.0 port 0 0: The power is shut down. 1: The output power of the USB 2.0 controller is enabled.
[11]	RO	reserved	Reserved
[10]	RO	reserved	Reserved
[9]	RW	usb2_host_ena_incr16	USB 2.0 burst16 enable 0: disabled 1: enabled
[8]	RW	usb2_host_ena_incr8	USB2.0 controller burst8 enable 0: disabled 1: enabled
[7]	RW	usb2_host_ena_incr4	USB2.0 controller burst4 enable 0: disabled 1: enabled
[6]	RW	usb2_host_ena_incrx_align	USB2.0 controller burst alignment enable 0: disabled 1: enabled
[5]	RW	usb2_host_autoppd_on_overcur	Automatic port power shutdown enable during USB 2.0 controller overcurrent 0: disabled 1: enabled
[4]	RO	reserved	Reserved
[3]	RO	reserved	Reserved
[2]	RW	usb2_host_app_start_clk	USB 2.0 OHCI clock control signal 0 (default): The OHCI works properly. 1: The OHCI clock is enabled in suspend mode.
[1]	RW	usb2_host_ohci_susp_lgcy	Strap input signal when the USB 2.0 OHCI is suspended
[0]	RW	usb2_host_word_if	Data bit width select of the USB 2.0 host UTMI interface 0: 8 bits 1: 16 bits

MISC_CTRL21

MISC_CTRL21 is USB 2.0 control register 1.

Offset Address	Register Name	Total Reset Value
0x0054	MISC_CTRL21	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								usb2_phy_test_rddata								usb2_phy_test_wrdata								reserved		usb2_phy_test_wren		usb2_phy_test_addr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RO	usb2_phy_test_rddata	Read data of the USB 2.0 PHY test register
[15:8]	RW	usb2_phy_test_wrdata	Write data of the USB 2.0 PHY test register
[7:6]	RO	reserved	Reserved
[5]	RW	usb2_phy_test_wren	Read/Write control for the USB 2.0 PHY test register 0: read enable 1: write enable
[4:0]	RW	usb2_phy_test_addr	Address of the USB 2.0 PHY test register

MISC_CTRL22

MISC_CTRL22 is SATA PHY 0 control register 0.

Offset Address	Register Name	Total Reset Value
0x0058	MISC_CTRL22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sata_phy0_crdatain																reserved												sata_phy0_crwrite	sata_phy0_crread	sata_phy0_crcapdata	sata_phy0_crcapaddr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	sata_phy0_crdatain	Address and write data input for the SATA PHY 0 control register
[15:4]	RO	reserved	Reserved
[3]	RW	sata_phy0_crwrite	Write enable for the SATA PHY 0 control register, active high
[2]	RW	sata_phy0_crread	Read enable for the SATA PHY 0 control register, active high
[1]	RW	sata_phy0_crcapdata	Data capture enable for the SATA PHY 0 control register, active high
[0]	RW	sata_phy0_crcapaddr	Address capture enable for the SATA PHY 0 control register, active high

MISC_CTRL23

MISC_CTRL23 is SATA PHY 0 control register 1.

Offset Address	Register Name	Total Reset Value
0x005C	MISC_CTRL23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sata_phy0_crdataout																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	sata_phy0_crdataout	Data output for the SATA PHY 0 control register

MISC_CTRL24

MISC_CTRL24 is SATA PHY 0 control register 2.

Offset Address	Register Name	Total Reset Value
0x0060	MISC_CTRL24	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												sata_phy0_acjt_level			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	sata_phy0_acjt_level	RX sensitivity level of the SATA PHY 0 JTAG interface

MISC_CTRL25

MISC_CTRL25 is SATA PHY 1 control register 0.

Offset Address	Register Name	Total Reset Value
0x0064	MISC_CTRL25	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sata_phy1_crdatain																reserved												sata_phy1_crwrite	sata_phy1_crread	sata_phy1_crcapdata	sata_phy1_crcapaddr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	sata_phy1_crdatain	Address and write data input for the SATA PHY 1 control register
[15:4]	RO	reserved	Reserved
[3]	RW	sata_phy1_crwrite	Write enable for the SATA PHY 1 control register, active high
[2]	RW	sata_phy1_crread	Read enable for the SATA PHY 1 control register, active high
[1]	RW	sata_phy1_crcapdata	Data capture enable for the SATA PHY 1 control register, active high

[0]	RW	sata_phy1_crcapaddr	Address capture enable for the SATA PHY 1 control register, active high

MISC_CTRL26

MISC_CTRL26 is SATA PHY 1 control register 1.

Offset Address	Register Name	Total Reset Value
0x0068	MISC_CTRL26	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sata_phy1_crdataout																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	sata_phy1_crdataout	Data output for the SATA PHY 1 control register

MISC_CTRL27

MISC_CTRL27 is SATA PHY 1 control register 2.

Offset Address	Register Name	Total Reset Value
0x006C	MISC_CTRL27	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												sata_phy1_acjt_level			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	sata_phy1_acjt_level	RX sensitivity level of the SATA PHY 1 JTAG interface

MISC_CTRL28

MISC_CTRL28 is an SATA loopback control register.

Offset Address	Register Name	Total Reset Value
0x0070	MISC_CTRL28	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										sata_lpbk_mode_sel1	sata_lpbk_mode_sel0	reserved				sata_lpbk_ctrl_en1	sata_lpbk_ctrl_en0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	sata_lpbk_mode_sel1	Loopback mode select for SATA port 1 0: forcible loopback 1: data matching loopback
[4]	RW	sata_lpbk_mode_sel0	Loopback mode select for SATA port 0 0: forcible loopback 1: data matching loopback
[3:2]	RO	reserved	Reserved
[1]	RW	sata_lpbk_ctrl_en1	Loopback enable for SATA port 1 0: disabled 1: enabled
[0]	RW	sata_lpbk_ctrl_en0	Loopback enable for SATA port 0 0: disabled 1: enabled

MISC_CTRL29

MISC_CTRL29 is an SATA port 0 loopback configuration register.

Offset Address	Register Name	Total Reset Value
0x0074	MISC_CTRL29	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sata_lpbk_match_cfg0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sata_lpbk_match_cfg0	Loopback configuration for SATA port 0

MISC_CTRL30

MISC_CTRL30 is an SATA port 1 loopback configuration register.

Offset Address	Register Name	Total Reset Value
0x0078	MISC_CTRL30	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sata_lpbk_match_cfg1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sata_lpbk_match_cfg1	Loopback configuration for SATA port 1

MISC_CTRL31

MISC_CTRL31 is DDQ QoS control register 0.

Offset Address	Register Name	Total Reset Value
0x007C	MISC_CTRL31	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vgs_qos				jpgd_qos				ive_qos				tde_qos				avc0_qos				a7_qos				vdp_qos				vicap_qos			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	vgs_qos	QoS mapping value of the VGS in the MDDRC
[27:24]	RW	jpgd_qos	QoS mapping value of the JPGD in the MDDRC
[23:20]	RW	ive_qos	QoS mapping value of the IVE in the MDDRC
[19:16]	RW	tde_qos	QoS mapping value of the TDE in the MDDRC

[15:12]	RW	avc0_qos	QoS mapping value of the AVC0 in the MDDRC
[11:8]	RW	a7_qos	QoS mapping value of the A7 in the MDDRC
[7:4]	RW	vdp_qos	QoS mapping value of the VDP in the MDDRC
[3:0]	RW	vicap_qos	QoS mapping value of the VICAP in the MDDRC

MISC_CTRL32

MISC_CTRL32 is DDQ QoS control register 1.

Offset Address	Register Name	Total Reset Value
0x0080	MISC_CTRL32	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	gsf_qos	ddrt_qos	avc1_qos	vpss_qos	voie_qos	jpge_qos	aio_qos	mdu_qos
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	gsf_qos	QoS mapping value of the GSF in the MDDRC
[27:24]	RW	ddrt_qos	QoS mapping value of the DDRT in the MDDRC
[23:20]	RW	avc1_qos	QoS mapping value of the AVC1 in the MDDRC
[19:16]	RW	vpss_qos	QoS mapping value of the VPSS in the MDDRC
[15:12]	RW	voie_qos	QoS mapping value of the VOIE in the MDDRC
[11:8]	RW	jpge_qos	QoS mapping value of the JPGE in the MDDRC
[7:4]	RW	aio_qos	QoS mapping value of the AIAO in the MDDRC
[3:0]	RW	mdu_qos	QoS mapping value of the MDU in the MDDRC

MISC_CTRL33

MISC_CTRL33 is DDQ QoS control register 2.

Offset Address	Register Name	Total Reset Value
0x0084	MISC_CTRL33	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	dma_m1_qos	dma_m0_qos	fmc_qos	usb2_qos	cipher_qos	scd_qos	sata_qos
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27:24]	RW	dma_m1_qos	QoS mapping value of DMA master 1 in the MDDRC
[23:20]	RW	dma_m0_qos	QoS mapping value of DMA master 0 in the MDDRC
[19:16]	RW	fmc_qos	QoS mapping value of the FMC in the MDDRC
[15:12]	RW	usb2_qos	QoS mapping value of USB 2.0 in the MDDRC
[11:8]	RW	cipher_qos	QoS mapping value of the cipher in the MDDRC
[7:4]	RW	scd_qos	QoS mapping value of the SCD in the MDDRC
[3:0]	RW	sata_qos	QoS mapping value of the SATA in the MDDRC

MISC_CTRL36

MISC_CTRL36 is VIVO bus arbitration control register 0.

Offset Address	Register Name	Total Reset Value
0x0090	MISC_CTRL36	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vivo_timeout_en_m2				vivo_timeout_value_m2												vivo_timeout_en_m1				vivo_timeout_value_m1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vivo_timeout_en_m2	Timeout count enable for the VIVO bus M2 port 0: disabled 1: enabled
[30:16]	RW	vivo_timeout_value_m2	Timeout count value of the VIVO bus M2 port Count value = media0_timeout_value_m2 x 2
[15]	RW	vivo_timeout_en_m1	Timeout count enable for the VIVO bus M1 port 0: disabled 1: enabled
[14:0]	RW	vivo_timeout_value_m1	Timeout count value of the VIVO bus M1 port Count value = media0_timeout_value_m1 x 2

MISC_CTRL37

MISC_CTRL37 is a VIVO bus priority register.

Offset Address	Register Name	Total Reset Value
0x0094	MISC_CTRL37	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									vivo_port1_pri_in			reserved	vivo_port0_pri_in		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:4]	RW	vivo_port1_pri_in	Bus access priority of the VIVO bus M2 port (VO) The value 1 indicates the highest priority.
[3]	RO	reserved	Reserved
[2:0]	RW	vivo_port0_pri_in	Bus access priority of the VIVO bus M1 port (VI) The value 1 indicates the highest priority.

3.6 DMA Controller

3.6.1 Overview

The DMA operation is a high-speed data transfer operation. It supports data read/write between peripherals and memories without using the CPU. The direction memory access controller (DMAC) directly transfers data between a memory and a peripheral, between peripherals, or between memories. This avoids the CPU intervention and reduces the interrupt handling overhead of the CPU.

3.6.2 Features

The DMAC has the following features:

- Transfers data in 8-bit, 16-bit, or 32-bit mode.
- Provides four DMA channels. Each channel can be configured to support unidirectional transfer.
- Provides two 32-bit master bus interfaces for data transfer.
- Supports the DMA requests controlled through software.

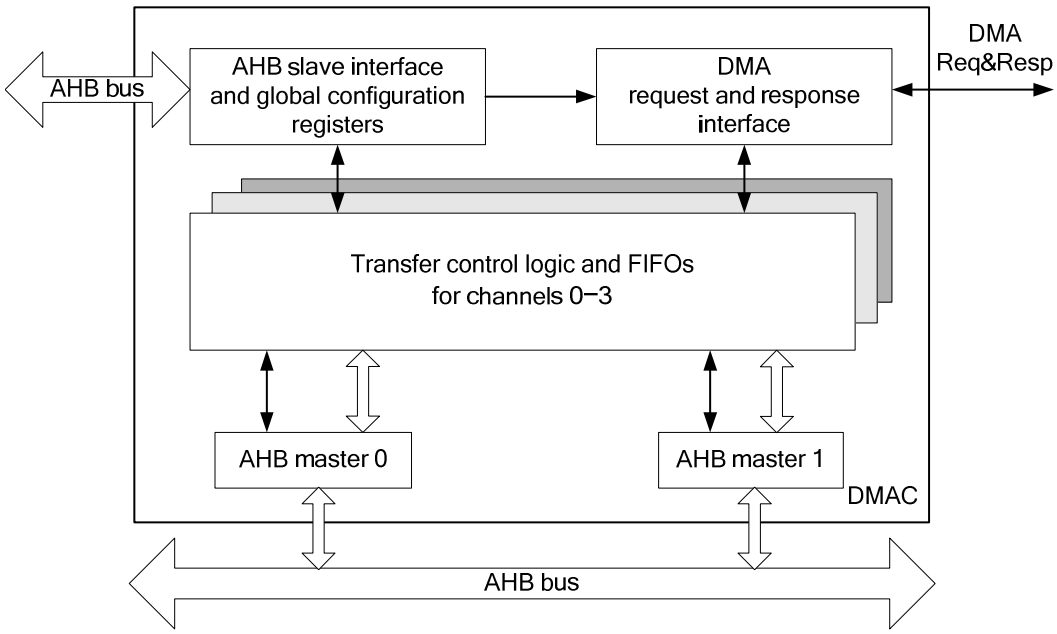
- Programs the DMA burst size.
- Configures the source address and the destination address as automatic incremental or decremented addresses during DMA transfer.
- Supports DMA transfer with the linked list.
- Supports the DMAC flow control.
- Supports four data transfer directions:
  - Memory to peripheral
  - Memory to memory
  - Peripheral to memory
  - Peripheral to peripheral
- Supports two types of DMA requests for peripherals: single transfer request and burst transfer request.
- Provides a maskable interrupt output and supports the query of the statuses of the raw/masked DMA error interrupt and DMA transfer completion interrupt and the status of the combination of the two interrupts.

3.6.3 Function Description

Functional Block Diagram

Figure 3-5 shows the functional block diagram of the DMAC.

Figure 3-5 Functional block diagram of the DMAC



NOTE

- The priorities of DMAC channels are fixed. DMA channel 0 has the highest priority; whereas channel 3 has the lowest priority. When the DMA requests from two peripherals are valid simultaneously, the channel with the higher priority starts data transfer first.
- DMA channel 0 and DMA channel 1 have one 4 x 32-bit FIFO each, and DMA channel 2 and DMA channel 3 have one 16 x 32-bit FIFO each.

Each DMA channel has a group of transfer control logic and one FIFO. The transfer control logic automatically performs the following operations:

Step 1 Read data from the source address specified by the software.

Step 2 Buffer data in the FIFO.

Step 3 Fetch data from the FIFO.

Step 4 Write the data to the destination address specified by the software.

----End

Workflow

The workflow of the DMAC is as follows:

Step 1 The software selects one DMA channel for DMA transfer, configures the following items, and enables the channel:

- Source address
- Destination address
- Header pointer of the linked list
- Amount of the transferred data
- Source and destination peripheral request signal numbers
- Masters used at the source and destination ends of the channel.

After the channel is enabled, the DMAC starts to check the activities of the DMA request lines of the source peripheral and destination device connected to this channel.

Step 2 The source device transmits a DMA request to the DMAC. If the source device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 3 The DMAC channel responds to the DMA request of the source device. Then the DAMC reads data from the source device and stores it in the internal FIFO of the channel.

Step 4 The destination device transmits a DMA request to the DMAC. If the destination device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 5 The DMA channel responds to the DMA request of the destination device. Then the DMAC fetches data from the internal FIFO of the channel and writes it to the destination device.

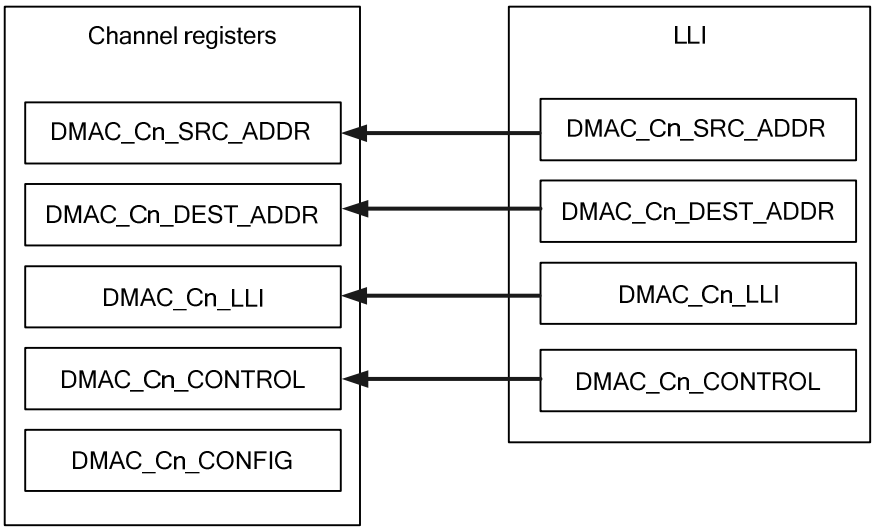
Step 6 The steps 2 and step 3 as well as step 4 and 5 may be performed concurrently, because the source and destination devices may transmit DMA requests to the DMAC at the same time. When the FIFO overrun or underrun occurs on the DMA channel, the DMAC blocks the DMA requests of the source device or destination device until the FIFO is full or empty. When the DMAC interacts with the source device and destination device for several times, step 2 to step 5 are performed repeatedly until the specified data is completely transferred and a maskable transfer terminal interrupt is sent. If the value of DMAC_Cn_LLI is not 0, read linked list item (LLI) nodes by considering the register value as an address, load the read

values to DMAC_Cn_SRC_ADDR, DMAC_Cn_DEST_ADDR, DMAC_Cn_LLI, and DMAC_Cn_CONTROL in sequence (see Figure 3-5), and then go to step 2. If the value of DMAC_Cn_LLI is 0, the current DMA transfer is stopped. In this case, the channel is disabled automatically and the transfer ends.

----End

Figure 3-6 illustrates how to update channel registers through the LLI.

Figure 3-6 Updating channel registers through the LLI

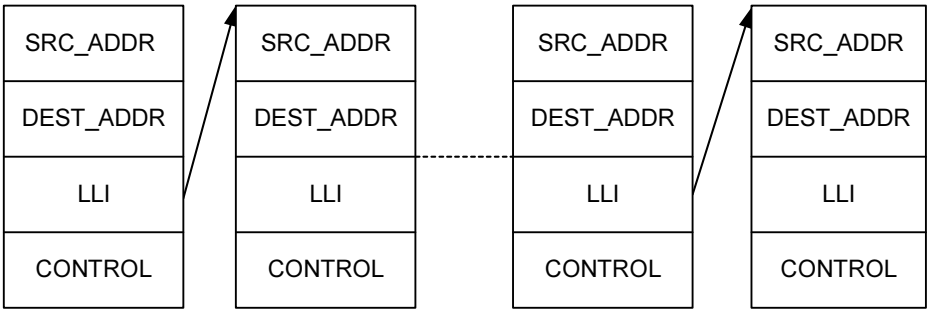


DMA Linked List

The data structure of the DMAC LLI node is as follows:

- Channel register DMAC_Cn_SRC_ADDR, for setting the start address for the source device
- Channel register DMAC_Cn_DEST_ADDR, for setting the start address for the destination device
- Channel register DMAC_Cn_LLI, for setting the address for the next node
- Channel register DMAC_Cn_CONTROL, for setting the master, data width, burst size, address increment, and transfer size of the source device and destination device

Figure 3-7 Structure of DMAC LLIs



CAUTION

The LLI field value must be less than or equal to 0xFFFF_FFF0. Otherwise, the address is wrapped around to 0x0000_0000 during a 4-word burst transfer. As a result, the data structure of LLI nodes cannot be stored in a consecutive address area.

If the LLI field is set to 0, the current node is at the end of the linked list. In this case, the corresponding channel is disabled after data blocks corresponding to the current node are transferred.

Connection Between the DMA and Peripherals

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC.

The DMAC provides the following two DMA request signals for each peripheral:

- DMACBREQ

  Burst transfer request signal. It triggers a burst transfer and the burst size is preconfigured.
- DMACSREQ

  Single transfer request signal. It triggers a single transfer. That is, the DMAC reads a data segment from a peripheral or writes a data segment to a peripheral.

The DMAC provides a request clear signal DMACLR.

This signal is sent to each peripheral by the DMAC as a response to the DMA request signal of each peripheral.

DMAC Request Signals

Table 3-10 describes the mapping between DMAC hardware request signal IDs and peripherals.

Table 3-10 DMAC hardware request signals and corresponding peripherals

DMAC Hardware Request Signal ID	Peripherals
0	UART0 RX channel
1	UART0 TX channel
2	UART1 RX channel
3	UART1 TX channel
4	UART2 RX channel
5	UART2 TX channel
6	SSP RX channel
7	SSP TX channel

DMAC Hardware Request Signal ID	Peripherals
8	I^2C RX channel
9	I^2C TX channel
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved

The source and destination requests of each DMA channel are configured by software. For example, DMA request 0 is the request of the UART0 RX channel. To transmit the UART0 RX data by using channel 3, you must configure DMA request 0 as the source request of channel 3.

As memories do not provide DMA request signals, when a memory is used for DMA transfer, the DMAC considers that the DMA request of the memory is always valid by default. In addition, an idle cycle is inserted after each bus operation during the DMAC transfer on channel 2 or channel 3. In this way, the Master with a higher priority channel can transfer data on the bus first. Therefore, to avoid other channels waiting for the bus for a long time, it is recommended that data be transmitted from memory to memory using channel 2 or channel 3.

3.6.4 Operating Mode

Clock Gating

In the following cases, the DMAC and DMAC clock can be disabled using the software to reduce power consumption:

- All DMA channels are idle and there is no DMA transfer request.
- DMAC_Cn_CONFIG[ch_en] is set to 0 and all the DMA channels are disabled.

To disable the DMAC clock, perform the following steps:

Step 1 Write 0 to DMAC_Cn_CONFIG[ch_en] to disable DMAC channels.

Step 2 Write 0 to DMAC_CONFIG [dmac_enable] to disable the DMAC.

Step 3 Write 0 to PERI_CRG32 [5] to disable DMAC bus clock gating. Then the DMAC clock is disabled.

Step 4 Enable the clock and the DMAC again when the DMAC is required for data transfer.

----End

Initialization

To initialize the DMAC, perform the following steps:

Step 1 Write to DMAC_CONFIG to set the endianness of DMAC master 1 and DMAC master 2, and write 1 to DMAC_CONFIG[dmac_enable] to enable the DMAC.

Step 2 Write 1 to all the bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear all interrupts.

Step 3 Write 0 to the corresponding bits of DMAC_SYNC to set the DMA request signal groups to be synchronized.

Step 4 Configure and disable channels in sequence. You can disable all the channels by writing 0 to DMAC_Cn_CONFIG[ch_en] of each channel.

----End

Enabling a Channel

After the DMAC is initialized, the DMAC can transmit data only when a DMAC channel is configured and enabled. To enable a DMA channel, perform the following steps:

Step 1 Read DMAC_ENABLED_CHNS to search for idle channels and select one.

Step 2 Write 1 to the corresponding bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear the interrupt status of the selected channel.

Step 3 Write to DMAC_Cn_SRC_ADDR to set the access start address for the source device.

Step 4 Write to DMAC_Cn_DEST_ADDR to set the access start address for the destination device.

Step 5 Write to DMAC_Cn_LLI to set the linked list information. If the channel is used for single-block data transfer, set DMAC_Cn_LLI to 0. If the channel is used for linked list data transfer, set DMAC_Cn_LLI to the linked list header pointer.

Step 6 Write to DMAC_Cn_CONTROL to set the master, data width, burst size, address increment, and transfer size of the source device and destination device.

Step 7 Write to DMAC_Cn_CONFIG to set the DMA request signal, flow control mode, and interrupt mask of this channel.

Step 8 Write 1 to DMAC_Cn_CONFIG[ch_en] to enable this channel.

----End

Usage of DMAC_Cn_CONTROL

The DMAC_Cn_CONTROL register contains the control information about the DMA channels, such as the transfer size, burst size, and transfer bit width.

Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register value is updated when being loaded from an LLI node after a complete data block is transferred.

If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. As a result, the register can be read after the channel stops data transfer.

Table 3-11 lists the mapping between the value of dbsize or sbsize of DMAC_Cn_CONTROL and the burst length.

Table 3-11 Mapping between the value of dbsize or sbsize and the burst length

Value of bsize or sbSize	Burst Length
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Table 3-12 describes mapping between the value of dwidth or swidth of DMAC_Cn_CONTROL and the transfer data width.

Table 3-12 Mapping between the value of dwidth or swidth and the transfer bit width

Value of swidth or dwidth	Transfer Bit Width
000	Byte (8 bits)
001	Halfword (16 bits)
010	Word (32 bits)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Note the following when configuring DMAC_Cn_CONTROL:

- When the transfer bit width of the source device is smaller than that of the destination device, the product of the transfer bit width and transfer size of the source device must be an integral multiple of the transfer bit width of the destination device. Otherwise, data retention and data loss occur in the FIFO.
- swidth and dwidth fields cannot be set to undefined bit widths.
- If the transfer size field is set to 0 and the DMAC is a flow controller, the DMAC does not transfer data. In this case, the programmer needs to disable the DMA channel and reprogram it.
- Never conduct common write/read tests on the DMAC_Cn_CONTROL register, because the transfer size field is different from the common register field whose written value and read value may be the same. During the write operation, this field serves as a control

register, because it determines the number of data segments transferred by the DMAC. During the read operation, this field serves as a status register, because it returns the number (in the unit of the bit width of the source device) of the remaining data segments to be transferred.

- When the transfer size field is set to a value greater than the depth of the FIFO (peripheral FIFO but not the DMAC FIFO) of the source device or destination device, the mode of DMAC source address or destination address must be set to non-incremental mode. Otherwise, the peripheral FIFO may overflow.

Usage of DMAC_Cn_CONFIG

Table 3-13 describes the flow controllers and transfer types corresponding to the flow_cntrl field of DMAC_Cn_CONFIG.

Table 3-13 Flow controllers and transfer types corresponding to the flow_cntrl field

Bit Value	Transfer Mode	Controller
000	Memory to memory	DMAC
001	Memory to peripheral	DMAC
010	Peripheral to memory	DMAC
011	Source device to destination device	DMAC
100	Source device to destination device	Destination device
101	Memory to peripheral	Destination device
110	Peripheral to memory	Source device
111	Source device to destination device	Source device

Interrupt Handling

When data transfer is complete or an error occurs during data transfer, interrupts are reported to the interrupt controller. An interrupt is handled as follows:

Step 1 Read DMAC_INT_STAT to find the channel that transmits an interrupt request. When multiple channels initiate interrupt requests at the same time, the interrupt request with the highest priority is handled first.

Step 2 Read DMAC_INT_TC_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is a transfer terminal interrupt. If the value is 1, the interrupt is a transfer terminal interrupt. In this case, go to step 4; otherwise, go to step 3.

Step 3 Read DMAC_INT_ERR_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is an error interrupt. If the selected bit is 1, the interrupt is an error interrupt. In this case, go to step 5; otherwise, end the operation.

Step 4 Handle the transfer terminal interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_TC_CLR to clear the interrupt status of the corresponding channel.

2. Fetch or use up the data buffered in the memory. If necessary (for example, you need to create a buffer in the memory), configure and enable the channel again.
3. End interrupt handling.

Step 5 Handle the error interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_ERR_CLR to clear the interrupt status of the corresponding channel.
2. Provide the error information. If necessary, configure and enable the channel again.
3. End interrupt handling.

----End

3.6.5 Register Summary

NOTE

The *n* in the offset addresses for DMA registers indicates the DMA channel and its value range is 0–3.

Table 3-14 describes the DMAC registers.

Table 3-14 Summary of the DMAC registers (base address: 0x1006_0000)

Offset Address	Register	Description	Page
0x0000	DMAC_INT_STAT	DMAC interrupt status register	3-112
0x0004	DMAC_INT_TC_STAT	DMAC transfer terminal interrupt status register	3-113
0x0008	DMAC_INT_TC_CLR	DMAC transfer terminal interrupt clear register	3-114
0x000C	DMAC_INT_ERR_STAT	DMAC error interrupt status register	3-114
0x0010	DMAC_INT_ERR_CLR	DMAC error interrupt clear register	3-115
0x0014	DMAC_RAW_INT_TC_STAT	DMAC raw transfer terminal interrupt status register	3-116
0x0018	DMAC_RAW_INT_ERR_STAT	DMAC raw error interrupt status register	3-117
0x001C	DMAC_ENABLED_CHNS	DMAC channel enable status register	3-118
0x0020	DMAC_SOFT_BREQ	DMAC software burst transfer request register	3-119
0x0024	DMAC_SOFT_SREQ	DMAC software single transfer request register	3-120
0x0028	DMAC_SOFT_LBREQ	DMAC software last burst request register	3-121
0x002C	DMAC_SOFT_LSREQ	DMAC software last single request register	3-121

Offset Address	Register	Description	Page
0x0030	DMAC_CONFIG	DMAC configuration register	3-122
0x0034	DMAC_SYNC	DMAC request line sync enable register	3-123
0x0100 + *n* x 0x20	DMAC_Cn_SRC_ADDR	Source address register of DMA channel *n* (*n* = 0−3)	3-123
0x0104 + *n* x 0x20	DMAC_Cn_DEST_ADDR	Destination address register of DMA channel *n* (*n* = 0−3)	3-124
0x0108 + *n* x 0x20	DMAC_Cn_LLI	LLI information register of DMA channel *n* (*n* = 0−3)	3-124
0x010C + *n* x 0x20	DMAC_Cn_CONTROL	Control register of DMA channel *n* (*n* = 0−3)	3-125
0x110 + *n* x 0x20	DMAC_Cn_CONFIG	Configuration register of DMA channel *n* (*n* = 0−3)	3-128

3.6.6 Register Description

DMAC_INT_STAT

DMAC_INT_STAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	DMAC_INT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_stat	ch2_int_stat	ch1_int_stat	ch0_int_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_stat	Masked interrupt status of channel 3 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.

[2]	RO	ch2_int_stat	Masked interrupt status of channel 2 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[1]	RO	ch1_int_stat	Masked interrupt status of channel 1 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[0]	RO	ch0_int_stat	Masked interrupt status of channel 0 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.

DMAC_INT_TC_STAT

DMAC_INT_TC_STAT is a DMAC transfer terminal interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	DMAC_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_tc_stat	ch2_int_tc_stat	ch1_int_tc_stat	ch0_int_tc_stat
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_tc_stat	Status of the masked transfer terminal interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_int_tc_stat	Status of the masked transfer terminal interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_int_tc_stat	Status of the masked transfer terminal interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.

[0]	RO	ch0_int_tc_stat	Status of the masked transfer terminal interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_INT_TC_CLR

DMAC_INT_TC_CLR is a DMAC transfer terminal interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0008	DMAC_INT_TC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_tc_clr	ch2_int_tc_clr	ch1_int_tc_clr	ch0_int_tc_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	ch3_int_tc_clr	Transfer terminal interrupt clear for channel 3 0: not cleared 1: cleared
[2]	WO	ch2_int_tc_clr	Transfer terminal interrupt clear for channel 2 0: not cleared 1: cleared
[1]	WO	ch1_int_tc_clr	Transfer terminal interrupt clear for channel 1 0: not cleared 1: cleared
[0]	WO	ch0_int_tc_clr	Transfer terminal interrupt clear for channel 0 0: not cleared 1: cleared

DMAC_INT_ERR_STAT

DMAC_INT_ERR_STAT is a DMAC error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000C	DMAC_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_stat		ch2_int_err_stat		ch1_int_err_stat		ch0_int_err_stat	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_err_stat	Status of the masked error interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_int_err_stat	Status of the masked error interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_int_err_stat	Status of the masked error interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_int_err_stat	Status of the masked error interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_INT_ERR_CLR

DMAC_INT_ERR_CLR is a DMAC transfer error interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0010	DMAC_INT_ERR_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_clr	ch2_int_err_clr	ch1_int_err_clr	ch0_int_err_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	ch3_int_err_clr	Error interrupt clear for channel 3 0: not cleared 1: cleared
[2]	WO	ch2_int_err_clr	Error interrupt clear for channel 2 0: not cleared 1: cleared
[1]	WO	ch1_int_err_clr	Error interrupt clear for channel 1 0: not cleared 1: cleared
[0]	WO	ch0_int_err_clr	Error interrupt clear for channel 0 0: not cleared 1: cleared

DMAC_RAW_INT_TC_STAT

DMAC_RAW_INT_TC_STAT is a DMAC raw transfer terminal interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0014	DMAC_RAW_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_tc		ch2_raw_int_tc		ch1_raw_int_tc		ch0_raw_int_tc	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_raw_int_tc	Status of the raw transfer terminal interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_raw_int_tc	Status of the raw transfer terminal interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_raw_int_tc	Status of the raw transfer terminal interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_raw_int_tc	Status of the raw transfer terminal interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_RAW_INT_ERR_STAT

DMAC_RAW_INT_ERR_STAT is a DMAC raw error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0018	DMAC_RAW_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_err	ch2_raw_int_err	ch1_raw_int_err	ch0_raw_int_err
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_raw_int_err	Status of the raw error interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_raw_int_err	Status of the raw error interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_raw_int_err	Status of the raw error interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_raw_int_err	Status of the raw error interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_ENABLED_CHNS

DMAC_ENABLED_CHNS is a DMAC channel enable status register.

Offset Address	Register Name	Total Reset Value
0x001C	DMAC_ENABLED_CHNS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_enabled	ch2_enabled	ch1_enabled	ch0_enabled
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_enabled	Channel 3 enable 0: disabled 1: enabled
[2]	RO	ch2_enabled	Channel 2 enable 0: disabled 1: enabled
[1]	RO	ch1_enabled	Channel 1 enable 0: disabled 1: enabled
[0]	RO	ch0_enabled	Channel 0 enable 0: disabled 1: enabled

DMAC_SOFT_BREQ

DMAC_SOFT_BREQ is a DMAC software burst transfer request register.

Software controls the generation of a DMA burst transfer request by using this register.

When this register is read, the device that is requesting the DMA burst transfer can be queried. This register and any peripheral can generate a DMA request each.

Offset Address	Register Name	Total Reset Value
0x0020	DMAC_SOFT_BREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_breq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_breq	Whether to generate a DMA burst transfer request When this register is written: 0: No effect. 1: A DMA burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACBREQ[15:0] does not send any DMA burst request. 1: The peripheral corresponding to the request signal DMACBREQ[15:0] is requesting the DMA burst transfer.

DMAC_SOFT_SREQ

DMAC_SOFT_SREQ is a DMAC software single transfer request register.

Software controls the generation of DMA single transfer requests by using this register.

When this register is read, the device that is requesting the DMA single transfer can be queried. This register and any of the 16 DMA request input signals of the DMAC can generate a DMA request each.

Offset Address	Register Name	Total Reset Value
0x0024	DMAC_SOFT_SREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_sreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	soft_sreq	Whether to generate a DMA single transfer request When this register is written: 0: no effect 1: A DMA single transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACSREQ[15:0] does not send a DMA single request. 1: The peripheral corresponding to the request signal DMACSREQ[15:0] is requesting the DMA single transfer.

DMAC_SOFT_LBREQ

DMAC_SOFT_LBREQ is a DMAC software last burst request register.

Software controls the generation of the DMA last burst transfer requests by using this register.

Offset Address	Register Name	Total Reset Value
0x0028	DMAC_SOFT_LBREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lbreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_lbreq	Last burst request issued by the software 0: no effect 1: A DMA last burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_SOFT_LSREQ

DMAC_SOFT_LSREQ is a DMAC software last single transfer request register.

Software controls the generation of the DMA last single transfer requests by using this register.

Offset Address	Register Name	Total Reset Value
0x002C	DMAC_SOFT_LSREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lsreq																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_lsreq	Last single transfer request issued by the software 0: no effect 1: A DMA last single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_CONFIG

DMAC_CONFIG is a DMAC configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	DMAC_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													m2_endianness	m1_endianness	dmac_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	m2_endianness	Byte endianness of master 2 0: little endian 1: big endian
[1]	RW	m1_endianness	Byte endianness of master 1 0: little endian 1: big endian
[0]	RW	dmac_enable	DMAC enable 0: disabled 1: enabled

DMAC_SYNC

DMAC_SYNC is a DMAC request line sync enable register.

Offset Address	Register Name	Total Reset Value
0x0034	DMAC_SYNC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dmac_sync															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	dmac_sync	Whether to synchronize the request signals 0: The sync logic provided for the DMA request signals of the corresponding peripheral is enabled. 1: The sync logic provided for the DMA request signals of the corresponding peripheral is disabled.

DMAC_Cn_SRC_ADDR

DMAC_Cn_SRC_ADDR is a source address register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x100 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register is updated in any of the following cases:

- The source address is incremented.
- A complete data block is transferred and then loaded from LLI nodes.
- If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last source address read by the DMAC.

Offset Address	Register Name	Total Reset Value
0x0100 + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_SRC_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_addr	DMA source address

DMAC_Cn_DEST_ADDR

DMAC_Cn_DEST_ADDR is a destination address register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x104 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

This register contains the destination address for the data to be transferred. Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register is updated in any of the following cases:

- Destination address increment.
- A complete data block is transferred and then loaded from LLI nodes.
- If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last destination address written by the DMAC.

Offset Address	Register Name	Total Reset Value
0x0104 + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_DEST_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_addr	DMA destination address

DMAC_Cn_LLI

DMAC_Cn_LLI is an LLI information register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x108 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3. For details, see section "DMA Linked List."

Offset Address	Register Name	Total Reset Value
0x0108 + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_LLI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ll_item																														reserved	ll_master
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	ll_item	The bit[31:2] in the next LLI node address and the address bit[1:0] are set to 0. A linked list address must be 4-byte aligned.
[1]	RW	reserved	Reserved. This bit value must be 0 during write operations, and this bit must be masked during read operations.
[0]	RW	ll_master	Master for loading the next LLI node 0: master 1 1: master 2

DMAC_Cn_CONTROL

DMAC_Cn_CONTROL is a control register of DMA channel *n* (*n* = 0–3).

Its offset address is 0x10C + n x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

Offset Address	Register Name	Total Reset Value
0x010C + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_tc_enable	prot_stat			dest_incr	src_incr	dest_select	src_select	dwidth				swidth				dbsize				sbsize				trans_size							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_tc_enable	Transfer terminal interrupt enable. This bit determines whether the current LLI node triggers a transfer terminal interrupt. 0: do not trigger 1: trigger
[30:28]	RW	prot_stat	HPROT[2:0] access protection signal transmitted by the master.
[27]	RW	dest_incr	Destination address increment 0: The destination address is not incremented 1: The destination address is incremented once after a data segment is transferred If the destination device is a peripheral, the destination address is not incremented. If the destination device is a memory, the destination address is incremented.
[26]	RW	src_incr	Source address increment 0: The source address is not incremented 1: The source address is incremented once after a data segment is transferred If the source device is a peripheral, the source address is not incremented. If the source device is a memory, the source address is incremented.
[25]	RW	dest_select	Master for accessing the destination device 0: master 1 1: master 2
[24]	RW	src_select	Master for accessing the source device 0: master 1 1: master 2

[23:21]	RW	dwidth	Transfer bit width of the destination device The transfer bit width is invalid if it is greater than the bit width of the master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For the mapping between the value of dwidth and the bit width, see Table 3-12.
[20:18]	RW	swidth	Transfer bit width of the source device The transfer bit width is invalid if it is greater than the bit width of the master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For the mapping between the value of swidth and the bit width, see Table 3-12.
[17:15]	RW	dbsize	Burst size of the destination device It indicates the number of data segments to be transferred by the destination device in a burst transfer, that is, the number of transferred data segments when DMACCxBREQ is valid. This value must be set to a burst size supported by the destination device. If the destination device is a memory, the value is set to the storage area size beyond the storage address boundary. For the mapping between the value of dbsize and the transfer length, see Table 3-11.
[14:12]	RW	sbsize	Burst size of the source device It indicates the amount of data to be transferred by the source device in a burst transfer, that is, the amount of transferred data when DMACCxBREQ is valid. The value must be set to a burst size supported by the source device. If the source device is a memory, the value is set to the storage area size beyond the storage address boundary. For the mapping between the value of sbsize and the transfer length, see Table 3-11.
[11:0]	RW	trans_size	The DMA transfer size can be configured by writing to this register only when the DMAC is a flow controller. The field indicates the amount of data to be transferred by the source device. When this register is read, the amount of data transferred through the bus connected to the destination device is obtained. If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel is enabled and data transfer stops.

DMAC_Cn_CONFIG

DMAC_Cn_CONFIG is a configuration register of channel *n* (*n* = 0−3).

Its offset address is 0x110 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

This register is not updated when a new LLI node is loaded.

Offset Address	Register Name	Total Reset Value
0x110 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													ch_halt	ch_active	ch_lock	tc_int_msk	err_int_msk	flow_ctrl		reserved		dest_periph		reserved		src_periph		ch_en			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[18]	RW	ch_halt	Halt bit 0: The DMA request is allowed. 1: The subsequent DMA requests are ignored and the contents in the channel FIFO are completely transmitted. This bit can disable a DMA channel without data loss by working with the Active bit and the Channel Enable bit.
[17]	RW	ch_active	Active bit 0: There is no data in the channel FIFO. 1: There is data in the channel FIFO. This bit can disable a DMA channel without data loss by working with the Halt bit and Channel Enable bit.
[16]	RW	ch_lock	Lock bit 0: Lock transfer on the bus is disabled. 1: Lock transfer on the bus is enabled.
[15]	RW	tc_int_msk	Transfer terminal interrupt mask 0: The transfer terminal interrupts of the channel are masked. 1: The transfer terminal interrupts of the channel are not masked.

[14]	RW	err_int_msk	Transfer error interrupt mask 0: The error interrupts of the channel are masked. 1: The error interrupts of the channel are not masked.
[13:11]	RW	flow_ctrl	Flow control and transfer type This field specifies the flow controller and transfer type. The flow controller can be the DMAC, source device, or destination device. The transfer type can be memory to peripheral, peripheral to memory, peripheral to peripheral, or memory to memory. For details, see Table 3-13.
[10]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[9:6]	RW	dest_periph	Destination device. The field is used to select a peripheral request signal as the request signal for the DMA destination device of the channel. If the destination device for DMA transfer is a memory, this field is ignored.
[5]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[4:1]	RW	src_periph	Source device. This field is used to select a peripheral request signal as the request signal for the DMA source device of the channel. If the source device for DMA transfer is a memory, this field is ignored.
[0]	RW	ch_en	Channel enable. The current status of the channel can be queried by reading this field or DMAC_ENABLED_CHNS. 0: disabled 1: enabled Clearing this bit can disable a channel. When this bit is cleared, the current bus transfer continues until the data transfer is complete. Then, the channel is disabled and the remaining data in the FIFO is lost. When the last LLI node is transferred or an error occurs during transfer, the channel is also disabled and this bit is cleared. If you want to disable a channel without data loss, the Halt bit must be set to 1 so the subsequent DMA requests are ignored by the channel. After this, the Active bit must be polled until its value becomes 0, indicating that there is no data in the channel FIFO. At this time, the Enable bit can be cleared. Before enabling a channel by setting this bit to 1, you must reinitialize the channel; otherwise, unexpected results may occur. When a channel is disabled by writing DMAC_Cn_CONFIG [ch_en], DMAC_Cn_CONFIG [ch_en] can be reset again only after the corresponding bit of DMAC_ENABLED_CHNS is 0. This is because the channel is not disabled immediately after the Channel Enable bit is cleared. The running delay during a bus

			burst operation also needs to be considered.

3.7 Cipher

3.7.1 Overview

The cipher module supports data encryption and decryption by following the data encryption standard (DES), 3DES, or advanced encryption standard (AES) algorithm. The DES, 3DES, and AES algorithms are implemented according to FIPS46-3 and FIPS 197 standards. The DES/3DES and AES operating modes comply with FIPS-81 and NIST special 800-38a standards.

The cipher module can encrypt or decrypt a large amount of data effectively. In addition, it encrypts and decrypts one or more blocks at one time.

3.7.2 Features

The cipher module has the following features:

- Supports the AES key length of 128 bits, 192 bit, or 256 bits. If keys are configured by the key management module, the key length can be set only to 128 bits.
- Supports the DES key length of 64 bits. The values for bit 0, bit 8, bit 16, bit 24, bit 32, bit 40, bit 48, and bit 56 represent the parity check values for eight bytes respectively. The parity check values are not used during encryption or decryption.
- Supports 3-key and 2-key modes for the 3DES algorithm. If keys are configured by the key management module, only the 2-key mode is supported.
- Supports the operating modes of electronic codebook (ECB), cipher block chaining (CBC), 1-/8-/128-cipher feedback (CFB), 128-output feedback (OFB), and counter (CTR) for the AES algorithm. These operating modes comply with the NIST special 800-38a standard.
- Supports the operating modes of ECB, CBC, 1-/8-/64-CFB, and 1-/8-/64-OFB for the DES or 3DES algorithm. These operating modes comply with the FIPS-81 standard.
- Encrypts and decrypts one or more blocks at one time in ECB, CBC, CFB, OFB or CTR operating mode.
- Encrypts and decrypts one or more blocks at one time in CTR operating mode using the AES algorithm.
- Provides eight encryption/decryption keys (64 bits, 128 bits, 192 bits, or 256 bits) configured by the CPU.
- Provides a single-block encryption/decryption channel and seven multi-block encryption/decryption channels. The single-block encryption/decryption channel can encrypt or decrypt a single block only at one time. In this case, the CPU writes data to the channel register and reads the results. For the multi-block encryption/decryption channel, the logic reads data from the DDR, and writes the encrypted or decrypted data to the DDR automatically.
- Supports weighted round robin policy for each channel. For a single-block channel, the weighted value is 1 by default; for a multi-block channel, the weighted value is configurable.
- Supports the same set of keys or different sets of keys for any channel.

- Keeps the data in the last incomplete block unprocessed when the data of the multi-block channels is not an integral multiple of encryption/decryption blocks.
- Supports data combination for multi-block channels. To be specific, if the remaining data in a linked list data block is insufficient to form an encryption/decryption block and the data block is not the last one to be processed, the remaining data is combined with the data in the next data block for encryption or decryption. This avoids data stuffing.
- Supports byte address for the multi-block encryption/decryption channel.
- Supports the multi-linked-list structure for the multi-block encryption/decryption channel and supports the combination of data from multiple linked lists. The linked list length is 20 bits. That is, the maximum data amount is 1 MB minus 1.
- Queries the interrupt status and masks and clears interrupts.
- Separately processes and controls interrupts for each channel.
- Supports multi-packet interrupts and aging interrupts.

3.7.3 Function Description

The operating modes of the DES, 3DES, and AES algorithms comply with the FIPS-81 and NIST special 800-38a standards. In the DES, 3DES, and AES algorithms, the ECB, CBC, and CFB operating modes are identical; however, the CTR (for the AES algorithm only) and OFB operating modes are slightly different.

3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation.

Figure 3-8 shows the 3DES encryption of a 3-key operation and a 2-key operation.

Figure 3-8 3DES encryption of a 3-key operation and a 2-key operation

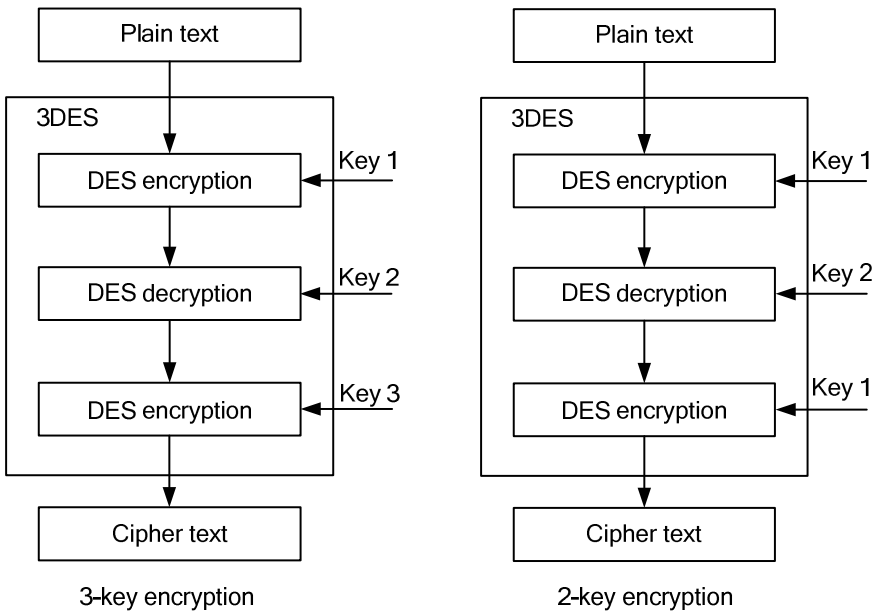
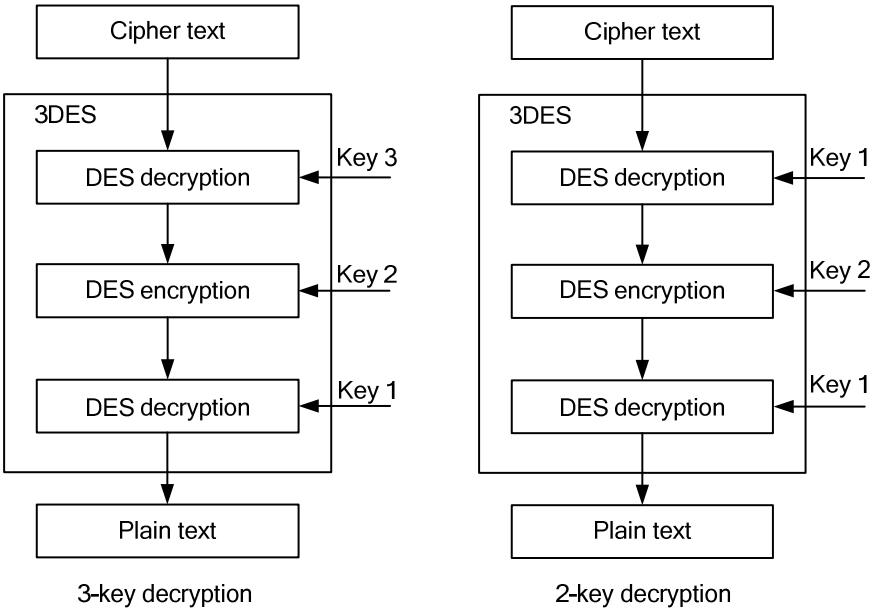


Figure 3-9 shows the 3DES decryption of a 3-key operation and a 2-key operation.

Figure 3-9 3DES decryption of a 3-key operation and a 2-key operation



ECB Mode

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent. With this feature, the plain text encryption and cipher text decryption can be performed concurrently. Figure 3-10 shows the ECB mode of the AES and DES algorithms, and Figure 3-11 shows the ECB mode of the 3DES algorithm.

Figure 3-10 ECB mode of the AES and DES algorithms

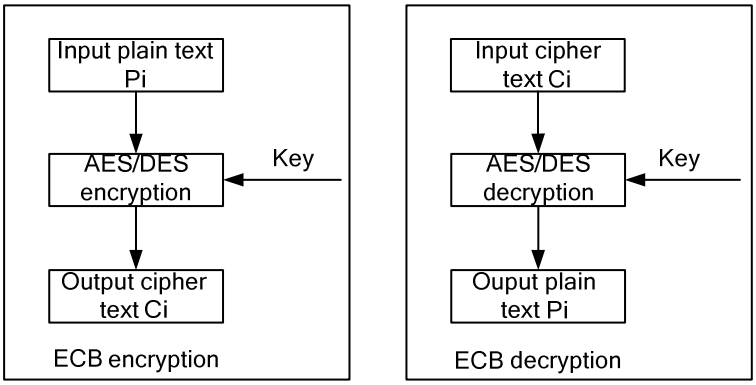
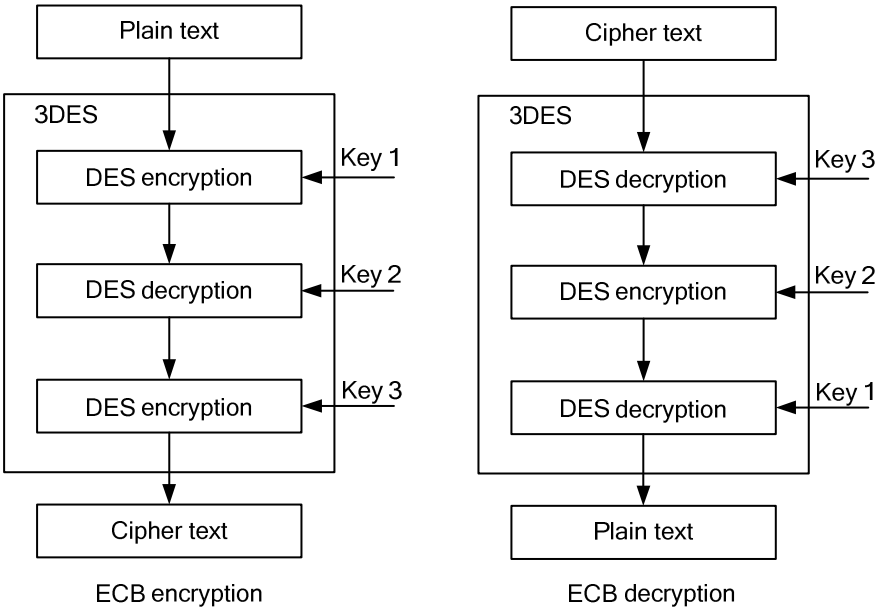


Figure 3-11 ECB mode of the 3DES algorithm



CBC Mode

In CBC mode, the encrypted input plain text block must be exclusively ORed with the input initialization vector (IV) before being encrypted. The encryption processing of each plain text block is related to the block processing result (cipher text) of the previous plain text. Therefore, encryption operations cannot be concurrently performed in CBC mode. The decryption operation, however, is independent of output plain text of the previous block. Therefore, decryption operations can be performed concurrently. Figure 3-12 shows the CBC mode of the AES and DES algorithms, and Figure 3-13 shows the CBC mode of the 3DES algorithm.

Figure 3-12 CBC mode of the AES and DES algorithms

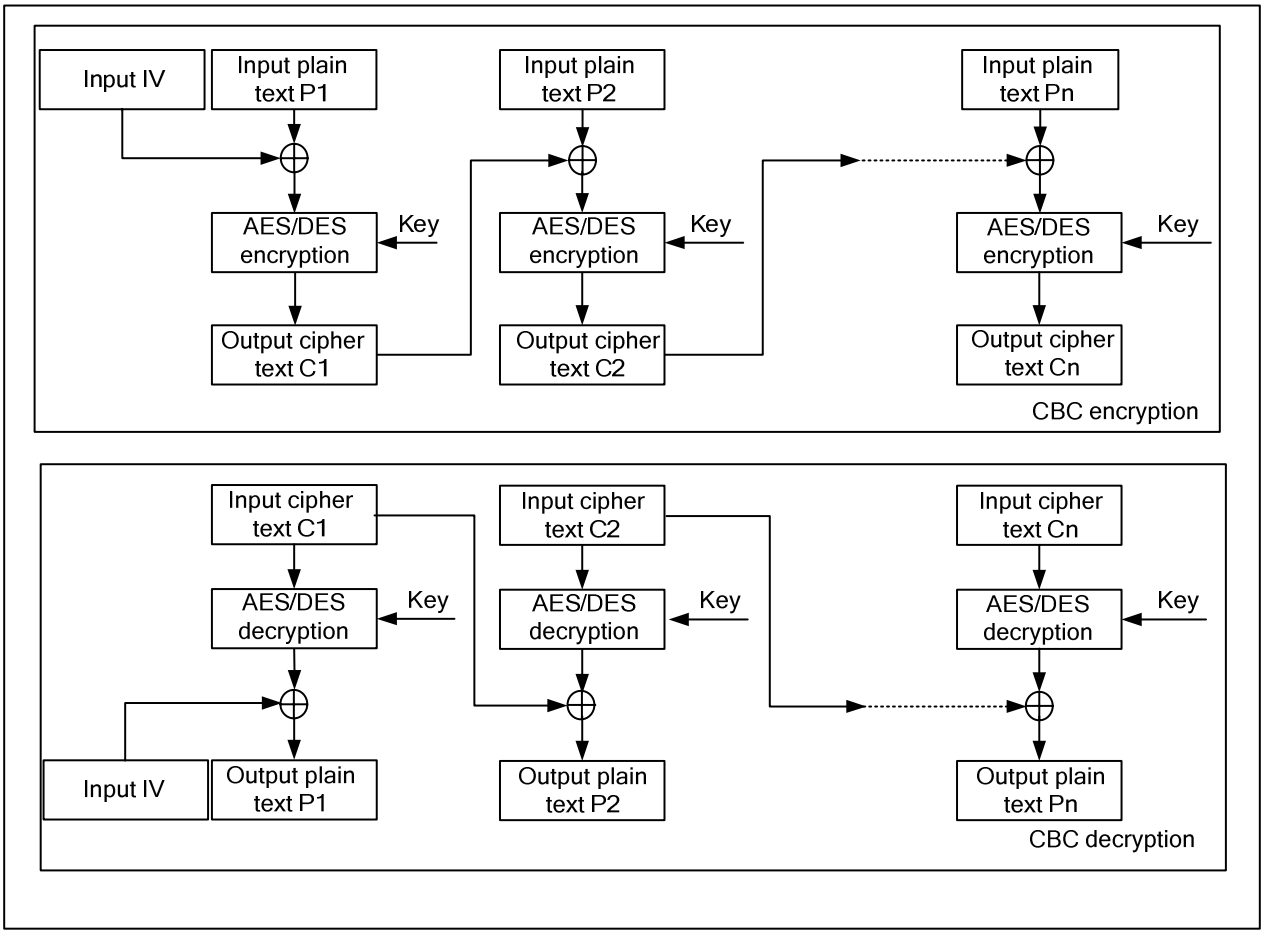
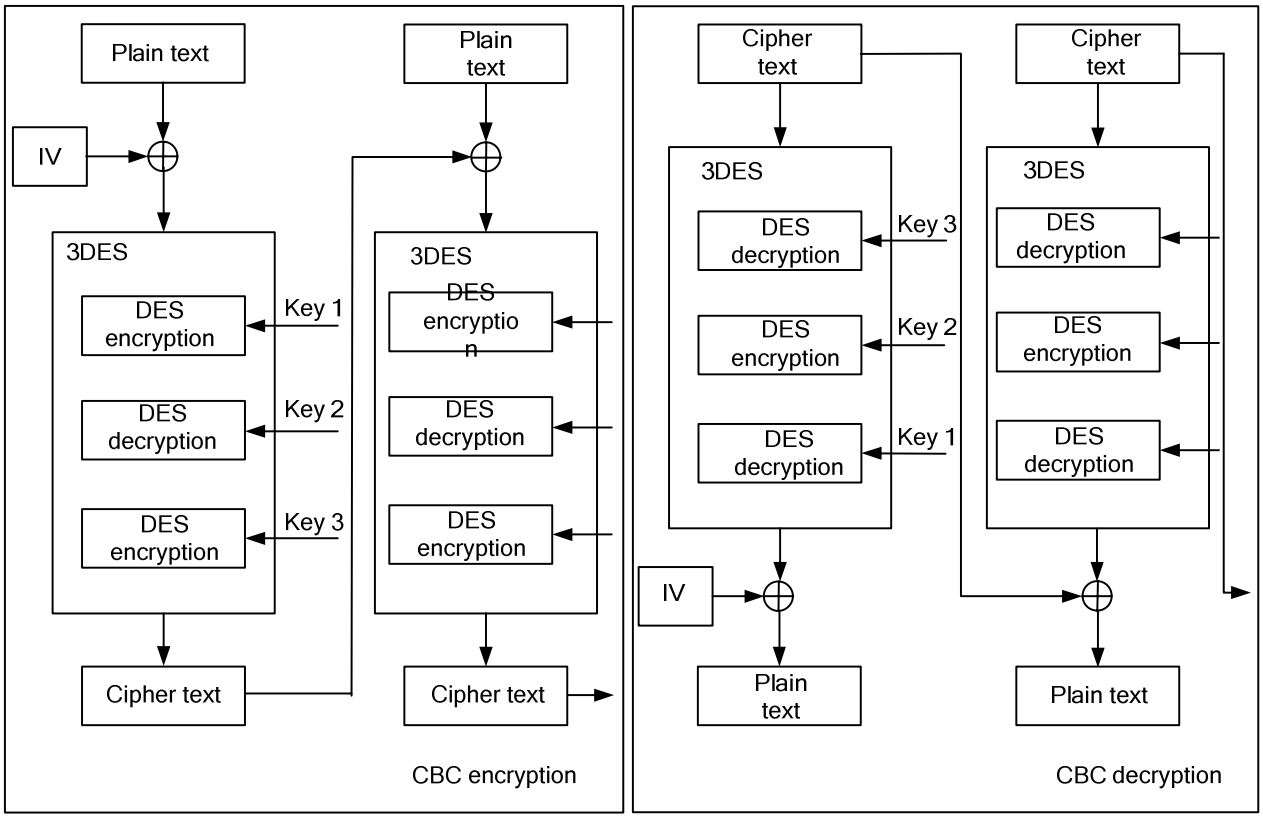


Figure 3-13 CBC mode of the 3DES algorithm



CFB Mode

The CFB mode is used to convert a block cipher into a stream cipher. This mode is implemented by selecting the operation bits of the CFB. The shift operation bits are represented by the letter s. The value of s is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 1 bit, 8 bits, or 128 bits for the AES algorithm

Figure 3-14 shows the s-bit CFB mode of the AES and DES algorithms, and Figure 3-15 shows the s-bit CFB mode of the 3DES algorithm.

Figure 3-14 S-bit CFB mode of the AES and DES algorithms

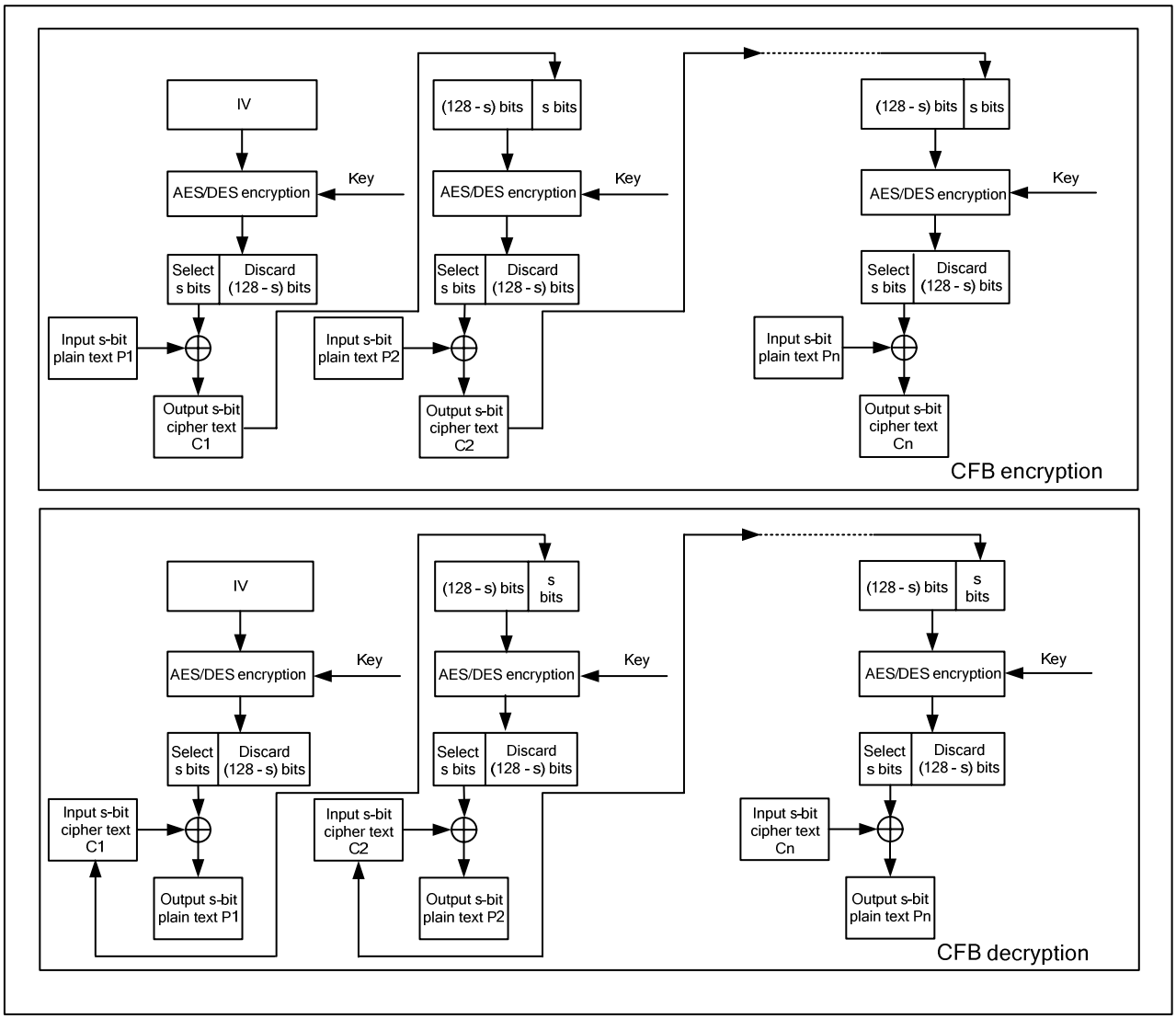
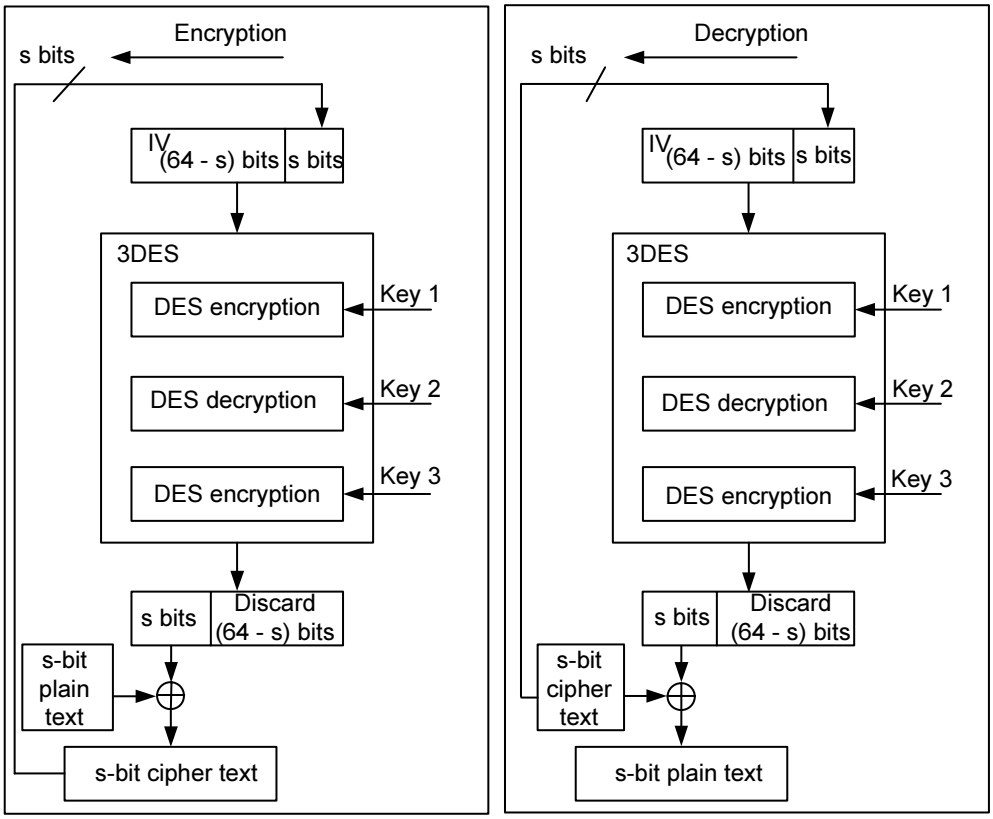


Figure 3-15 S-bit CFB mode of the 3DES algorithm



OFB Mode

In OFB mode, IVs serve as the inputs during encryption. If a same key is used, different IVs must be used to ensure operation security. The value of the s bit is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 128 bits for the AES algorithm

Figure 3-16 shows the OFB mode of the AES algorithm.

Figure 3-16 OFB mode of the AES algorithm

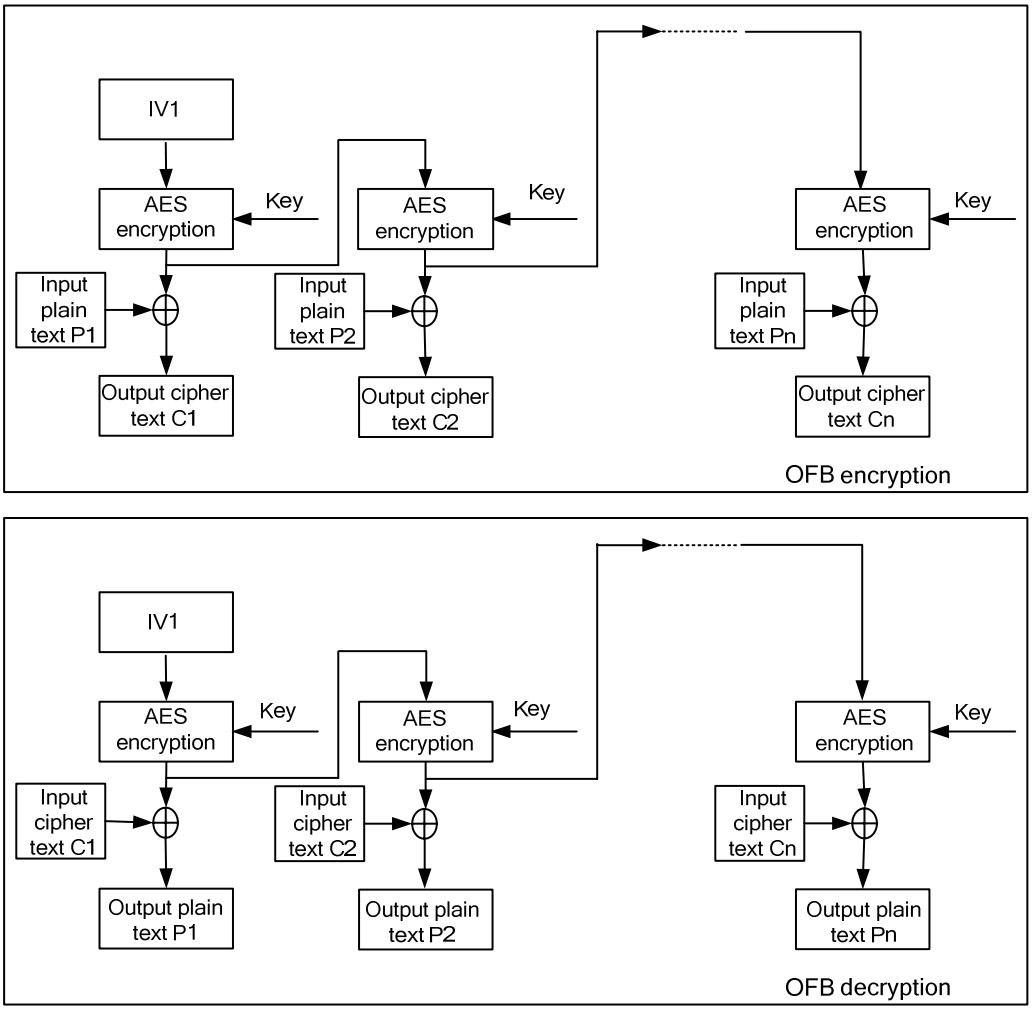


Figure 3-17 shows the s-bit OFB mode of the DES algorithm.

Figure 3-17 S-bit OFB mode of the DES algorithm

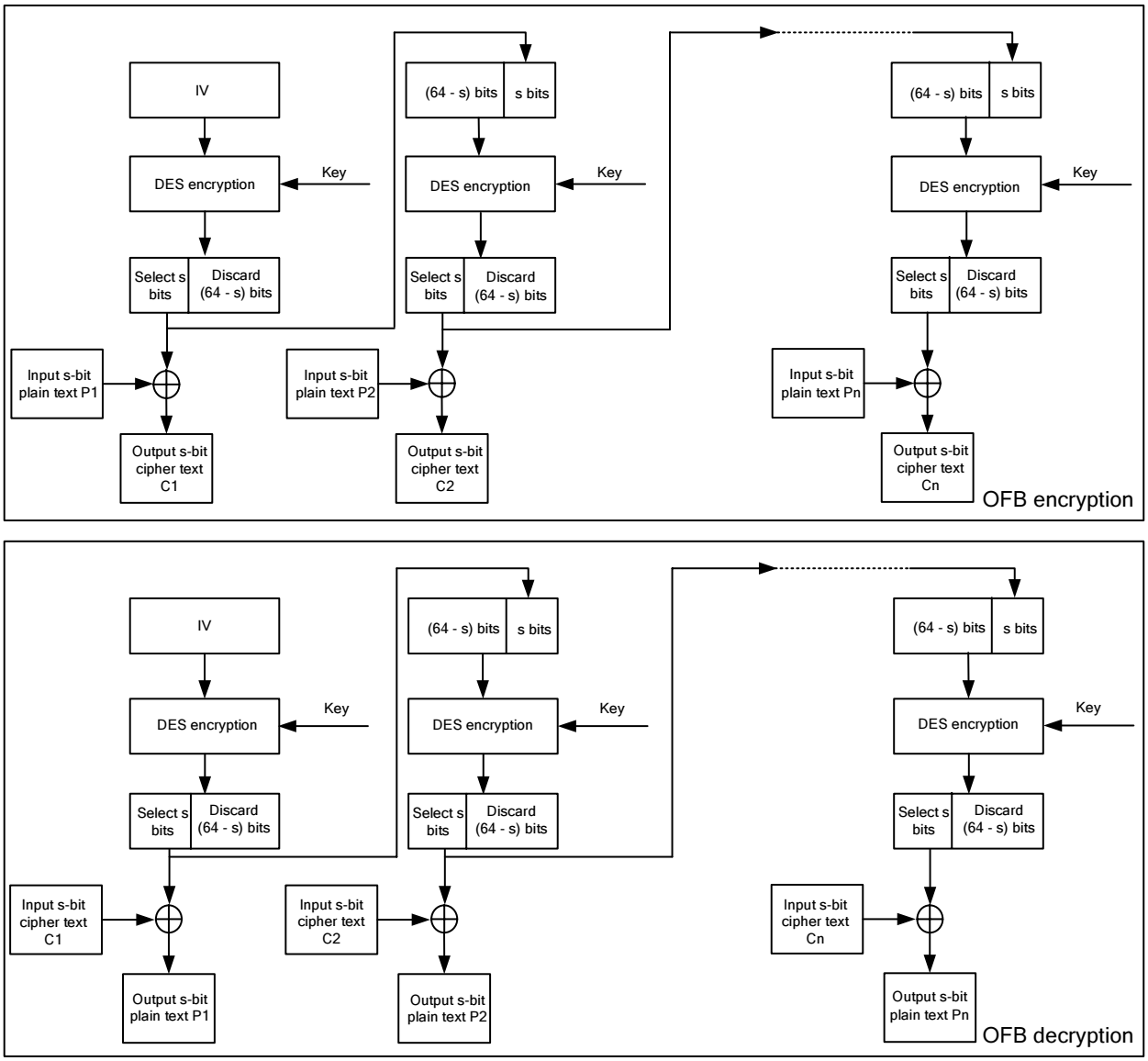
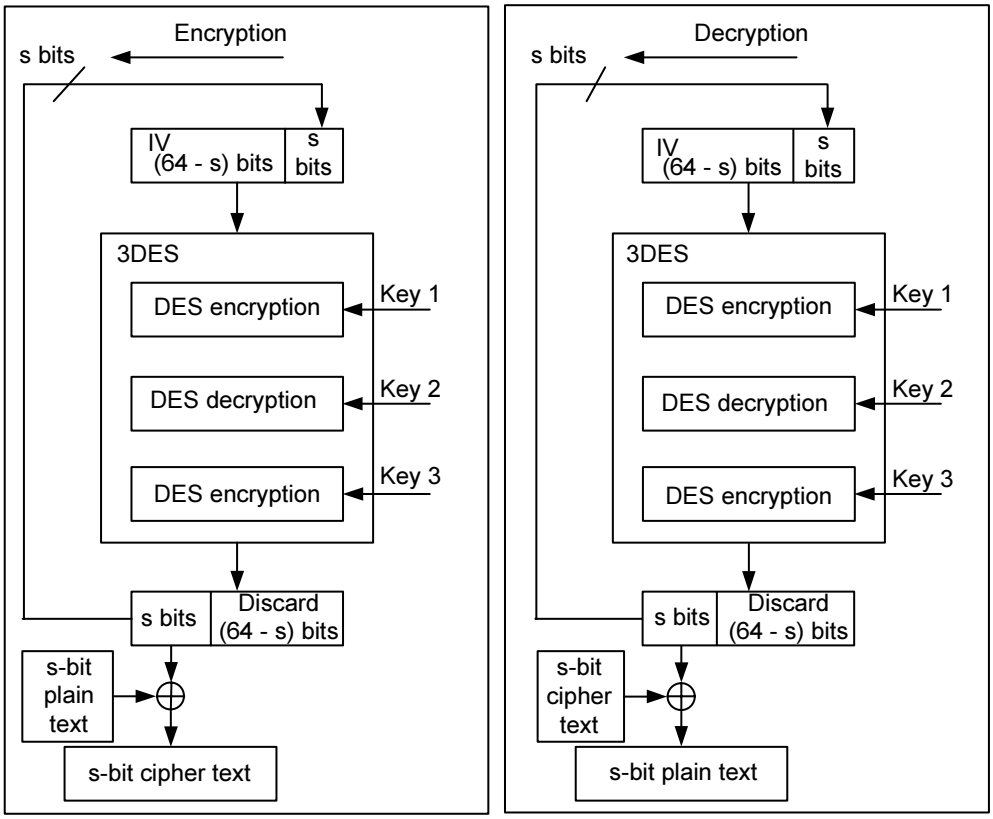


Figure 3-18 shows the s-bit OFB mode of the 3DES algorithm.

Figure 3-18 S-bit OFB mode of the 3DES algorithm



CTR Mode

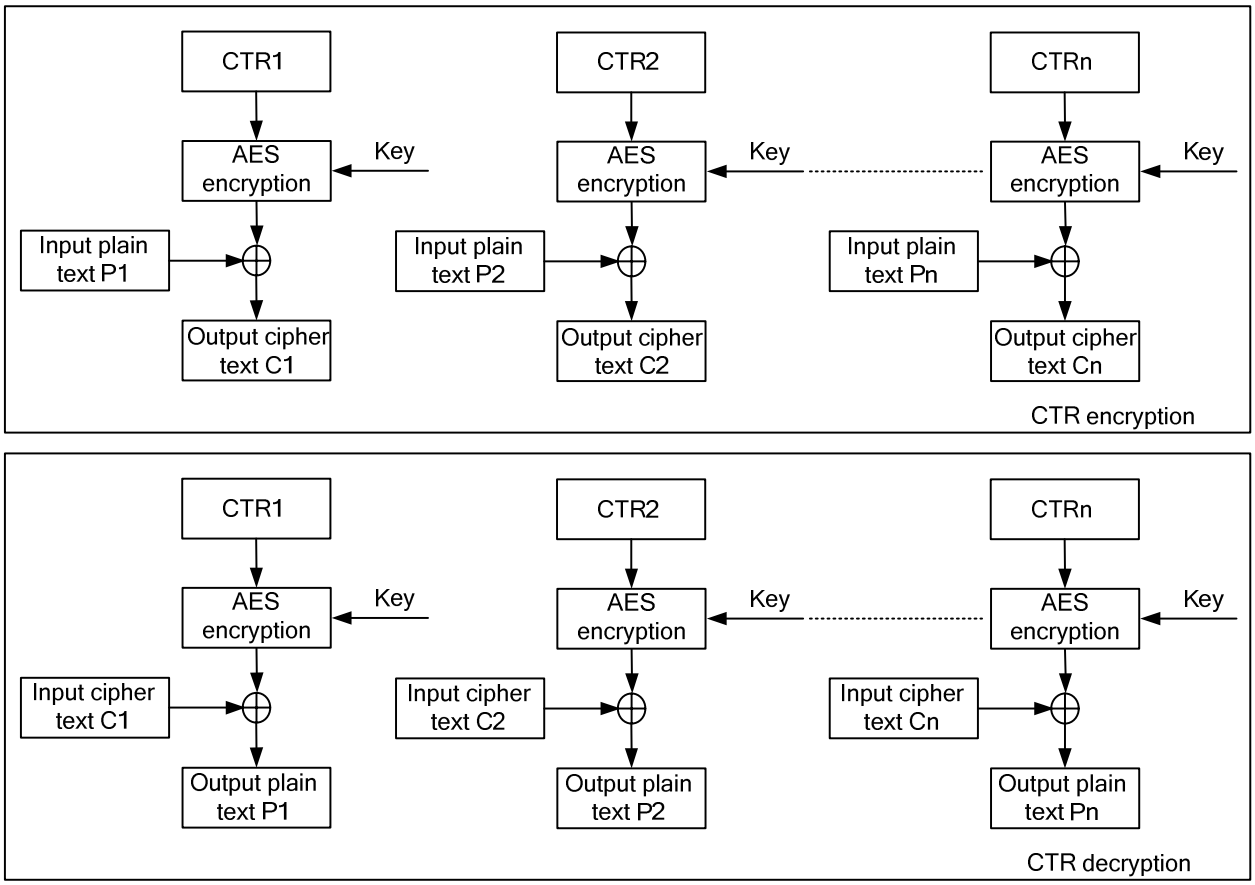
In CTR mode, different data segments are input to the cipher module by using the AES algorithm to ensure data security. Such data can be the count value CTRn. Therefore, CTRn determines the security of the CTR mode.

NOTE

CTR*n* is obtained by using the accumulation count mode.

Figure 3-19 shows the CTR mode of the AES algorithm.

Figure 3-19 CTR mode of the AES algorithm



3.7.4 Operating Mode

Single-Block Operation Process of the Cipher Module

The cipher module provides channel 0 as the single-block encryption/decryption channel. A single-block operation is performed as follows:

Step 1 Check whether channel 0 is busy by querying the ch0_busy field of the configuration register CHAN0_CFG of channel 0. If channel 0 is not busy, configure data inputs and write related configuration information to the registers of channel 0.

Step 2 Write to the ch0_start field of CHAN0_CFG to enable channel 0 to start encryption or decryption.

Step 3 Check whether encryption and decryption of channel 0 are complete in either of following ways:

- Query the ch0_busy field. If ch0_busy indicates that channel 0 is not busy, encryption and decryption are complete.
- Check whether the interrupt of channel 0 is generated. If the interrupt is generated, encryption and decryption are complete.

Step 4 Read the registers CHAN0_CIPHER_DOUT and CHAN0_CIPHER_IVOUT of channel 0.

----End

Multi-Block Operation Process of the Cipher Module

The cipher module provides seven multi-block encryption/decryption channels. The weighted value of each channel can be set using software based on its rate. These channels automatically read data from the DDR, and write the encrypted or decrypted data to the DDR.

A multi-block operation is performed as follows:

Step 1 Initialize the channels, including setting the depth, start address, number of multi-packet interrupts, aging interrupt time of the input and output queues of each channel, and setting the control register of each channel.

Step 2 When data needs to be encrypted or decrypted, query CHANn_IBUF_CNT. If the value of this register is smaller than the value of CHANn_IBUF_NUM, add the header of the data linked list corresponding to the data to be encrypted or decrypted to the input queue, and go to Step 4; otherwise, go to Step 3.

Step 3 Enable the interrupt corresponding to the input queue channel, wait for the generation of the interrupt, read CHANn_IEMPTY_CNT, write to this register to clear the interrupt, and add new data to the input queue.

Step 4 Add the linked list header of the output buffer to the output queue.

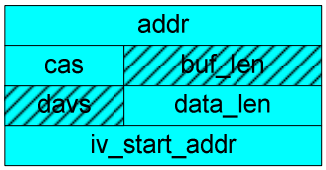
Step 5 Enable the interrupt corresponding to the output queue.

Step 6 Fetch data from the output queue, and write the number of currently received packets to CHANn_OFULL_CNT to clear the interrupt.

----End

Figure 3-20 shows the structure of the linked list header of a multi-block encryption/decryption channel.

Figure 3-20 Structure of the linked list header of a multi-block encryption/decryption channel

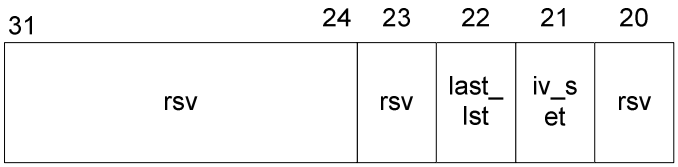


The field definitions are as follows:

- addr is the start address of the buffer pointer by the linked list header. The start address can be byte address.
- data_len is the length of the valid data pointed by the linked list header.
- cas is cipher control information.

  Figure 3-21 shows the bits of cas.

Figure 3-21 Bits of cas



- iv_set indicates that the IV of the data pointed by the current linked list header must be replaced. iv_start_addr indicates the start address of the IV in the DDR. This address must be aligned by word.
- last_lst indicates that the data pointed by the current linked list header is the last linked list of a data block. If the logic encounters an incomplete encryption/decryption block after processing the linked list, the logic writes the incomplete block to the output buffer without performing encryption and decryption.

Clock Gating

When no encryption is required and the cipher module is idle, the cipher clock can be disabled by configuring the registers of the system controller, which reduces power consumption.

Soft Reset

The cipher module can be soft-reset by configuring the registers of the system controller.

3.7.5 Register Summary

Table 3-15 describes cipher registers.

NOTE

The variable *n* in the offset addresses indicates the channel ID and ranges from 1 to 7.

Table 3-15 Summary of cipher registers (base address: 0x1007_0000)

Offset Address	Register	Description	Page
0x0000–0x000C	CHAN0_CIPHER_DOUT	Cipher output register for channel 0 (for single-block encryption/decryption)	3-145
0x0010–0x001C	CHAN0_CIPHER_IVOUT	Operation complete IV output register of the cipher module	3-145
0x0020–0x008C	CHAN_CIPHER_IVOUT	IV output register for channels 1–7	3-146
0x0090–0x018C	CIPHER_KEY	CPU configuration key register of the cipher module	3-147
0x1000	CHAN0_CIPHER_CTRL	Encryption/decryption control register for channel 0	3-148

Offset Address	Register	Description	Page
0x1004–0x1010	CHAN0_CIPHER_IV IN	Cipher VI block input register for channel 0	3-150
0x1014–0x1020	CHAN0_CIPHER_DI N	128-bit block input register of the cipher module	3-151
0x1000 + *n* x 0x128	CHANn_IBUF_NUM	Input queue total depth register for channel n (n = 1–7) (linked list header count register)	3-152
0x1000 + *n* x 0 x128 + 0x4	CHANn_IBUF_CNT	Pending data buffer count register for channel n in the input queue	3-152
0x1000 + *n* x 0x128 + 0x8	CHANn_IEMPTY_C NT	Processed data buffer count register for channel n in the input queue	3-153
0x1000 + *n* x 0x128 + 0xC	CHANn_INT_ICNTC FG	Input queue multi-packet interrupt threshold register for channel n	3-153
0x1000 + *n* x 0x128 + 0x10	CHANn_CIPHER_C TRL	Encryption/decryption control register for channel n	3-154
0x1000 + *n* x 0x128 + 0x14	CHANn_SRC_LST_S ADDR	Input queue start address register for channel n	3-156
0x1000 + *n* x 0x128 + 0x18	CHANn_IAGE_TIM ER	Input queue interrupt aging time configuration register for channel n	3-156
0x1000 + *n* x 0x128 + 0x3C	CHANn_OBUF_NU M	Output queue total depth register for channel n (linked list header count register)	3-157
0x1000 + *n* x 0x128 + 0x40	CHANn_OBUF_CNT	Pending data buffer count register for channel n in the output queue	3-157
0x1000 + *n* x 0x128 + 0x44	CHANn_OFULL_CN T	Processed data buffer count register for channel n in the output queue	3-158
0x1000 + *n* x 0x128 + 0x48	CHANn_INT_OCNT CFG	Output queue multi-packet interrupt threshold register for channel n	3-158
0x1000 + *n* x 0x128 + 0x4C	CHANn_DEST_LST_ SADDR	Output queue start address register for channel n	3-158
0x1000 + *n* x 0x128 + 0x50	CHANn_OAGE_TIM ER	Output queue interrupt aging time configuration register for channel n	3-159
0x1400	INT_STATUS	Interrupt status register	3-159
0x1404	INT_EN	Interrupt enable register	3-160
0x1408	INT_RAW	Raw interrupt status register	3-161
0x140C	RST_STATUS	Reset status indicator register	3-162
0x1410	CHAN0_CFG	Channel 0 configuration register	3-162

3.7.5.2 Register Description

CHAN0_CIPHER_DOUT

CHAN0_CIPHER_DOUT is a cipher output register for channel 0 (for single-block encryption/decryption).

The data read from this register is the results of a single-block operation. The results of the AES algorithm are different from those of the DES or 3DES algorithm. The details are as follows:

- For the AES algorithm
  - If the 1-CFB mode is selected, the least significant bit (LSB) is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- For the DES or 3DES algorithm
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0000–0x000C	CHAN0_CIPHER_DOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_dout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_dout	128-bit block output of the cipher module. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0000 CIPHER_DOUT[63:32]: address 0x0004 CIPHER_DOUT[95:64]: address 0x0008 CIPHER_DOUT[127:96]: address 0x000C

CHAN0_CIPHER_IVOUT

CHAN0_CIPHER_IVOUT is an operation complete IV output register of the cipher module.

Note the following points when reading this register:

- This register can be ignored in ECB or CTR mode.
- If a single-block operation is performed, the data of this register is the vector output of the block. The data can be used as the vector input in the next block operation for the same data packet.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected (CIPHER_CTRL[cipher_mode] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.
- If a multi-block operation is performed, the data read from this register is the output vector of the last block operation.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0010–0x001C	CHAN0_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_ivout	Vector output after the operation of the cipher module is complete. It can be ignored in ECB or CTR mode. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0010 CIPHER_IVOUT[63:32]: address 0x0014 CIPHER_IVOUT[95:64]: address 0x0018 CIPHER_IVOUT[127:96]: address 0x001C

CHAN_CIPHER_IVOUT

CHAN_CIPHER_IVOUT is an IV output register for channels 1–7.

Offset Address	Register Name	Total Reset Value
0x0020–0x008C	CHAN_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan_cipher_ivout																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan_cipher_ivout	0x0020–0x002C: channel 1 0x0030–0x003C: channel 2 0x0040–0x004C: channel 3 0x0050–0x005C: channel 4 0x0060–0x006C: channel 5 0x0070–0x007C: channel 6 0x0080–0x008C: channel 7

CIPHER_KEY

CIPHER_KEY is a CPU configuration key register of the cipher module. The key is the configured value of the CPU, and the CPU can be read or written.

Note the following points when configuring this register:

- If the DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_KEY[63:0] is valid.
- For the 3DES algorithm

  If a 3-key operation is performed (CIPHER_CTRL[key_length] = 0b00, 0b01, or 0b10), low 192 bits are valid.

  where

  - CIPHER_KEY bit[63:0] indicates key 1.
  - CIPHER_KEY bit[127:64] indicates key 2.
  - CIPHER_KEY bit[191:128] indicates key 3.

  If a 2-key operation is selected (CIPHER_CTRL[key_length] = 0b11), lower 128 bits are valid.

  where

  - CIPHER_KEY bit[63:0] indicates key 1.
  - CIPHER_KEY bit[127:64] indicates key 2.
- For the AES algorithm
  - If a 128-bit key operation is performed, lower 128 bits are valid, that is, CIPHER_KEY bit[127:0] is valid.
  - If a 192-bit key operation is performed, lower 192 bits are valid, that is, CIPHER_KEY bit[191:0] is valid.
  - If a 256-bit key operation is performed, 256 bits are valid.

The cipher module allows you to configure eight keys. Each channel can use one key, and multiple channels can share one key.

Offset Address	Register Name	Total Reset Value
0x0090–0x018C	CIPHER_KEY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cipher_key																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	cipher_key	Key input of the cipher module. Each address maps to a 32-bit data segment. CIPHER_KEY[31:0]: address 0x0090 CIPHER_KEY[63:32]: address 0x0094 CIPHER_KEY[95:64]: address 0x0098 CIPHER_KEY[127:96]: address 0x009C CIPHER_KEY[159: 128]: address 0x00A0 CIPHER_KEY[191:160]: address 0x00A4 CIPHER_KEY[223:192]: address 0x00A8 CIPHER_KEY[255:224]: address 0x00AC 0x0090–0x00AC: host_key0 0x00B0–0x00CC: host_key1 0x00D0–0x00EC: host_key2 0x00F0–0x010C: host_key3 0x0110–0x012C: host_key4 0x0130–0x014C: host_key5 0x0150–0x016C: host_key6 0x0170–0x018C: host_key7

CHAN0_CIPHER_CTRL

CHAN0_CIPHER_CTRL is an encryption/decryption control register for channel 0. Channel 0 is a single-block encryption/decryption channel.

Note the following points when configuring this register:

- Configure this register before configuring others registers of the cipher module.
- In the modes except the CFB mode of the AES algorithm, the CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes except the CFB and OFB modes of the DES and 3DES algorithms, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder			key_sel	reserved			key_length			ivin_sel	width			alg_sel	mode			decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16:14]	RW	key_adder	ID of the key used by the current channel 000: host_key0 001: host_key1 010: host_key2 011: host_key3 100: host_key4 101: host_key5 110: host_key6 111: host_key7
[13]	RW	key_sel	Key select 0: keys configured by the CPU 1: reserved
[12]	RO	reserved	Reserved
[11]	RO	reserved	Reserved
[10:9]	RW	key_length	Key length select For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RW	ivin_sel	Input select of CIPHER_IVIN 0: do not configure CIPHER_IVIN 1: configure CIPHER_IVIN

[7:6]	RW	width	Bit width control For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm
[3:1]	RW	mode	Operating mode select For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select 0: encryption 1: decryption

CHAN0_CIPHER_IVIN

CHAN0_CIPHER_IVIN is a cipher VI block input register for channel 0.

Assume that channel 0 is selected for the single-block encryption/decryption and the selected mode is not ECB mode (CIPHER_CTRL[mode] = 0b001, 0b010, 0b011, or 0b100).

- If you do not want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b0), CIPHER_IVIN can be ignored.
- If you want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b1), CIPHER_IVIN needs to be configured. If the AES algorithm is selected (CIPHER_CTRL [alg_sel] = 0b10), CIPHER_IVIN bit[127:0] is valid. If the DES or 3DES algorithm is selected (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1004–0x1010	CHAN0_CIPHER_IVIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivin																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_ivin	128-bit IV of the cipher module for channel 0 or the data input from the counter. Each address maps to a 32-bit data segment. CIPHER_IVIN[31:0]: address 0x1004 CIPHER_IVIN[63:32]: address 0x1008 CIPHER_IVIN[95:64]: address 0x100C CIPHER_IVIN[127:96]: address 0x1010

CHAN0_CIPHER_DIN

CHAN0_CIPHER_DIN is a 128-bit block input register of the cipher module.

Note the following points when configuring this register:

If channel 0 is selected for the single-block operation, this register needs to be configured.

- Assume that the AES algorithm (CIPHER_CTRL[alg_sel] = 0b10) is selected.
  - If the 1-CFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- Assume that the DES or the 3DES algorithm (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11) is selected.
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1014–0x1020	CHAN0_CIPHER_DIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_din																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_din	128-bit block input of the cipher module for channel 0. Each address maps to a 32-bit data segment. CIPHER_DIN[31:0]: address 0x1014 CIPHER_DIN[63:32]: address 0x1018 CIPHER_DIN[95:64]: address 0x101c CIPHER_DIN[127:96]: address 0x1020

CHANn_IBUF_NUM

CHANn_IBUF_NUM is an input queue total depth register for channel *n* (*n* = 1–7). This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128	CHANn_IBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ibuf_num	Input queue depth, that is, count of linked list headers configured for each channel.

CHANn_IBUF_CNT

CHANn_IBUF_CNT is a pending data buffer count register for channel *n* in the input queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x128 + 0x4	CHANn_IBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ibuf_cnt	Count of buffers to be processed in the input queue

CHANn_IEMPTY_CNT

CHANn_IEMPTY_CNT is a processed buffer count register for channel *n* in the input queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x8	CHANn_IEMPTY_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iempty_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	iempty_cnt	Count of processed buffers in the input queue

CHANn_INT_ICNTCFG

CHANn_INT_ICNTCFG is an input queue multi-packet interrupt threshold register for channel *n*. When the count of buffers in the input queue processed by the logic is above the threshold, an input queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0xC	CHANn_INT_ICNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_icnt_cfg															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	int_icnt_cfg	Input queue multi-packet interrupt threshold

CHANn_CIPHER_CTRL

CHANn_CIPHER_CTRL is an encryption/decryption control register for channel *n*.

Note the following points when configuring this register:

- You must configure this register before performing encryption or decryption using the channel.
- In the modes other than the CFB mode of the AES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes other than the CFB and OFB modes of the DES or 3DES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x10	CHANn_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	weight										reserved						key_adder				key_sel	byte_seq	ts_vld	key_length			reserved		width		alg_sel		mode		decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	weight	Weighted value of the current channel, in the unit of 64 bytes
[21:17]	RO	reserved	Reserved
[16:14]	RW	key_adder	ID of the key used by the current channel. The key can be any one in the addresses 0–7.
[13]	RW	key_sel	Key select 0: keys configured by the CPU 1: reserved
[12:11]	RO	reserved	Reserved

[10:9]	RW	key_length	Key length select For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RO	reserved	Reserved
[7:6]	RW	width	Bit width control For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm

[3:1]	RW	mode	Operating mode select For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select 0: encryption 1: decryption

CHANn_SRC_LST_SADDR

CHANn_SRC_LST_SADDR is an input queue start address register for channel n. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x14	CHANn_SRC_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_lst_saddr	Start address for the input queue

CHANn_IAGE_TIMER

CHANn_IAGE_TIMER is an input queue interrupt aging time configuration register for channel *n*. If overflow occurs in the aging time counter and the count of processed buffers in the input queue is greater than 0, an input queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x18	CHANn_IAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	iage_timer	Aging interrupt timer

CHANn_OBUF_NUM

CHANn_OBUF_NUM is an output queue total depth register for channel *n*. This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x3C	CHANn_OBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	obuf_num	Total depth of the output queue

CHANn_OBUF_CNT

CHANn_OBUF_CNT is a pending data buffer count register for channel *n* in the output queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x40	CHANn_OBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	obuf_cnt	Count of buffers to be processed in the output queue

CHANn_OFULL_CNT

CHANn_OFULL_CNT is a processed buffer count register for channel *n* in the output queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x44	CHANn_OFULL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ofull_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ofull_cnt	Count of processed buffers in the output queue

CHANn_INT_OCNTCFG

CHANn_INT_OCNTCFG is an output queue multi-packet interrupt threshold register for channel *n*. When the count of buffers in the output queue processed by the logic is above the threshold, an output queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x48	CHANn_INT_OCNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ocnt_cfg															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	int_ocnt_cfg	Output queue multi-packet interrupt threshold

CHANn_DEST_LST_SADDR

CHANn_DEST_LST_SADDR is an output queue start address register for channel *n*. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x4C	CHANn_DEST_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_lst_saddr	Start address for the output queue

CHANn_OAGE_TIMER

CHANn_OAGE_TIMER is an output queue interrupt aging time configuration register for channel *n*. If overflow occurs in the aging time counter and the count of processed buffers in the output queue is greater than 0, an output queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 128 + 0x50	CHANn_OAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																oage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	oage_timer	Aging interrupt timer

INT_STATUS

INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_int	ch6_ibuf_int	ch5_ibuf_int	ch4_ibuf_int	ch3_ibuf_int	ch2_ibuf_int	ch1_ibuf_int	ch0_ibuf_int	ch7_obuf_int	ch6_obuf_int	ch5_obuf_int	ch4_obuf_int	ch3_obuf_int	ch2_obuf_int	ch1_obuf_int	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15]	RO	ch7_ibuf_int	Input queue data interrupt for channel 7
[14]	RO	ch6_ibuf_int	Input queue data interrupt for channel 6
[13]	RO	ch5_ibuf_int	Input queue data interrupt for channel 5
[12]	RO	ch4_ibuf_int	Input queue data interrupt for channel 4
[11]	RO	ch3_ibuf_int	Input queue data interrupt for channel 3
[10]	RO	ch2_ibuf_int	Input queue data interrupt for channel 2
[9]	RO	ch1_ibuf_int	Input queue data interrupt for channel 1
[8]	RO	ch0_ibuf_int	Data processing complete interrupt for channel 0
[7]	RO	ch7_obuf_int	Output queue data interrupt for channel 7
[6]	RO	ch6_obuf_int	Output queue data interrupt for channel 6
[5]	RO	ch5_obuf_int	Output queue data interrupt for channel 5
[4]	RO	ch4_obuf_int	Output queue data interrupt for channel 4
[3]	RO	ch3_obuf_int	Output queue data interrupt for channel 3
[2]	RO	ch2_obuf_int	Output queue data interrupt for channel 2
[1]	RO	ch1_obuf_int	Output queue data interrupt for channel 1
[0]	RO	reserved	Reserved

INT_EN

INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x1404	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_en	reserved															ch7_ibuf_en	ch6_ibuf_en	ch5_ibuf_en	ch4_ibuf_en	ch3_ibuf_en	ch2_ibuf_en	ch1_ibuf_en	ch0_ibuf_en	ch7_obuf_en	ch6_obuf_en	ch5_obuf_en	ch4_obuf_en	ch3_obuf_en	ch2_obuf_en	ch1_obuf_en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_en	Total interrupt enable for the cipher module
[30:16]	RO	reserved	Reserved
[15]	RW	ch7_ibuf_en	Input queue data interrupt enable for channel 7
[14]	RW	ch6_ibuf_en	Input queue data interrupt enable for channel 6

[13]	RW	ch5_ibuf_en	Input queue data interrupt enable for channel 5
[12]	RW	ch4_ibuf_en	Input queue data interrupt enable for channel 4
[11]	RW	ch3_ibuf_en	Input queue data interrupt enable for channel 3
[10]	RW	ch2_ibuf_en	Input queue data interrupt enable for channel 2
[9]	RW	ch1_ibuf_en	Input queue data interrupt enable for channel 1
[8]	RW	ch0_ibuf_en	Data processing complete interrupt enable for channel 0
[7]	RW	ch7_obuf_en	Output queue data interrupt enable for channel 7
[6]	RW	ch6_obuf_en	Output queue data interrupt enable for channel 6
[5]	RW	ch5_obuf_en	Output queue data interrupt enable for channel 5
[4]	RW	ch4_obuf_en	Output queue data interrupt enable for channel 4
[3]	RW	ch3_obuf_en	Output queue data interrupt enable for channel 3
[2]	RW	ch2_obuf_en	Output queue data interrupt enable for channel 2
[1]	RW	ch1_obuf_en	Output queue data interrupt enable for channel 1
[0]	RO	reserved	Reserved

INT_RAW

INT_RAW is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_raw	ch6_ibuf_raw	ch5_ibuf_raw	ch4_ibuf_raw	ch3_ibuf_raw	ch2_ibuf_raw	ch1_ibuf_raw	ch0_ibuf_raw	ch7_obuf_raw	ch6_obuf_raw	ch5_obuf_raw	ch4_obuf_raw	ch3_obuf_raw	ch2_obuf_raw	ch1_obuf_raw	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RWC	ch7_ibuf_raw	Raw input queue data interrupt for channel 7
[14]	RWC	ch6_ibuf_raw	Raw input queue data interrupt for channel 6
[13]	RWC	ch5_ibuf_raw	Raw input queue data interrupt for channel 5
[12]	RWC	ch4_ibuf_raw	Raw input queue data interrupt for channel 4
[11]	RWC	ch3_ibuf_raw	Raw input queue data interrupt for channel 3

[10]	RWC	ch2_ibuf_raw	Raw input queue data interrupt for channel 2
[9]	RWC	ch1_ibuf_raw	Raw input queue data interrupt for channel 1
[8]	RWC	ch0_ibuf_raw	Raw data processing complete interrupt for channel 0
[7]	RWC	ch7_obuf_raw	Raw output queue data interrupt for channel 7
[6]	RWC	ch6_obuf_raw	Raw output queue data interrupt for channel 6
[5]	RWC	ch5_obuf_raw	Raw output queue data interrupt for channel 5
[4]	RWC	ch4_obuf_raw	Raw output queue data interrupt for channel 4
[3]	RWC	ch3_obuf_raw	Raw output queue data interrupt for channel 3
[2]	RWC	ch2_obuf_raw	Raw output queue data interrupt for channel 2
[1]	RWC	ch1_obuf_raw	Raw output queue data interrupt for channel 1
[0]	RO	reserved	Reserved

RST_STATUS

RST_STATUS is a reset status indicator register.

Offset Address	Register Name	Total Reset Value
0x140C	RST_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								rst_status
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	rst_status	Reset status indicator of the cipher module 0: The cipher module is being reset. 1: The cipher module is working properly.

CHAN0_CFG

CHAN0_CFG is channel 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	CHAN0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ch0_busy	ch0_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	ch0_busy	Status signal of channel 0
[0]	RW	ch0_start	Encryption/Decryption start signal of channel 0

3.8 Timer

3.8.1 Overview

The timer module implements the timing and counting functions. It not only serves as the system clock of the operating system, but also can be used by applications for timing and counting. The Hi3521A has eight timers.

3.8.2 Features

Timer has the following features:

- Provides 16-bit or 32-bit down counter that has a programmable 8-bit prescaler.
- Provides a configurable count clock, that is, the clock can serve as the bus clock or 3 MHz crystal oscillator clock.
- Supports three count modes: free-running mode, periodic mode, and one-shot mode.
- Loads the initial value through either of the following registers: TIMERx_LOAD and TIMERx_BGLOAD.
- Reads the current count value at any time.
- Generates an interrupt when the count value is decreased to 0.

3.8.3 Function Description

The timer is a 32-bit or 16-bit configurable down counter. The counter value is decremented by 1 on each rising edge of the count clock. When the count value reaches 0, the timer generates an interrupt.

The timer supports three count modes:

- Free-running mode

The timer counts continuously. When the count value reaches 0, the timer wraps its value around to the maximum value automatically and then continues to count. When the count length is 32 bits, the maximum value is 0xFFFF_FFFF. When the count length is 16 bits, the maximum value is 0xFFFF. In free-running mode, the count value is decremented immediately from the loaded value. When the value reaches 0, the value is wrapped around to the maximum value.

- Periodic mode

  The timer counts continuously. When the count value reaches 0, the timer loads an initial value from TIMERx_BGLOAD again and then continues to count.

- One-shot mode

  The initial value is loaded to the timer. When the count value of the timer reaches 0, the timer stops counting. The timer starts to count again only when a new value is loaded and the timer is enabled.

Each timer has a prescaler that divides the frequency of the working clock of each timer by 1, 16, or 256. In this way, flexible frequencies of the count clock are provided. An initial value is loaded to the timer as follows:

- An initial value can be loaded by writing TIMERx_LOAD. When the timer works, if a value is written to TIMERx_LOAD, the timer recounts starting from this value immediately. This method is applicable to all count modes.
- The count cycle in periodic mode can be set by writing TIMERx_BGLOAD. The current count value of the timer is not affected immediately when TIMERx_BGLOAD is written. Instead, the timer continues to count until the count value reaches 0. Then the timer loads the new value of TIMERx_BGLOAD and starts to count.

3.8.4 Operating Mode

Initialization

The timer must be initialized when the system is initialized. To initialize timer*X* (*X* ranges from 0 to 7), do as follows:

Step 1 Write to TIMERx_LOAD to load an initial value to the timer.

Step 2 When the timer is required to work in periodic mode and the count cycle is different from the initial value loaded to the timer, write to TIMERx_BGLOAD to set the count cycle of the timer.

Step 3 Configure the SC_CTRL register of the system controller to set the reference clock of the clock enable signal of the timer.

Step 4 Write to TIMERx_CONTROL to set the count mode, counter length, prescaling factor, and interrupt mask of the timer, and then enable the timer to count.

----End

Interrupt Processing

The timer is used to generate interrupts periodically. Therefore, interrupt processing is a process of activating and waiting the timing interrupt. To process an interrupt, do as follows:

Step 1 Configure TIMERx_INTCLR to clear the interrupt of the timer.

Step 2 Activate the processes of waiting for the interrupt and execute the process.

Step 3 When all the processes of waiting for the interrupt are complete or the wait interrupt is in hibernate state, resume the interrupt and continue to execute the interrupted program.

----End

Clock Selection

Each timer has two optional count clocks. The following sections describe how to select a clock by taking timer0 as an example.

To select the bus clock as the count clock, do as follows:

Step 1 Set SC_CTRL [timeren0ov] to 1.

Step 2 Initialize the timer and start to count.

----End

To select the 3 MHz crystal oscillator clock as the count clock, do as follows:

Step 1 Set SC_CTRL [timeren0sel] to 0.

Step 2 Set SC_CTRL [timeren0sel] to 0.

Step 3 Initialize the timer and start to count.

----End

3.8.5 Register Summary

The timer module consists of eight timers and each timer involves a group of registers. The eight groups of registers have the same features except that their base addresses are different. The details about their base addresses are as follows:

- The base address of timer 0: 0x1200_0000.
- The base address of timer 1: 0x1200_0020.
- The base address of timer 2: 0x1201_0000.
- The base address of timer 3: 0x1201_0020.
- The base address of timer 4: 0x1202_0000.
- The base address of timer 5: 0x1202_0020.
- The base address of timer 6: 0x1203_0000.
- The base address of timer 7: 0x1203_0020.

NOTE

The value of *X* in timer*X* ranges from 0 to 7. The registers for timer 0 to timer 7 are the same. In this section, timer 0 registers are described as an example.

Table 3-16 Summary of timer registers

Offset Address	Register	Description	Page
0x000	TIMERx_LOAD	Initial count value register	3-166

Offset Address	Register	Description	Page
0x004	TIMERx_VALUE	Current count value register	3-167
0x008	TIMERx_CONTROL	Control register	3-167
0x00C	TIMERx_INTCLR	Interrupt clear register	3-168
0x010	TIMERx_RIS	Raw interrupt status register	3-169
0x014	TIMERx_MIS	Masked interrupt status register	3-169
0x018	TIMERx_BGLOAD	Initial count value register in periodic mode	3-170

3.8.6 Register Description

TIMERx_LOAD

TIMERx_LOAD is an initial count value register. It is used to set the initial count value of each timer. Each timer (timers 0–7) has one such register.

NOTE

- The minimum valid value written to TIMERx_LOAD is 1.
- When the value 0 is written to TIMERx_LOAD, the dual-timer module generates an interrupt immediately.

If values are written to TIMERx_BGLOAD and TIMERx_LOAD before the rising edge of TIMCLK enabled by TIMCLKENx reaches, the count value of the next rising edge of TIMCLK is changed to the value written to TIMERx_LOAD. As the value of TIMERx_BGLOAD changes when data is written to TIMERx_LOAD, the value returned after TIMERx_BGLOAD is read is the latest value that is written to TIMERx_LOAD and TIMERx_BGLOAD. When the timer works in periodic mode and the count value decreases to 0, the initial value is loaded from TIMERx_BGLOAD to continue counting.

Offset Address	Register Name	Total Reset Value
0x000	TIMER0_LOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_load																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0_load	Initial count value of timer 0

TIMERx_VALUE

TIMERx_VALUE is a current count value register. It shows the current value of the counter that is decremented. Each timer (timers 0–7) has one such register.

After a value is written to TIMERx_LOAD, TIMERx_VALUE immediately shows the newly loaded value of the counter in the PCLK domain without waiting for the clock edge of TIMCLK enabled by TIMCLKENx.

NOTE

When a timer is in 16-bit mode, the 16 upper bits of the 32-bit TIMERx_VALUE are not set to 0 automatically. If the timer is switched from 32-bit mode to 16-bit mode and no data is written to TIMERx_LOAD, the upper 16 bits of TIMERx_VALUE may be non-zero.

Offset Address	Register Name	Total Reset Value
0x004	TIMER0_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_value																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	timer0_value	Current count value of timer 0 that is decremented

TIMERx_CONTROL

TIMERx_CONTROL is a control register. Each timer (timers 0–7) has one such register.

NOTE

When the periodic mode is selected, TIMERx_CONTROL[timermode] must be set to 1 and TIMERx_CONTROL[oneshot] must be set to 0.

Offset Address	Register Name	Total Reset Value
0x008	TIMER0_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timeren	timermode	intenable	reserved	timerpre		timersize	oneshot
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	timeren	Timer enable 0: disabled 1: enabled

[6]	RW	timermode	Timer count mode 0: free-running mode 1: periodic mode
[5]	RW	intenable	Raw interrupt mask 0: masked 1: not masked
[4]	RO	reserved	Reserved
[3:2]	RW	timerpre	Prescaling factor configuration 00: no prescaling. That is, the clock frequency of the timer is divided by 1 01: 4-level prescaling. That is, the clock frequency of the timer is divided by 16 10: 8-level prescaling. That is, the clock frequency of the timer is divided by 256 11: undefined. If the bits are set to 11, 8-level prescaling is considered. That is, the clock frequency of the timer is divided by 256.
[1]	RW	timersize	Counter select 0: 16-bit counter 1: 32-bit counter
[0]	RW	oneshot	Count mode select 0: periodic mode or free-running mode 1: one-shot mode

TIMERx_INTCLR

TIMERx_INTCLR is the interrupt clear register. The interrupt status of a counter is cleared after any operation is performed on this register. Each timer (timers 0–7) has one such register.

CAUTION

This register is a write-only register. The timer clears interrupts when any value is written to this register. In addition, no value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x00C	TIMER0_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	timer0_intclr
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Access	Name	Description
[31:0]	WO	timer0_intclr	Writing this register clears the output interrupt of timer 0

TIMERx_RIS

TIMERx_RIS is a raw interrupt status register. Each timer (timers 0–7) has one such register.

Offset Address	Register Name	Total Reset Value
0x010	TIMER0_RIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								timer0ris
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved. Writing this register has no effect and reading this register returns 0.
[0]	RO	timer0ris	Raw interrupt status of timer0 0: No interrupt is generated. 1: An interrupt is generated.

TIMERx_MIS

TIMERx_MIS is a masked interrupt status register. Each timer (timers 0–7) has one such register.

Offset Address	Register Name	Total Reset Value
0x014	TIMER0_MIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								timer0mis

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	timer0mis	Masked interrupt status of timer 0 0: The interrupt is invalid. 1: The interrupt is valid.

TIMERx_BGLOAD

TIMERx_BGLOAD is an initial count value register in periodic mode. Each timer (timers 0–7) has one such register.

The TIMERx_BGLOAD register contains the initial count value of the timer. This register is used to reload an initial count value when the count value of the timer reaches 0 in periodic mode.

In addition, this register provides another method of accessing TIMERx_LOAD. The difference is that after a value is written to TIMERx_BGLOAD, the timer does not count starting from the input value immediately.

Offset Address	Register Name	Total Reset Value
0x018	TIMER0_BGLOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0bgload																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0bgload	Initial count value of timer 0 Note: This register differs from TIMERx_LOAD. For details, see the descriptions of TIMERx_LOAD.

3.9 Watchdog

3.9.1 Overview

The watchdog is used to transmit a reset signal to reset the entire system within a period after an exception occurs in the system.

3.9.2 Features

The watchdog has the following features:

- Provides a 32-bit internal down counter. The count clock source is configurable.
- Supports the configurable timeout interval, namely, initial count value.

- Locks registers to avoid any modification to them.
- Supports the generation of timeout interrupts.
- Supports the generation of reset signals.
- Supports the debugging mode.

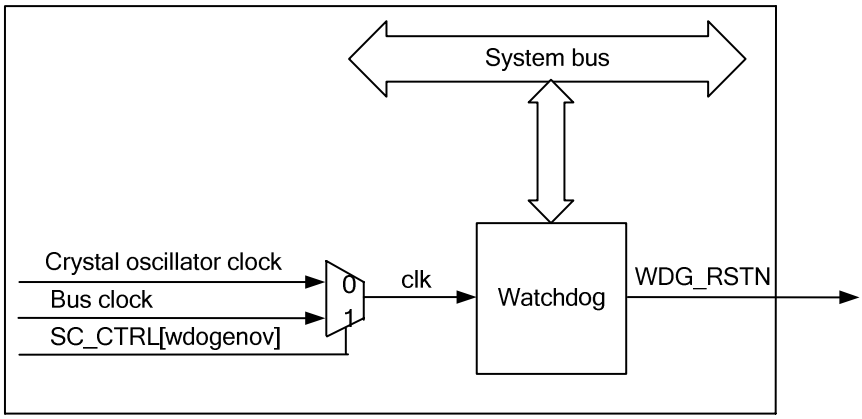
3.9.3 Function Description

Application Block Diagram

The system selects clocks for the watchdog by configuring the system control register SC_CTRL[wdogenov] and configures the parameter values of watchdog registers by using the system bus. The watchdog transmits interrupt requests to the system periodically. When the system does not respond to the interrupt requests (such as the suspend case), the watchdog transmits the WDG_RSTN reset signal to reset the system. In this way, the system running status is monitored.

Figure 3-22 shows the application block diagram of the watchdog.

Figure 3-22 Application block diagram of the watchdog



Function Principle

The watchdog works based on a 32-bit down counter. The initial value is loaded by WDG_LOAD. When the watchdog clock is enabled, the count value is decremented by 1 on the rising edge of each count clock. When the count value reaches 0, the watchdog generates an interrupt. On the next rising edge of the count clock, the counter reloads the initial value from WDG_LOAD and continues to count in decremental mode.

If the count value of the counter reaches 0 for the second time but the CPU does not clear the watchdog interrupt, the watchdog transmits the reset signal WDG_RSTN and the counter stops counting.

You can enable or disable the watchdog by configuring WDG_CONTROL as required. That is, you can control the watchdog whether to generate interrupts and reset signals.

- When the interrupt generation function is disabled, the watchdog counter stops counting.

- When the interrupt generation function is enabled again, the watchdog counter counts starting from the preset value of WDG_LOAD instead of the last count value. Before an interrupt is generated, the initial value can be reloaded.

The count clock of the watchdog can be a crystal oscillator clock or a bus clock so different count time ranges are available.

By configuring WDG_LOCK, you can disable the operation of writing to the internal registers of the watchdog.

- Writing 0x1ACC_E551 to WDG_LOCK to enable the write permission for all the registers of the watchdog.
- Writing any other values to WDG_LOCK to disable the write permission for all the registers of the watchdog except WDG_LOCK.

This feature avoids modifications to the watchdog registers by software. Therefore, the watchdog operation is not terminated by mistake by software when an exception occurs.

In debugging mode, the watchdog is disabled automatically to avoid the intervention to the normal debugging.

3.9.4 Operating Mode

Configuring the Frequency of the Count Clock

The system supports two types of watchdog count clocks: 3 MHz crystal oscillator clock and bus clock. The two clocks are selected by configuring the system control register SC_CTRL[wdogenov].

The count time T_{WDG} of the watchdog is calculated as follows:

$$T_{WDG} = Value_{WDG\_LOAD} \times \left(\frac{1}{f_{clk}} \right)$$

NOTE

The definition of each parameter in the preceding formula is as follows:

- T_{WDG} indicates the count time of the watchdog.
- $Value_{WDG\_LOAD}$ indicates the initial count value of the watchdog.
- f_{clk} indicates the frequency of the watchdog count clock.

The ranges of the count time of the watchdog under different clocks are as follows:

- When a 3 MHz crystal oscillator clock is selected, the count time ranges from 0s to 1400s.
- When a bus clock (such as a 100 MHz clock) is selected, the count time ranges from 0s to 42s.

Initializing the System

The watchdog counter stops counting after the system POR. Before the system is initialized, the watchdog must be initialized and enabled. To initialize the watchdog, perform the following steps:

Step 1 Write to WDG_LOAD to set the initial count value.

Step 2 Write to WDG_CONTROL to enable the interrupt mask function and start the watchdog counter.

Step 3 Write to WDG_LOCK to lock the watchdog to avoid the watchdog settings being modified by the software by mistake.

----End

Processing an Interrupt

After an interrupt is received from the watchdog, the interrupt must be cleared in time and the initial count value must be reloaded to the watchdog to restart counting. A watchdog interrupt is processed as follows:

Step 1 Write 0x1ACC_E551 to WDG_LOCK to unlock the watchdog.

Step 2 Write to WDG_INTCLR to clear the watchdog interrupt and load the initial count value to the watchdog to restart counting.

Step 3 Write any other values rather than 0x1ACC_E551 to WDG_LOCK to lock the watchdog.

----End

Disabling the Watchdog

You can control the status of the watchdog by writing 0 or 1 to WDG_CONTROL[inten].

- 0: disabled
- 1: enabled

3.9.5 Register Summary

Table 3-17 describes watchdog registers.

Table 3-17 Summary of watchdog registers (base address: 0x1207_0000)

Offset Address	Register	Description	Page
0x0000	WDG_LOAD	Initial count value register	3-174
0x0004	WDG_VALUE	Current count value register	3-174
0x0008	WDG_CONTROL	Control register	3-174
0x000C	WDG_INTCLR	Interrupt clear register	3-175
0x0010	WDG_RIS	Raw interrupt register	3-175
0x0014	WDG_MIS	Masked interrupt status register	3-176
0x0C00	WDG_LOCK	Lock register	3-176

3.9.6 Register Description

WDG_LOAD

WDG_LOAD is an initial count value register. It is used to configure the initial count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_load																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	wdg_load	Initial count value of the watchdog counter

WDG_VALUE

WDG_VALUE is a current count value register. It is used to read the current count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdogvalue																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	Current count value of the watchdog counter

WDG_CONTROL

WDG_CONTROL is a control register. It is used to enable or disable the watchdog and control the interrupt and reset functions of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														resen	inten

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	resen	Output enable of the watchdog reset signal 0: disabled 1: enabled
[0]	RW	inten	Output enable of the watchdog interrupt signal 0: The counter stops counting, the current count value remains unchanged, and the watchdog is disabled. 1: The counter, interrupt, and watchdog are enabled.

WDG_INTCLR

WDG_INTCLR is an interrupt clear register. It is used to clear watchdog interrupts so the watchdog can reload an initial value for counting. This register is write-only. When a value is written to this register, the watchdog interrupts are cleared. No written value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_intclr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	wdg_intclr	Writing any value to this register clears the watchdog interrupts and enables the watchdog to reload an initial count value from WDG_LOAD to restart counting.

WDG_RIS

WDG_RIS is a raw interrupt status register. It shows the raw interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdgris

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wdogris	Status of the raw interrupts of the watchdog. When the count value reaches 0, this bit is set to 1. 0: No interrupt is generated. 1: An interrupt is generated.

WDG_MIS

WDG_MIS is a masked interrupt status register. It shows the masked interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogmis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wdogmis	Status of the masked interrupts of the watchdog 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

WDG_LOCK

WDG_LOCK is a lock register. It is used to control the write and read permissions for the watchdog registers.

Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdg_lock	Writing 0x1ACC_E551 to this register enables the write

			permission for all the registers. Writing other values disables the write permission for all the registers. When this register is read, the lock status rather than the written value of this register is returned. 0x0000_0000: The write permission is available (unlocked). 0x0000_0001: The write permission is unavailable (locked).

3.10 RTC

3.10.1 Overview

The RTC is used to display the time in real time and periodically generate alarms.

3.10.2 Features

The RTC has the following features:

- Provides a 40-bit counter. Of the 40 bits, 16 bits are for counting days, five bits are for counting hours, six bits are for counting minutes, six bits are for counting seconds, and the other seven bits are for counting 10 ms.
- Provides a 100 Hz count clock.
- Allows you to configure the initial count value.
- Allows you to configure the match value.
- Supports the timeout interrupt.
- Supports soft reset.
- Supports the fixed frequency-division mode.
- Provides the junction temperature of the position where the RTC is located.
- Stores user data in a 64-bit user register.

3.10.3 Function Description

The RTC has a 40-bit up counter for counting days, hours, minutes, seconds, and 10 ms. The initial values are loaded from RTC_LR_10MS, RTC_LR_S, RTC_LR_M, RTC_LR_H, RTC_LR_D_L, and RTC_LR_D_H. This section assumes that the counter is divided into the day counter, hour counter, minute counter, second counter, and 10 ms counter. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt. Then, the counter continues to count in incremental mode on the rising edge of the next count clock.

By configuring RTC_IMSC, you can allow or forbid the RTC to generate interrupts. Note the following two cases:

- When the function of generating interrupts is disabled, the RTC counter continues to count in incremental mode and no interrupts are generated. RTC_MSC_INT shows the status of masked interrupts and RTC_RAW_INT shows the status of raw interrupts.

- When the function of generating interrupts is enabled, the RTC counter still counts in incremental mode. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt.

The RTC uses a 100 Hz count clock and a 16-bit day counter. The value of the day counter can be used to reckon the specific year, month, and day.

3.10.4 Operating Mode

3.10.4.1 Count Clock Frequency

The RTC uses a 100 Hz count clock. The maximum RTC count time (T_{RTC}) is calculated as follows:

$T_{RTC} = 2^{16} = 65536$ days

3.10.4.2 Soft Reset

The RTC can be separately soft-reset by configuring RTC_POR_N. After soft reset, the value of each RTC configuration register is restored to its default value. Therefore, these registers must be initialized again.

To soft-reset the RTC, perform the following steps:

Step 1 Write 0 to RTC_POR_N.

Step 2 Wait 30 ms.

----End

3.10.4.3 Initializing the RTC

The system needs to initialize the RTC when the RTC is powered on for the first time. The initialization process is as follows:

Step 1 Configure RTC_POR_N to reset the RTC.

Step 2 Wait 30 ms.

Step 3 Configure RTC_IMSC to set the interrupt mask bit of the RTC.

Step 4 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the RTC match value.

Step 5 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the initial count value of the RTC.

Step 6 Set RTC_LORD to 1 to load the initial count value to the RTC counter.

Step 7 Based on the 100 Hz count clock, the RTC counts starting from the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC determines whether to generate an interrupt based on the settings of RTC_IMSC.

----End

3.10.4.4 Handling Interrupts

If the system receives an interrupt from the RTC, the configured time is reached. Then user-defined operations can be performed. The RTC counter, however, still counts in incremental mode. To clear an RTC interrupt, set RTC_INT_CLR to 1. To continue to configure time, write a new match value to RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H.

3.10.4.5 Accessing RTC Registers

Internal RTC registers are located in the RTC module, not on the bus. The RTC registers on the bus are used only for accessing internal RTC registers.

To write to internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This example assumes that the clock is 120 MHz and the expected SPI clock is 12 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (120/12)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to write 0x10 to RTC_MR_10MS, write 0x01060010 to SPI_RW. That is, spi_start is 1, spi_rw is 0, spi_add is 0x06, and spi_wdata is 0x10.

----End

To read internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This step assumes that the clock is 120 MHz and the expected SPI clock is 12 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (120/12)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to read SPI_RW, write 0x01860000 to SPI_RW. That is, spi_start is 1, spi_rw is 0, and spi_add is 0x06.

Step 4 Read SPI_RW bit[31] until it is 0. SPI_RW [15:8] is the value that is returned after RTC_MR_10MS is read.

----End

3.10.5 Register Summary

Table 3-18 describes RTC registers.

Table 3-18 Summary of RTC registers (base address: 0x120B_0000)

Offset Address	Register	Description	Page
0x0000	SPI_CLK_DIV	SPI clock divider register	3-181
0x0004	SPI_RW	SPI read/write register	3-182

Table 3-19 describes the internal RTC registers.

Table 3-19 Summary of internal RTC registers (base address: 0x00)

Offset Address	Register	Description	Page
0x00	RTC_10MS_COUNT	Count value register for the RTC 10 ms counter	3-183
0x01	RTC_S_COUNT	Count value register for the RTC second counter	3-183
0x02	RTC_M_COUNT	Count value register for the RTC minute counter	3-184
0x03	RTC_H_COUNT	Count value register for the RTC hour counter	3-184
0x04	RTC_D_COUNT_L	Lower-8-bit count value register for the RTC day counter	3-185
0x05	RTC_D_COUNT_H	Upper-8-bit count value register for the RTC day counter	3-185
0x06	RTC_MR_10MS	Match value register for the RTC 10 ms counter	3-185
0x07	RTC_MR_S	Match value register for the RTC second counter	3-186
0x08	RTC_MR_M	Match value register for the RTC minute counter	3-186
0x09	RTC_MR_H	Match value register for the RTC hour counter	3-187
0x0A	RTC_MR_D_L	Lower-8-bit match value register for the RTC day counter	3-187
0x0B	RTC_MR_D_H	Upper-8-bit match value register for the RTC day counter	3-188
0x0C	RTC_LR_10MS	Configured value register for the RTC 10 ms counter	3-188
0x0D	RTC_LR_S	Configured value register for the RTC second counter	3-189

Offset Address	Register	Description	Page
0x0E	RTC_LR_M	Configured value register for the RTC minute counter	3-189
0x0F	RTC_LR_H	Configured value register for the RTC hour counter	3-189
0x10	RTC_LR_D_L	Lower-8-bit configured value register for the RTC day counter	3-190
0x11	RTC_LR_D_H	Upper-8-bit configured value register for the RTC day counter	3-190
0x12	RTC_LORD	RTC configured value loading enable register	3-191
0x13	RTC_IMSC	RTC interrupt enable register	3-192
0x14	RTC_INT_CLR	RTC interrupt clear register	3-192
0x15	RTC_MSC_INT	RTC mask interrupt status register.	3-193
0x16	RTC_RAW_INT	RTC raw interrupt status register	3-193
0x17	RTC_CLK	RTC output clock select register	3-193
0x18	RTC_POR_N	RTC reset control register	3-194
0x51	SDM_COEF_OUSIDE_H	Upper-4-bit clock divider register in fixed frequency-division mode	3-194
0x52	SDM_COEF_OUSIDE_L	Lower-8-bit register clock divider register in fixed frequency-division mode	3-195
0x53	USER_REGISTER1	64-bit user register 1	3-195
0x54	USER_REGISTER2	64-bit user register 2	3-195
0x55	USER_REGISTER3	64-bit user register 3	3-196
0x56	USER_REGISTER4	64-bit user register 4	3-196
0x57	USER_REGISTER5	64-bit user register 5	3-196
0x58	USER_REGISTER6	64-bit user register 6	3-197
0x59	USER_REGISTER7	64-bit user register 7	3-197
0x5A	USER_REGISTER8	64-bit user register 8	3-197

3.10.6 RTC Register Description

SPI_CLK_DIV

SPI_CLK_DIV is an SPI clock divider register.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_CLK_DIV	0x0000_003B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi_clk_div							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	spi_clk_div	SPI clock divider. The SPI clock frequency cannot be higher than 20 MHz. The value 12 MHz is recommended. The field value ranges from 1 to 255. The value of spi_clk_div is used to define the SPI RX and RX bit rates. The formula is as follows: FSPICLK = FAPBCLK/[2 x (spi_clk_div + 1)]. FAPBCLK is the clock frequency. If the clock is 120 MHz and the expected SPI clock is 12 MHz, the configured value of spi_clk_div is calculated as follows: (120/12)/2 – 1 = 4

SPI_RW

SPI_RW is an SPI read/write register.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_busy	reserved						spi_start	spi_rw	spi_add							spi_rdata								spi_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	spi_busy	SPI read/write status indicator 0: The SPI is idle, and a new read/write operation can be initiated over the SPI. 1: A read/write operation is being performed over the SPI, and no new operation is allowed.
[30:25]	RO	reserved	Reserved
[24]	W1_PULSE	spi_start	SPI read/write start. Writing 1 automatically clears this field. Writing has no effect when spi_busy is 1. That is, no new SPI operation is started before the previous read/write operation is complete. If a start request is sent, hardware ignores this request.

[23]	RW	spi_rw	SPI operation type 0: write 1: read
[22:16]	RW	spi_add	SPI operation address The address range is 0–127.
[15:8]	RO	spi_rdata	Data read from the SPI
[7:0]	RW	spi_wdata	Data to be written to the SPI

3.10.7 Internal Register Description

RTC_10MS_COUNT

RTC_10MS_COUNT is a count value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x00	RTC_10MS_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_10ms_count						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RO	rtc_10ms_count	RTC 10 ms counter value. It indicates the currently counted time. Its unit is 10 ms. The value range is 0–99.

RTC_S_COUNT

RTC_S_COUNT is a count value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x01	RTC_S_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_s_count					

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RO	rtc_s_count	RTC second counter value. It indicates the currently counted seconds. The value range is 0–59.

RTC_M_COUNT

RTC_M_COUNT is a count value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x02	RTC_M_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_m_count					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RO	rtc_m_count	RTC minute counter value. It indicates the currently counted minutes. The value range is 0–59.

RTC_H_COUNT

RTC_H_COUNT is a count value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x03	RTC_H_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_h_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved

[4:0]	RO	rtc_h_count	RTC hour counter value. It indicates the currently counted hours. The value range is 0–23.

RTC_D_COUNT_L

RTC_D_COUNT_L is a lower-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x04	RTC_D_COUNT_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_l	Lower eight bits of the RTC day counter value. This field works with RTC_D_COUNT_H to indicate the currently counted days. The day range is 0–65535.

RTC_D_COUNT_H

RTC_D_COUNT_H is an upper-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x05	RTC_D_COUNT_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_h	Upper eight bits of the RTC day counter value. This field works with RTC_D_COUNT_L to indicate the currently counted day. The day range is 0–65535.

RTC_MR_10MS

RTC_MR_10MS is a match value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x06	RTC_MR_10MS	0x7F

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_mr_10ms						
Reset	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RW	rtc_mr_10ms	Match value of the RTC 10 ms counter The value range is 0–99.

RTC_MR_S

RTC_MR_S is a match value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x07	RTC_MR_S	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_s					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_mr_s	Match value of the RTC second counter The value range is 0–59.

RTC_MR_M

RTC_MR_M is a match value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x08	RTC_MR_M	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_m					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_mr_m	Match value of the RTC minute counter The value range is 0–59.

RTC_MR_H

RTC_MR_H is a match value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x09	RTC_MR_H	0x1F

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_mr_h				
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved
[4:0]	RW	rtc_mr_h	Match value of the RTC hour counter The value range is 0–23.

RTC_MR_D_L

RTC_MR_D_L is a lower-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0A	RTC_MR_D_L	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_l							

Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_l	Lower eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_H to indicate the matched day. The day range is 0–65535.

RTC_MR_D_H

RTC_MR_D_H is an upper-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0B	RTC_MR_D_H	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_h							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_h	Upper eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_L to indicate the matched day. The day range is 0–65535.

RTC_LR_10MS

RTC_LR_10MS is a configured value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x0C	RTC_LR_10MS	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_lr_10ms						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RW	rtc_lr_10ms	Configured value of the RTC 10 ms counter The value range is 0–99.

RTC_LR_S

RTC_LR_S is a configured value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x0D	RTC_LR_S	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_lr_s					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_lr_s	Configured value of the RTC second counter The value range is 0–59.

RTC_LR_M

RTC_LR_M is a configured value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x0E	RTC_LR_M	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_lr_m					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_lr_m	Configured value of the RTC minute counter The value range is 0–59.

RTC_LR_H

RTC_LR_H is a configured value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x0F	RTC_LR_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_lr_h				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved
[4:0]	RW	rtc_lr_h	Configured value of the RTC hour counter The value range is 0–23.

RTC_LR_D_L

RTC_LR_D_L is a lower-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x10	RTC_LR_D_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_l	Lower eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_H to indicate the configured day. The day range is 0–65535.

RTC_LR_D_H

RTC_LR_D_H is an upper-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x11	RTC_LR_D_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_h							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_h	Upper eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_L to indicate the configured day. The day range is 0–65535.

RTC_LORD

RTC_LORD is an RTC configured value loading enable register.

Offset Address	Register Name	Total Reset Value
0x12	RTC_LORD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					rtc_lock_bypass	rtc_lock	rtc_load
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RO	reserved	Reserved
[2]	RW	rtc_lock_bypass	RTC lock enable 0: enabled. The RTC count value (0x00−0x05) is updated only after the RTC is successfully locked. 1: disabled. The RTC count value (0x00−0x05) is updated in real time.
[1]	RW	rtc_lock	RTC lock. If software writes 1, this field is automatically cleared by hardware after the RTC is successfully locked. Note: This field is valid only when rtc_lock_bypass is 0.
[0]	RW	rtc_load	RTC configured value loading enable. When the field is enabled, the RTC configured value will be loaded to the RTC accumulator. If software writes 1 to load the configured value, this field is automatically cleared by hardware after successful loading.

RTC_IMSC

RTC_IMSC is an RTC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x13	RTC_IMSC	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					rtc_imsc	rtc_imsc_uv	rtc_imsc
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RO	reserved	Reserved
[2]	RW	rtc_imsc	RTC global interrupt output enable 0: disabled 1: enabled
[1]	RW	rtc_imsc_uv	Battery low voltage detection interrupt output enable 0: disabled 1: enabled
[0]	RW	rtc_imsc	RTC timing interrupt enable 0: disabled 1: enabled

RTC_INT_CLR

RTC_INT_CLR is an RTC interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x14	RTC_INT_CLR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_int_clr
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved
[0]	RW	rtc_int_clr	RTC interrupt clear register. Software writes any value to clear the interrupt. Reading back the value has no effect.

RTC_MSC_INT

RTC_MSC_INT is an RTC mask interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15	RTC_MSC_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						mask_int_uv	mask_int
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved
[1]	RO	mask_int_uv	Masked battery low voltage detection interrupt status
[0]	RO	mask_int_time	Masked RTC timing interrupt status

RTC_RAW_INT

RTC_RAW_INT is an RTC raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16	RTC_RAW_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						raw_int_uv	raw_int
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved
[1]	RO	raw_int_uv	Battery low voltage detection raw interrupt status
[0]	RO	raw_int	Raw interrupt status

RTC_CLK

RTC_CLK is an RTC output clock select register.

Offset Address	Register Name	Total Reset Value
0x17	RTC_CLK	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						clk_out_sel	

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved
[1:0]	RW	clk_out_sel	Output test clock of the RTC 00: output crystal oscillator clock 01: output corrected 100 Hz clock 1x: output 1 Hz clock

RTC_POR_N

RTC_POR_N is an RTC reset control register.

Offset Address	Register Name	Total Reset Value
0x18	RTC_POR_N	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_por_n
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved
[0]	RW	rtc_por_n	RTC reset. This field is automatically set to 1 after the RTC is successfully reset. 0: reset

SDM_COEF_OUSIDE_H

SDM_COEF_OUSIDE_H is an external upper-4-bit clock divider register.

Offset Address	Register Name	Total Reset Value
0x51	SDM_COEF_OUSIDE_H	0x8

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Sdm_coef_ouside_h			
Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved
[3:0]	RW	Sdm_coef_ouside_h	Upper 4 bits of the clock divider in fixed frequency-division mode

SDM_COEF_OUSIDE_L

SDM_COEF_OUSIDE_L is an external lower-8-bit clock divider register.

Offset Address	Register Name	Total Reset Value
0x52	SDM_COEF_OUSIDE_L	0x1B

Bit	7	6	5	4	3	2	1	0
Name	Sdm_coef_ouside_l							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	Sdm_coef_ouside_l	Lower eight bits of the clock divider in fixed frequency-division mode Note: When Sdm_coef_ouside_h and Sdm_coef_ouside_l are read or written, you need to read or write to the upper four bits and then the lower eight bits continuously.

USER_REGISTER1

USER_REGISTER1 is 64-bit user register 1.

Offset Address	Register Name	Total Reset Value
0x53	USER_REGISTER1	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register1							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register1	64-bit user register 1 corresponding to bit[7:0]

USER_REGISTER2

USER_REGISTER2 is 64-bit user register 2.

Offset Address	Register Name	Total Reset Value
0x54	USER_REGISTER2	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register2							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register2	64-bit user register 2 corresponding to bit[15:8]

USER_REGISTER3

USER_REGISTER3 is 64-bit user register 3.

Offset Address	Register Name	Total Reset Value
0x55	USER_REGISTER3	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register3							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register3	64-bit user register 3 corresponding to bit[23:16]

USER_REGISTER4

USER_REGISTER4 is 64-bit user register 4.

Offset Address	Register Name	Total Reset Value
0x56	USER_REGISTER4	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register4							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register4	64-bit user register 4 corresponding to bit[31:24]

USER_REGISTER5

USER_REGISTER5 is 64-bit user register 5.

Offset Address	Register Name	Total Reset Value
0x57	USER_REGISTER5	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register5							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register5	64-bit user register 5 corresponding to bit[39:32]

USER_REGISTER6

USER_REGISTER6 is 64-bit user register 6.

Offset Address	Register Name	Total Reset Value
0x58	USER_REGISTER6	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register6							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register6	64-bit user register 6 corresponding to bit[47:40]

USER_REGISTER7

USER_REGISTER7 is 64-bit user register 7.

Offset Address	Register Name	Total Reset Value
0x59	USER_REGISTER7	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register7							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register7	64-bit user register 7 corresponding to bit[55:48]

USER_REGISTER8

USER_REGISTER8 is 64-bit user register 8.

Offset Address	Register Name	Total Reset Value
0x5A	USER_REGISTER8	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register8							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register8	64-bit user register 8 corresponding to bit[63:56]

3.11 PMC

3.11.1 Function Description

The power management controller (PMC) provides basic information about power consumption management of the Hi3521A and controls the power consumption.

- PWM output

  The PMC provides a programmable PWM module. The peripheral PWM voltage scaling circuit can be used to adjust the voltages of the CPU power supply and core power supply through two PWM outputs respectively of the Hi3521A.

NOTE

For Hi3521A , the voltages of the CPU power supply and core power supply are adjusted through two PWM outputs respectively.

- HPM control

  The high performance monitor (HPM) can be used to obtain the comprehensive PVT information about the Hi3521A. The reference power supply voltage scaling solution can be developed based on the PVT information.

- Hardware AVS

  After the hardware adaptive voltage scaling (AVS) function is enabled, the Hi3521A obtains the HPM monitoring value periodically. The PWM output duty cycle is adjusted based on the configured policy to implement adaptive adjustment of the power supply voltage.

- Internal temperature detection

  The Hi3521A has an integrated temperature sensor used for obtaining the internal temperature and providing temperature information for temperature protection.

3.11.2 Operating Mode

3.11.2.1 PWM Output

The PWM module in the PMC has a 24 MHz working clock, a 16-bit cycle counter, and a 16-bit duty cycle counter. The count cycle and duty cycle of the PWM output can be specified by configuring the PWM-related registers in the PMC.

To configure the count cycle and duty cycle of the PWM output, perform the following steps:

Step 1 Calculate the number of PWM count cycles and count value of the high level based on the PWM output frequency and duty cycle.

The number of count cycles is calculated as follows:

pwm_period = (24000000/Frequency) − 1

The count value of the high level is calculated as follows:

pwm_duty = (24000000/Frequency) x duty cycle − 1

Step 2 Configure the PWM count cycle and high level count register.

Step 3 Enable the PWM output.

----End

For example, the voltage of the core power supply is controlled by the PWM0 signal. Perform the following steps if the required PWM0 output frequency is 200 kHz and the duty cycle is 75%:

Step 1 Calculate the required number of count cycles and count value of the high level.

pwm_period = (24000000/200000) − 1 = 119

pwm_duty = (24000000/200000) x 0.75 – 1 = 89

Step 2 Configure the parameters of the PWM corresponding to the core power supply by setting PERI_PMC0 bit[15:0] to **0x77** and PERI_PMC0 bit[31:16] to **0x59**.

Step 3 Enable the PWM corresponding to the core power supply by setting PERI_PMC4 bit[0] to **1**.

----End

3.11.2.2 HPM Control

The Hi3521A has two HPMs used for obtaining the PVT information about the core module and the CPU module respectively.

The SYS AXI working clock is used as the working clock of the HPM for the core module and the CPU working clock is used as the working clock of the HPM for the CPU module. You are advised to set core_hpm_div and cpu_hpm_div to appropriate values to ensure that the HPM monitoring value is precise and the frequency of the HPM working clock is about 50 MHz.

The following section describes the HPM configuration procedure by taking the HPM monitoring value of the core module as an example:

Step 1 Set the HPM capture mode.

The HPM has two capture modes, single capture mode and cyclic capture mode. For details, see the description of the PERI_PMC10 register.

If the cyclic capture mode is used, the capture cycle needs to be configured. The capture cycle (in ms) is calculated as follows: T = (N x 2048 + M x 16)/1000.

Where N = PERI_PMC13 bit[31:24] and M = PERI_PMC13 bit[7:0]

Step 2 Calculate the value of core_hpm_div based on the frequency of SYS AXI, deassert reset, and start the cyclic HPM monitoring mode.

For example, if the frequency of SYS AXI is 200 MHz, core_hpm_div is calculated as follows: core_hpm_div = (200 MHz/50 MHz) – 1 = 3. Set PERI_PMC10 and PERI_PMC10 to **0x04000003** and **0x05000003** respectively in sequence. Then enable the cyclic HPM monitoring mode.

Step 3 Read the HPM monitoring value.

In single capture mode, only HPM original code pattern 0 recorded in PERI_PMC11 bit[9:0] is valid.

In cyclic capture mode, the latest four HPM original code patterns (patterns 0−3) are recorded in PERI_PMC11 bit[9:0], PERI_PMC11 bit[21:12], PERI_PMC12 bit[9:0], and PERI_PMC12 bit[21:12] respectively. HPM original code pattern 0 is the latest captured value.

----End

3.11.2.3 Hardware AVS

The Hi3521A automatically adjusts the PWM output duty cycle based on the HPM monitoring value by using the hardware AVS function of the PMC to implement automatic power supply voltage scaling.

The Hi3521A supports hardware AVS for the HPMs of the core module and CPU module. The following describes the hardware AVS start process by taking the core module as an example:

Step 1 Specify the hardware AVS calculation mode by configuring PERI_PMC5 bit[2:1].

Step 2 Specify the voltage scaling step of hardware AVS by configuring PERI_PMC5 bit[31:16].

Step 3 Enable hardware AVS by setting PERI_PMC5 bit[0] to **1**.

----End

3.11.2.4 Internal Temperature Detection

The Hi3521A has an integrated temperature sensor and the detected temperature ranges from −40ºC to +140ºC. To enable the temperature sensor to collect data, perform the following steps:

Step 1 Set the capture mode of the temperature sensor.

The temperature sensor captures the temperature in two modes, the single capture mode and cyclic capture mode. For details, see the description of the PERI_PMC68 register.

If the cyclic capture mode is used, the capture cycle needs to be configured. The capture cycle (in ms) is calculated as follows: Capture cycle = tsensor_monitor_period x 2.

Step 2 Enable the temperature sensor to start collecting the temperature code.

Step 3 Read the temperature code captured by the temperature sensor by using software.

In single capture mode, only temperature code 0 recorded in PERI_PMC69 bit[7:0] is valid.

In cyclic capture mode, the latest eight temperature codes (codes 0−7) are recorded in the registers PERI_PMC69 [31:0] and PERI_PMC70 [31:0]. Temperature code 0 is the latest temperature data.

Step 4 Calculate the corresponding temperature value based on the temperature code.

The temperature value (in ºC) is calculated as follows: T = (tsensor_temp_code x 180/256) − 40.

----End

3.11.3 PMC Register Summary

Table 3-20 describes PMC registers.

Table 3-20 Summary of PMC registers (base address: 0x120E_0000)

Offset Address	Register	Description	Page
0x0000	PERI_PMC0	PMC register 0	3-202
0x0004	PERI_PMC1	PMC register 1	3-202
0x0010	PERI_PMC4	PMC register 4	3-202
0x0014	PERI_PMC5	PMC register 5	3-203
0x0020	PERI_PMC8	PMC register 8	3-204
0x0028	PERI_PMC10	Core high performance monitor (HPM) control register 1	3-205
0x002C	PERI_PMC11	Core HPM status register 1	3-206
0x0030	PERI_PMC12	Core HPM status register 2	3-207
0x0034	PERI_PMC13	Core HPM control register 2	3-208
0x0058	PERI_PMC22	CPU HPM control register 1	3-209
0x005C	PERI_PMC23	CPU HPM status register 1	3-210
0x0060	PERI_PMC24	CPU HPM status register 2	3-211
0x0064	PERI_PMC25	CPU HPM control register 2	3-211
0x00B4	PERI_PMC45	Core TS status register 0	3-212
0x00B8	PERI_PMC46	Core TS status register 1	3-213
0x00BC	PERI_PMC47	Core TS status register 2	3-213
0x00C0	PERI_PMC48	Core TS status register 3	3-213
0x00C4	PERI_PMC49	CPU TS status register 0	3-214
0x00C8	PERI_PMC50	CPU TS status register 1	3-214
0x00CC	PERI_PMC51	CPU TS status register 2	3-215
0x00D0	PERI_PMC52	CPU TS status register 3	3-215
0x0110	PERI_PMC68	PMC register 68	3-216
0x0114	PERI_PMC69	PMC register 69	3-217
0x0118	PERI_PMC70	PMC register 70	3-217
0x011C	PERI_PMC71	PMC register 71	3-218

3.11.4 PMC Register Description

PERI_PMC0

PERI_PMC0 is PMC register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_PMC0	0x0012_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_pwm_duty																core_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	core_pwm_duty	Number of pulse-width modulation (PWM) high-level beats for the core AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	core_pwm_period	Number of PWM cycles for the core AVS output

PERI_PMC1

PERI_PMC1 is PMC register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_PMC1	0x0012_0078

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cpu_pwm_duty																cpu_pwm_period															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cpu_pwm_duty	Number of PWM high-level beats for the CPU AVS output. If the number is greater than or equal to the number of PWM cycles, the output level is always high. The value cannot be 0. If the configured value is 0, the value 1 is used.
[15:0]	RW	cpu_pwm_period	Number of PWM cycles for the CPU AVS output

PERI_PMC4

PERI_PMC4 is PMC register 4.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_PMC4	0x0000_0405

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					pwm1_reuse_cfg	reserved	pwm0_reuse_cfg	reserved				cpu_pwm_inv	cpu_pwm_enable	core_pwm_inv	core_pwm_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10]	RW	pwm1_reuse_cfg	PWM1 source select for the AVS output 0: core 1: CPU
[9]	RO	reserved	Reserved
[8]	RW	pwm0_reuse_cfg	PWM0 source select for the AVS output 0: core 1: CPU
[7:4]	RO	reserved	Reserved
[3]	RW	cpu_pwm_inv	PWM phase control for the CPU AVS output 0: normal output 1: inverted output
[2]	RW	cpu_pwm_enable	PWM enable for the CPU AVS output 0: disabled 1: enabled
[1]	RW	core_pwm_inv	PWM phase control for the core AVS output 0: normal output 1: inverted output
[0]	RW	core_pwm_enable	PWM enable for the core AVS output 0: disabled 1: enabled

PERI_PMC5

PERI_PMC5 is PMC register 5.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_PMC5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_avs_fsm_inc_pwm_step								core_avs_fsm_dec_pwm_step				reserved																		core_avs_hpm_fsm_calc_mode		core_hpm_fsm_en	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	core_avs_fsm_inc_pwm_step	Automatic increase step of the core AVS FSM PWM
[23:16]	RW	core_avs_fsm_dec_pwm_step	Automatic decrease step of the core AVS FSM PWM
[15:3]	RO	reserved	Reserved
[2:1]	RW	core_avs_hpm_fsm_calc_mode	Calculation mode of the core AVS HPM FSM 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	core_hpm_fsm_en	Core AVS HPM FSM enable 0: disabled 1: enabled

PERI_PMC8

PERI_PMC8 is PMC register 8.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_PMC8	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	cpu_avs_fsm_inc_pwm_step		cpu_avs_fsm_dec_pwm_step		reserved			cpu_avs_hpm_fsm_calc_mode		cpu_hpm_fsm_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0		0

Bits	Access	Name	Description
[31:24]	RW	cpu_avs_fsm_inc_pwm_step	Automatic increase step of the CPU AVS FSM PWM
[23:16]	RW	cpu_avs_fsm_dec_pwm_step	Automatic decrease step of the CPU AVS FSM PWM
[15:3]	RO	reserved	Reserved
[2:1]	RW	cpu_avs_hpm_fsm_calc_mode	Calculation mode of the CPU AVS HPM FSM 00: average value of four samplings 01: average value of eight samplings 10: average value of 16 samplings 11: average value of 32 samplings
[0]	RW	cpu_hpm_fsm_en	CPU AVS HPM FSM enable 0: disabled 1: enabled

PERI_PMC10

PERI_PMC10 is core HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_PMC10	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				core_hpm_srst_req	core_hpm_monitor_en	core_hpm_bypass	core_hpm_en	reserved				core_hpm_offset								reserved		core_hpm_shift		reserved				core_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	core_hpm_srst_req	Core HPM reset request 0: deassert reset 1: reset
[26]	RW	core_hpm_monitor_en	Core HPM cyclic monitoring enable 0: disabled 1: enabled
[25]	RW	core_hpm_bypass	Core HPM cyclic monitoring bypass 0: not bypassed 1: bypassed
[24]	RW	core_hpm_en	Core HPM measurement enable 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	WO	reserved	Reserved
[21:12]	RW	core_hpm_offset	Core HPM offset
[11:10]	RO	reserved	Reserved
[9:8]	RW	core_hpm_shift	Core HPM shift
[7:6]	RO	reserved	Reserved
[5:0]	RW	core_hpm_div	Core HPM clock divider n: divn

PERI_PMC11

PERI_PMC11 is core HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_PMC11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						core_hpm_up_warning	core_hpm_low_warning	reserved				core_hpm_pc_record1								reserved	core_hpm_pc_valid	core_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RO	core_hpm_up_warning	Upper limit for the core HPM warning
[24]	RO	core_hpm_low_warning	Lower limit for the core HPM warning
[23:22]	RO	reserved	Reserved
[21:12]	RO	core_hpm_pc_record1	Core HPM original code pattern 1
[11]	RO	reserved	Reserved
[10]	RO	core_hpm_pc_valid	Core HPM output validity indicator 0: invalid 1: valid
[9:0]	RO	core_hpm_pc_record0	Core HPM original code pattern 0

PERI_PMC12

PERI_PMC12 is core HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_PMC12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				core_hpm_rcc				reserved				core_hpm_pc_record3								reserved				core_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RO	core_hpm_rcc	Core HPM output with the RCC code
[23:22]	RO	reserved	Reserved
[21:12]	RO	core_hpm_pc_record3	Core HPM original code pattern 3
[11:10]	RO	reserved	Reserved
[9:0]	RO	core_hpm_pc_record2	Core HPM original code pattern 2

PERI_PMC13

PERI_PMC13 is core HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_PMC13	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_hpm_monitor_period								reserved				core_hpm_lowlimit								reserved				core_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	core_hpm_monitor_period	Core HPM cyclic monitoring period If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved

[21:12]	RW	core_hpm_lowlimit	Core HPM lower limit
[11:10]	RO	reserved	Reserved
[9:0]	RW	core_hpm_uplimit	Core HPM upper limit

PERI_PMC22

PERI_PMC22 is CPU HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0058	PERI_PMC22	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_hpm_srst_req	cpu_hpm_monitor_en	cpu_hpm_bypass	cpu_hpm_en	reserved				cpu_hpm_offset								reserved		cpu_hpm_shift		reserved				cpu_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	cpu_hpm_srst_req	CPU HPM reset request, active high 0: deassert reset 1: reset
[26]	RW	cpu_hpm_monitor_en	CPU HPM cyclic monitoring enable 0: disabled 1: enabled
[25]	RW	cpu_hpm_bypass	CPU HPM cyclic monitoring bypass 0: not bypassed 1: bypassed
[24]	RW	cpu_hpm_en	CPU HPM measurement enable 0: The value retains 0 before a process is started. 1: A frequency modulation process is started.
[23:22]	RO	reserved	Reserved
[21:12]	RW	cpu_hpm_offset	CPU HPM offset
[11:10]	RO	reserved	Reserved
[9:8]	RW	cpu_hpm_shift	CPU HPM shift

[7:6]	RW	reserved	Reserved
[5:0]	RW	cpu_hpm_div	CPU HPM clock divider n: divn

PERI_PMC23

PERI_PMC23 is CPU HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_PMC23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						cpu_hpm_up_warning	cpu_hpm_low_warning	reserved				cpu_hpm_pc_record1								reserved	cpu_hpm_pc_valid	cpu_hpm_pc_record0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RO	cpu_hpm_up_warning	Upper limit for the CPU HPM warning
[24]	RO	cpu_hpm_low_warning	Lower limit for the CPU HPM warning
[23:22]	RO	reserved	Reserved
[21:12]	RO	cpu_hpm_pc_record1	CPU HPM original code pattern 1
[11]	RO	reserved	Reserved
[10]	RO	cpu_hpm_pc_valid	CPU HPM output validity indicator 0: invalid 1: valid
[9:0]	RO	cpu_hpm_pc_record0	CPU HPM original code pattern 0

PERI_PMC24

PERI_PMC24 is CPU HPM status register 2.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_PMC24	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_hpm_rcc				reserved				cpu_hpm_pc_record3								reserved				cpu_hpm_pc_record2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RO	cpu_hpm_rcc	CPU HPM output with the RCC code
[23:22]	RO	reserved	Reserved
[21:12]	RO	cpu_hpm_pc_record3	CPU HPM original code pattern 3
[11:10]	RO	reserved	Reserved
[9:0]	RO	cpu_hpm_pc_record2	CPU HPM original code pattern 2

PERI_PMC25

PERI_PMC25 is CPU HPM control register 2.

Offset Address	Register Name	Total Reset Value
0x0064	PERI_PMC25	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cpu_hpm_monitor_period								reserved				cpu_hpm_lowlimit								reserved				cpu_hpm_uplimit							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	cpu_hpm_monitor_period	CPU HPM cyclic monitoring period If the configured value is *N*, the monitoring period (T) is as follows: T = *N* x 2048/1000 ms The maximum monitoring interval is 522 ms, and the minimum interval is 2 ms.
[23:22]	RO	reserved	Reserved
[21:12]	RW	cpu_hpm_lowlimit	CPU HPM lower limit
[11:10]	RO	reserved	Reserved
[9:0]	RW	cpu_hpm_uplimit	CPU HPM upper limit

PERI_PMC45

PERI_PMC45 is core TS status register 0.

Offset Address	Register Name	Total Reset Value
0x00B4	PERI_PMC45	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								core_ts_record1								reserved				core_ts_ record0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	core_ts_record1	Core TS record register 1
[15:11]	RO	reserved	Reserved
[10:0]	RO	core_ts_ record0	Core TS record register 0

PERI_PMC46

PERI_PMC46 is core TS status register 1.

Offset Address	Register Name	Total Reset Value
0x00B8	PERI_PMC46	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								core_ts_record3								reserved				core_ts_record2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	core_ts_record3	Core TS record register 3
[15:11]	RO	reserved	Reserved
[10:0]	RO	core_ts_record2	Core TS record register 2

PERI_PMC47

PERI_PMC47 is core TS status register 2.

Offset Address	Register Name	Total Reset Value
0x00BC	PERI_PMC47	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								core_ts_record5								reserved				core_ts_record4											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	core_ts_record5	Core TS record register 5
[15:11]	RO	reserved	Reserved
[10:0]	RO	core_ts_record4	Core TS record register 4

PERI_PMC48

PERI_PMC48 is core TS status register 3.

Offset Address	Register Name	Total Reset Value
0x0C0	PERI_PMC48	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				core_ts_record7												reserved				core_ts_record6											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	core_ts_record7	Core TS record register 7
[15:11]	RO	reserved	Reserved
[10:0]	RO	core_ts_record6	Core TS record register 6

PERI_PMC49

PERI_PMC49 is CPU TS status register 0.

Offset Address	Register Name	Total Reset Value
0x00C4	PERI_PMC49	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_ts_record1												reserved				core_ts_ record0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	cpu_ts_record1	CPU TS record register 1
[15:11]	RO	reserved	Reserved
[10:0]	RO	core_ts_ record0	CPU TS record register 0

PERI_PMC50

PERI_PMC50 is CPU TS status register 1.

Offset Address	Register Name	Total Reset Value
0x00C8	PERI_PMC50	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_ts_record3												reserved				cpu_ts_record2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	cpu_ts_record3	CPU TS record register 3
[15:11]	RO	reserved	Reserved
[10:0]	RO	cpu_ts_record2	CPU TS record register 2

PERI_PMC51

PERI_PMC51 is CPU TS status register 2.

Offset Address	Register Name	Total Reset Value
0x00CC	PERI_PMC51	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cpu_ts_record5												reserved				cpu_ts_record4											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	cpu_ts_record5	CPU TS record register 5
[15:11]	RO	reserved	Reserved
[10:0]	RO	cpu_ts_record4	CPU TS record register 4

PERI_PMC52

PERI_PMC52 is CPU TS status register 3.

Offset Address	Register Name	Total Reset Value
0x0D0	PERI_PMC52	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cpu_ts_record7								reserved				cpu_ts_record6											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RO	cpu_ts_record7	CPU TS record register 7
[15:11]	RO	reserved	Reserved
[10:0]	RO	cpu_ts_record6	CPU TS record register 6

PERI_PMC68

PERI_PMC68 is PMC register 68.

Offset Address	Register Name	Total Reset Value
0x110	PERI_PMC68	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	tsensor_en	tsensor_monitor_en	reserved					tsensor_monitor_period								tsensor_temp_uplimit								tsensor_temp_lowlimit							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	tsensor_en	Temperature sensor enable 0: disabled 1: enabled
[29]	RW	tsensor_monitor_en	Cyclic temperature monitoring enable 0: disabled 1: enabled
[28:24]	RO	reserved	Reserved

[23:16]	RW	tsensor_monitor_period	Cyclic temperature monitoring cycle. The timing reference is 1 ms.
[15:8]	RW	tsensor_temp_uplimit	Temperature overflow value
[7:0]	RW	tsensor_temp_lowlimit	Temperature underflow value

PERI_PMC69

PERI_PMC69 is PMC register 69.

Offset Address	Register Name	Total Reset Value
0x0114	PERI_PMC69	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	tsensor_temp_code3		tsensor_temp_code2		tsensor_temp_code1		tsensor_temp_code0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	tsensor_temp_code3	Temperature record value 3
[23:16]	RO	tsensor_temp_code2	Temperature record value 2
[15:8]	RO	tsensor_temp_code1	Temperature record value 1
[7:0]	RO	tsensor_temp_code0	Temperature record value 0

PERI_PMC70

PERI_PMC70 is PMC register 70.

Offset Address	Register Name	Total Reset Value
0x0118	PERI_PMC70	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	tsensor_temp_code7		tsensor_temp_code6		tsensor_temp_code5		tsensor_temp_code2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	tsensor_temp_code7	Temperature record value 7

[23:16]	RO	tsensor_temp_code6	Temperature record value 6
[15:8]	RO	tsensor_temp_code5	Temperature record value 5
[7:0]	RO	tsensor_temp_code4	Temperature record value 4

PERI_PMC71

PERI_PMC71 is PMC register 71.

Offset Address	Register Name	Total Reset Value
0x011C	PERI_PMC71	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								tsensor_low_warning	tsensor_up_warning
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	tsensor_low_warning	Temperature underflow alarm 0: no alarm 1: underflow alarm
[0]	RO	tsensor_up_warning	Temperature overflow alarm 0: no alarm 1: overflow alarm

3.12 Power Management and Low-Power Mode Control

3.12.1 Overview

In low-power mode, the power consumption of the chip is reduced effectively. The Hi3535 reduces its power consumption in the following low-power control modes:

- Clock gating and clock frequency adjustment

  The clock disabling function is used to disable unnecessary clocks to reduce the power consumption of the chip. In addition, the frequency of the system working clock can be adjusted. That is, when the function requirement is met, you can adjust the clock frequency to reduce the power consumption of the chip.

- Module low-power control

  When a module is idle, it can be disabled or switched to low-power mode to reduce the power consumption.

- DDR low-power control

  The power consumption of the DDRC and related pins can be controlled dynamically. You can enable this function to reduce the power consumption of the chip. You can also enable the self-refresh function of the DDR to reduce the power consumption of the entire product.

3.12.2 Clock Gating and Clock Frequency Adjustment

The system supports clock gating of each module. When a module is idle, its clock can be disabled to reduce the power consumption of the chip. For details about the process, see the description in the section of "clock gating" of each module.

The system can adjust its working frequency to reduce the power consumption of the chip. To adjust the system working frequency, perform the following steps:

- Disable the service module to prevent it from accessing the DDR.
- Enable the system to run in the off-chip memory.

Step 1 When DDRC_CTRL_SREF[sr_seq] is set to a valid value, the DDRC forces the DDRn SDRAM to enter the self-refresh mode.

NOTE

For details about the DDRC_CTRL_SREF register, see section 4.1.7 "DMC Registers of the DDRC" in chapter 4 "Memory Interfaces."

Step 2 Configure PERI_CRG_PLLn to control the PLL frequency divider..

Step 3 Wait a moment and configure DDRC_CTRL_SREF to enable the DDRC to exit the self-refresh mode based on the configuration requirements of the DDRC.

Step 4 The program starts to run in the DDR.

----End

The working frequencies of some modules can also be adjusted separately. This reduces the power consumption of the system further. For details about the clock source of each module, see section 3.2.5 "Frequency Configurations."

3.12.3 Module Low-Power Control

Most modules including USB 2.0 host, SATA, Video DAC (VDAC), and PLL modules support low-power operating modes. For details, see the descriptions of the system controller, VDP, and clocks.

- Low-power control for the USB 2.0 host module:

  If the USB 2.0 host is not used, it can be disabled to switch the USB 2.0 host clock by setting PERI_CRG28 bit[7] to 0.

- Low-power control for the SATA port 0 and SATA port 1 modules
  - If the SATA is not used, it can be disabled to switch the SATA PHY 0 working clock by setting PERI_CRG26 bit[0]
  - If the SATA is not used, it can be disabled to switch the SATA PHY 1 reference clock by setting PERI_CRG26 bit[2] to 0.
- Low-power control for the VDAC

  Unused VDAC channels can be disabled to reduce power consumption. For details, see section 11.5.2 "Registers Description."
- The PLL also supports the low-power mode. If the PLL is not used, it can be disabled to switch the system to low-power mode. For details, see the description of the power-down control bit in the CRG register PERI_CRG_PLLn.

3.12.4 DDR Low-Power Control

For details about the low-power control mode of the DDRC, see the description of "Configuring the Low-Power Mode" in section 4.1.4 "Operating Mode."

Contents

Figures

Tables

4 Memory Interfaces

4.1 DDRC

4.1.1 Overview

The DDR3 synchronous dynamic random access memory (SDRAM) controller (DDRC) controls access to the DDR3 SDRAM.

NOTE

The Hi3521A supports the 32-bit mode and Hi3520D V300 supports the 16-bit mode.

4.1.2 Features

The DDRC has the following features:

- Space for one DDR3 SDRAM chip select (CS) and 16/32-bit DDR3 SDRAM data bus
- Maximum 8 GB storage space
- 800 MHz DDR3 SDRAM interface clock frequency and 1.6 Gbit/s data rate
- Various DDR3 SDRAM low-power modes, such as the power-down and self-refresh modes
- INCR and wrap commands for the DDR3 SDRAM burst 8 transfer mode

4.1.3 Function Description

4.1.3.1 Application Block Diagram

The DDRC enables the master devices of the SoC such as the CPU to access the external DDR3 SDRAM. It supports the DDR3 SDRAM that complies with the JEDEC (JESD79) standard after the timing parameter registers of the DDRC are configured by using the CPU. Table 4-1 lists the mainstream DDR3 SDRAM supported by the DDRC. The descriptions in Table 4-1 are based on the working frequencies of DDR3 SDRAM. The restrictions such as the capacity are not taken into account.

Table 4-1 DDR3 SDRAMs supported by the DDRC

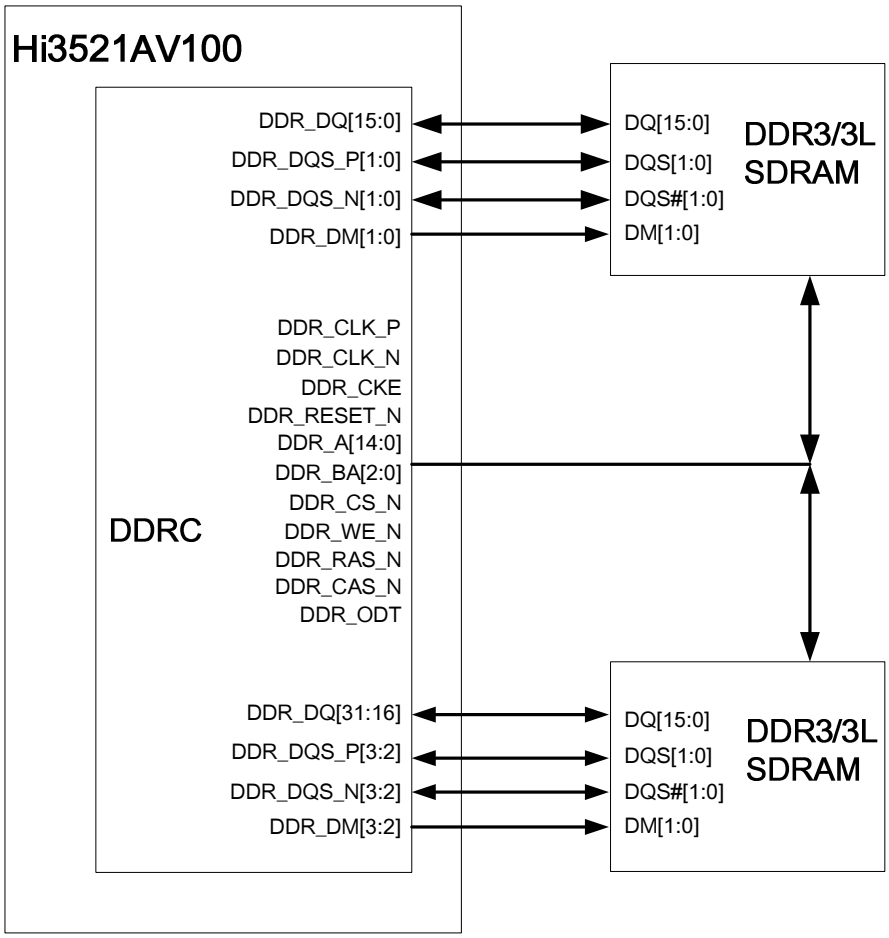
Vendor	800 MHz	933 MHz
Samsung	DDR3-1600 DDR3-1866 DDR3-2133	DDR3-1866 DDR3-2133
lanya	DDR3-1600 DDR3-1866 DDR3-2133	DDR3-1866 DDR3-2133
Hynix	DDR3-1600 DDR3-1866 DDR3-2133	DDR3-1866 DDR3-2133

NOTE

For details about the supported component types, see the JEDEC standard and the component data sheet.

Hi3521A supports the 32-bit interconnection mode. Figure 4-1 show the connection between the DDRC and DDR3 SDRAMs in 32-bit interconnection mode..

Figure 4-1 Connecting the DDRC to two 16-bit DDR3 SDRAMs in 32-bit interconnection mode

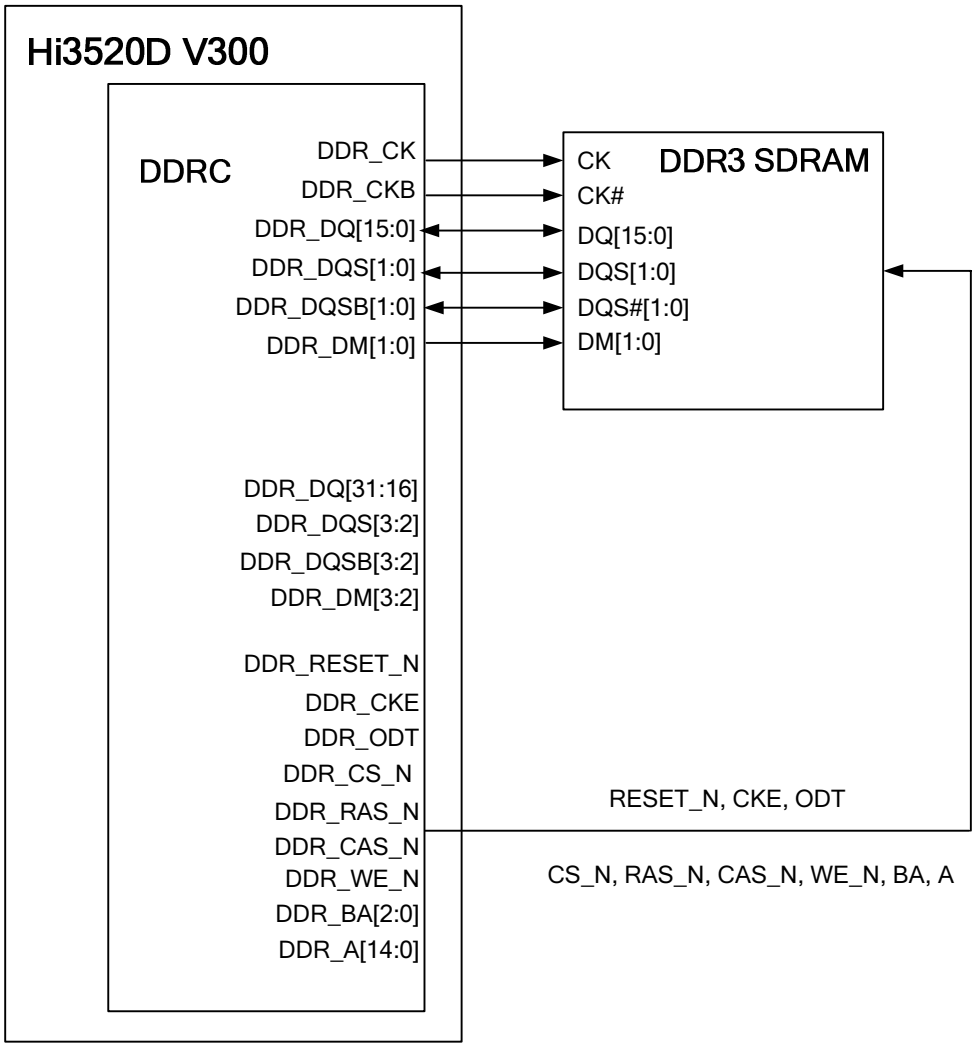


NOTE

The DDRC connects to two 16-bit DDR3 SDRAMs. The command control signals (DDR_CS_N, DDR_CKE, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[14:0], and DDR_ODT) of the DDRC connect to those of the DDR3 SDRAMs respectively. The command control bus of the DDRC uses the one-drive-two connection mode.

Hi3520D V300 supports the 16-bit interconnection mode. Figure 4-2 show the connection between the DDRC and DDR3 SDRAMs in 16-bit interconnection mode

Figure 4-2 Connecting the DDRC to one 16-bit DDR3 SDRAM in 16-bit interconnection mode



NOTE

The DDRC connects to one 16-bit DDR3 SDRAM. The command control signals (DDR_CS_N, DDR_CKE, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], DDR_A[14:0], and DDR_ODT) of the DDRC connect to those of the DDR3 SDRAM respectively. The command control bus of the DDRC uses the one-drive-one connection mode.

4.1.3.2 Function Implementation

As the timings of the DDRC interface comply with the JESD79 standard, the DDRC can access (read or write) data in the DDR3 SDRAM and control the status of the DDR3 SDRAM (including automatic refresh and low power control) by sending the command words of the DDR3 SDRAM.

Command Truth Value Table

The DDRC can read and write to the DDR3 SDRAM and control command words. Table 4-2 lists the command truth values of the DDRC. For details, see the JEDEC standard and component data sheet.

Table 4-2 Command truth values of the DDR3

Function	DDR3_CKE	DDR3_CSN	DDR3_RASN	DDR3_CASN	DDR3_WEN	DDR3_ADR			DDR3_BA
						15:11	AP(10)	9:0	
DESELECT	H	H	X	X	X	X	X	X	X
ACTIVE	H	L	L	H	H	V	V	V	V
READ	H	L	H	L	H	V	V	V	V
WRITE	H	L	H	L	L	V	V	V	V
PRECHARGE	H	L	L	H	L	V	L	V	BA
PRECHARGE ALL	H	L	L	H	L	V	H	V	V
AUTO REFRESH	H	L	L	L	H	V	V	V	V
SELF REFRESH ENTRY	H->L	L	L	L	H	V	V	V	V
SELF REFRESH EXIT	L->H	L	H	H	H	V	V	V	V
MODE REGISTER SET	H	L	L	L	L	V	V	V	V
ZQCL	H	L	H	H	L	X	H	X	X
ZQCS	H	L	H	H	L	X	L	X	X

H: high level; L: low level; V: valid; X: ignored.
ZQ calibration long (ZQCL): starts ZQ calibration on the DDR3 SDRAM when it is initialized during power-on.
ZQ calibration short (ZQCS): starts ZQ calibration on the DDR3 SDRAM when its ambient environment is changed.

Auto Refresh

When DDRC_CFG_TIMING2 [taref] is set to a non-zero value, the DDRC refreshes the DDR3 SDRAM by automatically generating a periodical auto refresh command. At ambient temperature, the DDR3 SDRAM is required to implement 8,192 auto-refresh operations within 64 ms. That is, the auto-refresh cycle is 7.8 μs. The relationship between the value of DDRC_CFG_TIMING2 [taref] (taref) and the auto-refresh cycle T (T = 7.8 μs) is as follows:

$T \geq taref \times (16 \times DDR\ clock\ cycle)$

When DDRC_CFG_TIMING2 [taref] is configured, the internal counter of the DDRC automatically loads the taref value and then counts in decremented mode. When the count value reaches 0, the DDRC initiates an auto-refresh operation and the counter reloads the taref value to count.

Low-Power Management

The DDRC supports two modes of low-power management: common low-power mode and auto-refresh low-power mode.

When DDRC_CFG_PD[pd_en] is set to 1 to enable the SDRAM low-power mode, and the system is idle (the DDR is not read or written through the DDRC bus interface for a period), the DDR3 SDRAM enters the common low-power mode automatically.

To switch the system mode to standby mode, you can force the DDR3 SDRAM to enter the auto-refresh mode by setting DDRC_CTRL_SREF[sref_req] to 1. In this mode, the power consumption of the DDR3 SDRAM is minimized, data in the DDR3 SDRAM is retained, but the system cannot access the DDR3 SDRAM.

Arbitration Mechanism

The DDRC schedules commands by using the priority scheduling algorithms. In addition, the DDRC can control the command requests by using traffic control and timeout control. The two auxiliary scheduling methods can be enabled separately or simultaneously as required.

1. Priority scheduling

Eight priorities (0−7) are provided. The priority of each advanced eXtensible interface (AXI) is configured separately as follows:

Step 1 Select the priority mapping mode by configuring AXI_QOS_MAP[pri_map_mode]. If AXI_QOS_MAP[pri_map_mode] is set to 1, the index is obtained by using the system bus associated signal of the command; if AXI_QOS_MAP[pri_map_mode] is set to 0, AXI_QOS_MAP[id_map_idx] needs to be configured to select any three bits in the command ID to obtain the index.

Step 2 Configure AXI_QOS_WRPRIn and AXI_QOS_RDPRIn.

Step 3 The DDRC queries a value from the eight preset values in the AXI_QOS_WRPRIn or AXI_QOS_RDPRIn register based on the priority index corresponding to each command, and adds this value to the read/write command sent to the bus as the priority attribute of the command. Then the DDRC internal arbiter schedules the commands that raise arbitration requests based on the priority attributes to implement highly effective access to the DDR3 SDRAM.

----End

- Priority adaptation is supported. The priority adaptation function of each port can be enabled by configuring AXI_QOS_ADPTn to ensure that commands with lower priorities will be arbitrated by level. The priority of a command is automatically increased to a higher level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one. The priority increase cycle is (adpt_prd x 16).
- The read and write commands from the same port are aggregated and arbitrated according to either of the following two rules:
  - The commands are arbitrated based on the arrival time. When the read and write commands are sent, the ones from the same port that arrive earlier are arbitrated first. When commands from two ports arrive simultaneously, the read commands are arbitrated before the write commands.
  - The commands are arbitrated based on the priorities.

When the commands are of different priorities, the commands from the port with the highest arbitration priority are arbitrated first.

When the commands are of the same priority, the commands from the port that has not been arbitrated for the longest time are arbitrated first.

2. Traffic control

The traffic is controlled by configuring QOSB_FLUX_EN[flux_en] and grouping the traffic according to the command ID as required. The DDRC allocates each group of traffic to ensure the bandwidth of each port when the traffic is heavy.

3. Timeout control

The mapping mode for the timeout attribute of the command is selected by configuring QOSB_TIMEOUT_MODE[timeout_mode], which is similar to the priority mapping mode. In configured mapping mode, the QoSBuf module in the DDRC queries a value from the 16 preset timeout values based on the timeout index corresponding to each command (the value 0 indicates that the timeout function is disabled), and adds this value to the command as the timeout value of the command. In the DDRC, commands with timeout attributes forcibly prevent commands without timeout attributes from raising arbitration requests and immediately raise arbitration requests when the waiting time elapses.

Traffic Statistics and Command Latency Statistics

The DDRC supports traffic statistics. The interface read and write traffic statistics can be collected to determine whether dynamic frequency scaling (DFS) is required, that is, whether to increase or reduce the DDRC frequency. The DDRC can collect the read and write traffic statistics of a specific ID, or the overall read and write traffic statistics. The DDRC can also collect DDR interface usage statistics. The statistic counter supports the continuous counts and one-time count. When counting continuously, the counter is a non-saturating counter, and it is wrapped when the maximum count is reached to facilitate the continuous count. Therefore, the system needs to read the count value before the counter is wrapped. When counting for only one time, the counter stops counting when the statistic time elapses. The system can obtain the instantaneous traffic and latency by using this function.

The DDRC can collect command latency statistics, including the maximum latency of the read and write access to a specific ID and the accumulative latency statistics.

The process for collecting statistics is as follows:

Step 1 Set the statistic mode to continuous triggering or one-time triggering by configuring DDRC_CFG_STADAT[dat_stat_mode]. If the one-time triggering is selected, set the dat_stat_prd field to configure the statistic cycle.

Step 2 Set the ID for which statistics are to be collected by configuring DDRC_CFG_STAID.

Step 3 Set the mask value of the ID by configuring DDRC_CFG_STAIDMSK. The DDRC determines whether to collect statistics of the current access based on sta_idmask and the accessed ID. Statistics of multiple IDs can be collected by using this method.

Step 4 Enable the statistic function by configuring DDRC_CTRL_PERF[perf_en]. For the one-time count, counting is complete when DDRC_CTRL_PERF[perf_en] restores to 0. For the continuous count, the software needs to write 0 to DDRC_CTRL_PERF[perf_en] to stop counting.

Step 5 Observe the collected statistics by using DDRC_HIS_FLUX_WR, DDRC_HIS_FLUX_RD, DDRC_HIS_FLUX_WCMD, DDR

C_HIS_FLUX_RCMD, DDRC_HIS_FLUXID_WR, DDRC_HIS_FLUXID_RD, DDRC_HIS_FLUXID_WCMD, DDRC_HIS_FLUXID_RCMD, DDRC_HIS_WLATCNT0, DDRC_HIS_WLATCNT1, DDRC_HIS_RLATCNT0, DDRC_HIS_RLATCNT1, and DDRC_HIS_INHERE_RLAT_CNT.

----End

Address Mapping

The DDRC can convert the access address for the system bus into that for the DDR*n* SDRAM (*n* = 3). You can set the address mapping mode to row-bank-column (RBC) by configuring DDRC_CFG_RNKVOL[mem_map]. Currently only the RBC mode is supported. Then you can set the SDRAM row and column address bit width by configuring DDRC_CFG_RNKVOL[mem_row] and DDRC_CFG_RNKVOL[mem_col]. The DDRC then converts the system bus address into the DDR*n* SDRAM (*n* = 3) address based on the address mapping algorithm.

The following describes the mapping algorithms for the system bus address and the address for the DDR*n* SDRAM (*n* = 3) by using the RBC mode as an example. Assume that the system bus address is BUSADR[31:0], the valid address is BUSADR[m – 1:0], and the address for the DDR3 SDRAM is DDRADR[14:0]. When DDRADR[14:0] serves as the row address, its valid address is DDRROW[x – 1:0]; when DDRADR[13:0] serves as the column address, its valid address is DDRCOL[y – 1:0]. In addition, the bank address for the DDR is DDRBA[z – 1:0], the width of the storage data bus of the DDRC is DW, and AXI_REGION_ATTRIB[ch_mode] is 2'b01 (the situation where AXI_REGION_ATTRIB[ch_mode] is 2'b11 is not described). In this case, the address mapping is as follows:

- When DDRC_CFG_RNKVOL[mem_map] is set to 2b00, the RBC mapping mode is as follows:

  BUSADR[m − 1:0] = {DDRROW[x − 1:0], DDRBA[z − 1:0], DDRCOL[y − 1:0], DW{b0}}
- When DDRC_CFG_RNKVOL[mem_map] is set to 2b01, the RBC mapping mode is as follows:

  BUSADR[m − 1:0] = {DDRBA[z − 1:0], DDRROW[x − 1:0], DDRCOL[y − 1:0], DW{b0}}

  In the preceding expressions, the following condition is met: m = x + y + z + DW
  - When the DDRC is in 16-bit mode, the value of DW is 1.
  - When the DDRC is in 32-bit mode, the value of DW is 2.
- When DDRC_CFG_RNKVOL[mem_map] is set to 2'b00 and A10 acts as the AP function bit of the DDR, the mapping between the system bus addresses and the DDR3 SDRAM addresses is shown in Table 4-3 and Table 4-5.

Table 4-3 DDRC DDR3 address mapping in 16-bit mode

Memory Type	Row Address Width	Column Address Width	DDR BA			Row Address or Column Address	DDR ADR							
Mbit x bw			2	1	0		14	13	12	11	10/AP	9	8	[7:0]
512 Mbits 8 banks														

Memory Type	Row Address Width	Column Address Width	DDR BA			Row Address or Column Address	DDR ADR							
Mbit x bw			2	1	0		14	13	12	11	10/AP	9	8	[7:0]
32 x 16	12	10	13	12	11	Row address	-	-	-	25	24	23	22	[21:14]
						Column address	-	-	-	-	AP	-	10	[9:1]
1 Gbits 8 banks														
64 x 16	13	10	13	12	11	Row address	-	-	26	25	24	23	22	[21:14]
						Column address	-	-	-	-	AP	-	10	[9:1]
2 Gbits 8 banks														
128 x 16	14	10	13	12	11	Row address	-	27	26	25	24	23	22	[21:14]
						Column address	-	-	-	-	AP	-	10	[9:1]
4 Gbits 8 banks														
256 x 16	15	10	13	12	11	Row address	28	27	26	25	24	23	22	[21:14]
						Column address	-	-	-	-	AP	-	10	[9:1]

Table 4-4 DDRC DDR3 address mapping in 32-bit mode

Memory Type	Row Address Width	Column Address Width	DDR BA			Row Address or Column Address	DDR ADR							
Mbit x bw			2	1	0		14	13	12	11	10/AP	9	8	[7:0]
512 Mbits 8 banks														
32 x 16	12	10	14	13	12	Row address	-	-	-	26	25	24	23	[22:15]
						Column address	-	-	-	-	AP	11	10	[9:2]
1 Gbits 8 banks														
64 x 16	13	10	14	13	12	Row address	-	-	27	26	25	24	23	[22:15]

Memory Type	Row Address Width	Column Address Width	DDR BA			Row Address or Column Address	DDR ADR							
Mbit x bw			2	1	0		14	13	12	11	10/AP	9	8	[7:0]
						Column address	-	-	-	-	AP	11	10	[9:2]
2 Gbits 8 banks														
128 x 16	14	10	14	13	12	Row address	-	28	27	26	25	24	23	[22:15]
						Column address	-	-	-	-	AP	11	10	[9:2]
4 Gbits 8 banks														
256 x 16	15	10	14	13	12	Row address	29	28	27	26	25	24	23	[22:15]
						Column address	-	-	-	-	AP	11	10	[9:2]

4.1.4 Operating Mode

4.1.4.1 Soft Reset

The DDRC does not support separate soft reset. It can be reset only by a global soft reset. After reset, the DDR3 SDRAM must be reinitialized according to the following initialization processes.

4.1.4.2 Initializing the DDR3 SDRAM

After power-on, the system can access the DDR3 SDRAM only after the DDR3 SDRAM is initialized. Before initializing the DDR3 SDRAM, note the following:

- Power on the DDR3 SDRAM by following the JEDEC standard. That is, you must power on VDD, VDDQ, VREF, and VTT in sequence.
- Initialize the DDR3 SDRAM after the system runs in normal mode.

The following describes the procedure for initializing the DDR subsystem when the ratio of the working frequency of the DDRC to that of the DDR3 SDRAM is 1:2 (400 MHz for the DDRC and 800 MHz (1.6 Gbit/s) for the DDR3 SDRAM):

Step 1 Set the DDRC_CFG_SREF register to 0x2 to exit from the self-refresh mode.

Step 2 Query the DDRC_CURR_FUNC register by using software. If bit[0] of this register is 1'b0, go to step 3.

Step 3 Configure the operating mode, clock frequency, and timing parameters. The related registers involve DDRC_CFG_WORKMODE, DDRC_CFG_RNKVOL, DDRC_CFG_TIMING0, DDRC_CFG_TIMING1, DDRC_CFG_TIMING2, DDRC_CFG_TIMING3, DDRC_CFG_TIMING4, DDRC_CFG_TIMING5, DDRC_CFG_TIMING6, DDRC_CFG_PD, DDRC_CFG_DDRPHY, and DDRC_CFG_ODT.

Step 4 Configure the DDRC_CFG_DDRMODE register to select the external DDR type.

Step 5 Configure the operating mode and time parameters of each DDRPHY, DDRPHY I/O drive, ODT impedance, swap mode, and the delay parameter for the read and write command channels. The related registers involve PACK_PHYTMR0, PHYTMR1, PLLTMR, DLYMEASCTRL, DRAMCFG, ACPHYCTL4, DRAMTMR0, DRAMTMR1, DRAMTMR2, DRAMTMR3, DRAMTMR4, IOCTL, MISC, DQSSEL, DRAM_MR01, and DRAM_MR23.

Step 6 Configure the PLLCTRL register of DDRPHY to power off the DDRPHY PLL.

Step 7 Set the delay time to 200 μs.

Step 8 Configure the PLLCTRL register of DDRPHY to power on the DDRPHY PLL.

Step 9 Set the delay time to 100 μs.

Step 10 Configure the PHYINITCTRL register of DDRPHY to initialize DDRPHY0 and DDRPHY1.

Step 11 Wait until the PHYINITCTRL register of DDRPHY is 0. That is, the initialization of DDRPHY is complete.

Step 12 Configure DDRC_CFG_NXT_TIMING2 bit[10:0] to enable the auto-refresh command transfer function.

Step 13 Configure the AXI_REGION_MAP register to configure the DDR address area mapping.

Step 14 Configure the AXI_REGION_ATTRIB register to configure the DDR address area attribute.

----End

After the preceding steps are complete, the DDR3 DRAM works properly.

NOTE

The register values may vary according to the DDR type, but the procedure is the same.

4.1.5 AXI Registers of the DDRC

4.1.5.1 Register Summary

Table 4-5 describes AXI registers.

Table 4-5 Summary of AXI registers (base address: 0x1211_0000)

Offset Address	Register	Description	Page
0x004	AXI_CFG_LOCK	Lock control register	4-13
0x008	AXI_CKG	Module clock gating register	4-13
0x020	AXI_ACTION	AXI operating mode register	4-14
0x100 + 0x10 x *regions*	AXI_REGION_MAP	Address area mapping register	4-15
0x104 + 0x10 x *regions*	AXI_REGION_ATTRIB	Address area attribute register	4-17

Offset Address	Register	Description	Page
0x108 + 0x10 x *regions*	AXI_REGION_SCRMBL	Address scrambling code mode register for address areas	4-19
0x200 + 0x10 x *ports*	AXI_QOS_MAP	Command priority mapping mode register	4-20
0x204 + 0x10 x *ports*	AXI_QOS_WRPRIn	Write command priority mapping table register	4-22
0x208 + 0x10 x *ports*	AXI_QOS_RDPRIn	Read command priority mapping table register	4-24
0x20C + 0x10 x *ports*	AXI_QOS_ADPTn	Priority adaptation cycle mapping table register	4-25
0x300 + 0x10 x *ports*	AXI_OSTD_PRTn	Port command outstanding (OSTD) restriction register	4-27
0x304 + 0x10 x *ports*	AXI_OSTD_PRT_STn	Port command OSTD statistics register0}	4-27
0x400 + 0x10 x *groups*	AXI_OSTD_GROUPn	Command OSTD register for the port group	4-27
0x404 + 0x10 x *groups*	AXI_OSTD_PRIn0	Priority-based port group command OSTD restriction register 0	4-28
0x408 + 0x10 x *groups*	AXI_OSTD_PRIn1	Priority-based port group command OSTD restriction register 1	4-30
0x40C + 0x10 x *groups*	AXI_OSTD_GROUP_STn	Command OSTD statistics register for the port group	4-31
0x500 + 0x10 x *ports*	AXI_PUSH_WRMIDn	Priority deliver enable register for write commands with the same MIDs	4-32
0x504 + 0x10 x *ports*	AXI_PUSH_RDMIDn	Priority deliver enable register for read commands with the same MIDs	4-32
0x600	AXI_STATUS	Port operating mode register	4-33
0x610	AXI_INT_STATUS	Interrupt status register	4-33

Table 4-6 describes the value ranges and meanings of variables in the offset addresses for AXI registers.

Table 4-6 Variables in the offset addresses for AXI registers

Variable	Value Range	Description
regions	0−8	Number of address areas
ports	0−5	Number of AXI ports

Variable	Value Range	Description
groups	0–4	Number of groups for the port command OSTD statistics

4.1.5.2 Register Description

AXI_CFG_LOCK

AXI_CFG_LOCK is a lock control register.

Offset Address	Register Name	Total Reset Value
0x004	AXI_CFG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															apb_cfg_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	apb_cfg_lock	Lock control of all the register configuration modules (AXI_IF/SEC/DMC/PUB) in the MDDRC 0: unlocked 1: locked (None of the AXI_IF configuration registers can be accessed except this register. Therefore, the power consumption is reduced.)

AXI_CKG

AXI_CKG is a module clock gating register.

Offset Address	Register Name	Total Reset Value
0x008	AXI_CKG	0x000F_1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												sta_ckg_dmc				reserved			dyn_ckg_rdr	dyn_ckg_axi											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RW	sta_ckg_dmc	Static clock gating for each DMC When sta_ckg_dmc[n] is 0, the clocks for the DMC*n* and the corresponding PHY utility block (PUB) are disabled. When sta_ckg_dmc[n] is 1, the clocks for the DMC*n* and the corresponding PUB are enabled. *n* = 1, 2 or 3: reserved
[15:13]	RO	reserved	Reserved
[12]	RW	dyn_ckg_rdr	Dynamic clock gating for the reorder module 0: The clock is always enabled. 1: The clock is automatically disabled when the module is idle.
[11:0]	RW	dyn_ckg_axi	Dynamic clock gating for each AXI port When dyn_ckg_axi[n] is 0, the clock for AXI port *n* is always enabled. When dyn_ckg_axi[n] is 1, the clock is automatically disabled when modules in AXI port *n* are idle. Notes: *n*= 6, 7, 8, 9, 10 or 11: reserved

AXI_ACTION

AXI_ACTION is an AXI operating mode register.

Offset Address	Register Name	Total Reset Value
0x020	AXI_ACTION	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												wr_rcv_mode												reserved						rd_wrap_split_en	exclusive_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:8]	RW	wr_rcv_mode	Anti-deadlock mode enable When wr_rcv_mode[n] is 0, the anti-deadlock mode for port *n* is disabled. When wr_rcv_mode[n] is 1, the anti-deadlock mode for port *n* is enabled. NOTE • Whether to enable the anti-deadlock mode depends on bus architecture requirements • When the anti-deadlock mode is enabled, the OSTD of the write command is restricted to 1.
[7:2]	RO	reserved	Reserved
[1]	RW	rd_wrap_split_en	Wrap read command split enable 0: no split. The address is wrapped by the DMC. 1: split
[0]	RW	exclusive_en	Exclusive command enable 0: disabled 1: enabled

AXI_REGION_MAP

AXI_REGION_MAP is an address area mapping register.

Offset Address	Register Name	Total Reset Value
0x100 + 0x10 x regions (regions = 0−15)	AXI_REGION_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			rgn_en	reserved		rgn_size		rgn_base_addr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	rgn_en	Current address area enable 0: disabled 1: enabled
[11]	RO	reserved	Reserved
[10:8]	RW	rgn_size	Size of the current address area 0x0: 16 MB 0x1: 32 MB. In this case, rgn_base_addr/ch_offset[0] must be set to 0. 0x2: 64 MB. In this case, rgn_base_addr/ch_offset[1:0] must be set to 0. 0x3: 128 MB. In this case, rgn_base_addr/ ch _offset[2:0] must be set to 0. 0x4: 256 MB. In this case, rgn_base_addr/ ch _offset[3:0] must be set to 0. 0x5: 512 MB. In this case, rgn_base_addr/ ch _offset[4:0] must be set to 0. 0x6: 1 GB. In this case, rgn_base_addr/ ch _offset[5:0] must be set to 0. 0x7: 2 GB. In this case, rgn_base_addr/ ch _offset[6:0] must be set to 0. **NOTE** • The preceding configuration is valid when the address bit width is 32 bits. The meaning of the configured value varies according to the address bit width. For example, when the address bit width is 40 bits, if this field is set to 0x3, the size of the current address area is 32 GB. In this case, rgn_base_addr[2:0] must be set to 0. • When the address mapping mode is the dual-channel-interleaved mode, rgn_size cannot be set to 0. When the addresses of four channels are interleaved, rgn_size cannot be set to 0 or 1.

[7:0]	RW	rgn_base_addr	Base address of the current address area (upper eight bits) **NOTE** The area address alignment granularity varies according to the address bit width because only the upper eight bits of the address can be configured. • When the address bit width is 32 bits, the lower 24 bits of the base address of the address area are 0 and the area address is 16-MB-aligned. • When the address bit width is 40 bits, the lower 32 bits of the base address of the address area are 0 and the area address is 4-GB-aligned. Only the 32-bit address bit width is supported in this version.

AXI_REGION_ATTRIB

AXI_REGION_ATTRIB is an address area attribute register.

Offset Address	Register Name	Total Reset Value
0x104 + 0x10 x regions (regions = 0−15)	AXI_REGION_ATTRIB	0x0001_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		bnk_mod			reserved		rnk_mod		reserved				addr_aligned				ch_offset								reserved			ch_intlv		ch_mode		ch_start	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	bnk_mod	Bank interleaving granularity in the channel of the current address area (the interleaving granularity varies according to the component) 8Byte*2^n (8-bit components); 16Byte*2^n (16-bit components); 32Byte*2^n (32-bit components); 64Byte*2^n (64-bit components). n=0−7 **NOTE** The bank interleaving granularity must be greater than or equal to the address alignment granularity (addr_aligned).
[27:26]	RO	reserved	Reserved

[25:24]	RW	rnk_mod	Rank interleaving mode of the channel of the current address area 00: The configuration in the DMC is used. 01: a single independent rank address 10: Two rank addresses are interleaved. 11: Four rank addresses are interleaved. Only a single channel is supported in this version and the channel supports only one rank.
[23:19]	RO	reserved	Reserved
[18:16]	RW	addr_aligned	Address boundary alignment granularity of the current address area 000: 8 bytes (valid only when the DMC data bit width is 64 bits) 001: 16 bytes 010: 32 bytes 011: 64 bytes 100: 128 bytes 101: 256 bytes 110: 512 bytes 111: 1 KB NOTE • Commands that cross the address alignment boundary will be split. • The address alignment granularity must be less than or equal to the bank interleaving granularity (bnk_mod). • When addresses are interleaved, the address alignment granularity must be less than or equal to the address interleaving granularity (ch_intlv). • When the address is independent, the address alignment granularity must be less than or equal to the page size of the DDR.
[15:8]	RW	ch_offset	Offset address of the current address area in the channel (upper eight bits) NOTE The offset address is used to replace the upper eight bits of the address in the channel to implement the offset of the mapping address in the channel. The offset address varies according to the address bit width. • Bits [31:24] of the 32-bit address after channel mapping can be replaced. • Bits [39:32] of the 40-bit address after channel mapping can be replaced. Only the 32-bit address bit width is supported in this version.
[7:6]	RO	reserved	Reserved

[5:4]	RW	ch_intlv	Address interleaving granularity of the current address area (invalid in single independent channel address mode) 0x0: 64 Byte 0x1: 128 bytes 0x2: 256 bytes 0x3: 512 bytes **NOTE** • Commands are alternately sent to multiple channels based on this granularity. • When channels are interleaved, the address interleaving granularity must be greater than or equal to the address alignment granularity (addr_aligned).
[3:2]	RW	ch_mode	Channel mapping mode of the current address area 00: no mapping 01: The address of a single channel is mapped to the channel, and the address is independent 10: The addresses of two channels are mapped to the channel, and the addresses are interleaved. 11: The addresses of four channels are mapped to the channel, and the addresses are interleaved. **NOTE** • Commands that attempt to access the unmapped address areas are processed as incorrect commands. In this case, interrupts are reported, command information is recorded, and the SLVERR response is returned from the AXI bus. • Only a single channel is supported in this version.
[1:0]	RW	ch_start	Mapping start channel of the current address area 00: channel 0 01: channel 1 10: channel 2 11: channel 3 **NOTE** • In single-channel mapping mode, the mapping start channel can be any channel. • In dual-channel mapping mode, the mapping start channel must be channel 0 (addresses of channel 0 and channel 1 are interleaved) or channel 2 (addresses of channel 2 and channel 3 are interleaved). • In quad-channel mapping mode, the mapping start channel must be channel 0 (addresses of channels 0−3 are interleaved). • Only a single channel is supported in this version.

AXI_REGION_SCRMBL

AXI_REGION_SCRMBL is an address scrambling code mode register for address areas.

Offset Address	Register Name	Total Reset Value
0x108 + 0x10 x regions (regions = 0–15)	AXI_REGION_SCRMBL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												bnk_scrmbl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved. This field is fixed at 0.
[3:0]	RW	bnk_scrmbl	Bank address scrambling code mode 0: no scrambling code 1: addr[14:12] = addr[14:12] XOR addr[17:15] 2: addr[14:12] = addr[14:12] XOR addr[18:16] 3: addr[14:12] = addr[14:12] XOR addr[19:17] 4: addr[14:12] = addr[14:12] XOR addr[20:18] 5: addr[14:12] = addr[14:12] XOR addr[21:19] 6: addr[14:12] = addr[14:12] XOR addr[22:20] 7: addr[14:12] = addr[14:12] XOR addr[23:21] Other values: reserved **NOTE** addr indicates the bus address.

AXI_QOS_MAP

AXI_QOS_MAP is a command priority mapping mode register.

Offset Address	Register Name	Total Reset Value
0x200 + 0x10 x ports (ports = 0–8)	AXI_QOS_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										qos_rever	rw_arb_mode	reserved	hurry_qos_en	push_qos_en	pri_push_en	reserved				pri_map_mode				id_map_idx							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved

[21]	RW	qos_rever	QoS inversion enable (for the priority arbitration of the read and write commands from the same port) 0: Priority 0 (axqos = 0) is the lowest priority. 1: Priority 0 (axqos = 0) is the highest priority. **NOTE** This register is valid only when rw_arb_mode is 1.
[20]	RW	rw_arb_mode	Arbitration mode for the read and write commands from the same port 0: The arbitration is based on the command read/write type. • The command that arrives first is arbitrated first. • When the read and write commands arrive simultaneously (or the back pressure is imposed on them simultaneously), the read command is arbitrated before the write command. 1: The arbitration is based on the command priority. • The command that arrives first is arbitrated first. • When the read and write commands arrive simultaneously (or the back pressure is imposed on them simultaneously), the command with a higher priority is arbitrated first. • If the priorities of the read and write commands are the same, the command that is not arbitrated last time is arbitrated according to the least recently used (LRU) rule.
[19]	RO	reserved	Reserved
[18]	RW	hurry_qos_en	Hurry priority deliver enable 0: disabled 1: enabled **NOTE** • The hurry signal on the NOC bus can deliver priorities at any time and is involved in the priority deliver in the AXI_IF. • This register is valid only when pri_push_en is 1.
[17]	RW	push_qos_en	Push priority deliver enable 0: disabled 1: enabled **NOTE** • The pressure signal on the NOC bus can deliver priorities when the back pressure is imposed on the command bus and is involved in the priority deliver in the AXI_IF. • This register is valid only when pri_push_en is 1.

[16]	RW	pri_push_en	Port priority deliver enable 0: disabled 1: enabled **NOTE** When the port priority deliver function is enabled, among the multiple commands in the port pipeline and external commands, the one with the highest priority is transferred to the command that is involved in port arbitration. This enables the command to be arbitrated instantly. However, the priority of the transferred command remains unchanged.
[15:13]	RO	reserved	Reserved
[12]	RW	pri_map_mode	Priority mapping mode of the read/write command 0: Any three bits in the command ID or associated signal are used as the mapping index. 1: Any three bits in the lower 16 bits of the command ID are used as the mapping index. **NOTE** The mapping index is obtained by using either of the preceding methods, and the command priority is obtained by mapping the index to the priority lookup table. The lookup table indicates the description of AXI_QOS_WRPRI or AXI_QOS_RDPRI.
[11:0]	RW	id_map_idx	Three methods for selecting bits in the command ID as the mapping index when the command ID is used to map the priority id_map_idx[11:8]: Any one bit in the lower 16 bits of the command ID is selected as idx[2]. id_map_idx[7:4]: Any one bit in the lower 16 bits of the command ID is selected as idx[1]. id_map_idx[3:0]: Any one bit in the lower 16 bits of the command ID is selected as idx[0]. For example, if id_map_idx is set to 0x3A0, ID[3], ID[10], and ID[0] of the command form idx[2:0], which is used to map the command priority from the priority lookup table. The lookup table indicates the description of AXI_QOS_WRPRI or AXI_QOS_RDPRI. **NOTE** The command ID indicates the original command ID.

AXI_QOS_WRPRIn

AXI_QOS_WRPRIn is a write command priority mapping table register.

Offset Address	Register Name	Total Reset Value
0x204 + 0x10 x ports (ports = 0−8)	AXI_QOS_WRPRIn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	wr_pri7			reserved	wr_pri6			reserved	wr_pri5			reserved	wr_pri4			reserved	wr_pri3			reserved	wr_pri2			reserved	wr_pri1			reserved	wr_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	wr_pri7	Priority of the write command when the mapping index is 7 0x0: highest priority … 0x7: lowest priority
[27]	RO	reserved	Reserved
[26:24]	RW	wr_pri6	Priority of the write command when the mapping index is 6 0x0: highest priority … 0x7: lowest priority
[23]	RO	reserved	Reserved
[22:20]	RW	wr_pri5	Priority of the write command when the mapping index is 5 0x0: highest priority … 0x7: lowest priority
[19]	RO	reserved	Reserved
[18:16]	RW	wr_pri4	Priority of the write command when the mapping index is 4 0x0: highest priority … 0x7: lowest priority
[15]	RO	reserved	Reserved
[14:12]	RW	wr_pri3	Priority of the write command when the mapping index is 3 0x0: highest priority … 0x7: lowest priority
[11]	RO	reserved	Reserved

[10:8]	RW	wr_pri2	Priority of the write command when the mapping index is 2 0x0: highest priority … 0x7: lowest priority
[7]	RO	reserved	Reserved
[6:4]	RW	wr_pri1	Priority of the write command when the mapping index is 1 0x0: highest priority … 0x7: lowest priority
[3]	RO	reserved	Reserved
[2:0]	RW	wr_pri0	Priority of the write command when the mapping index is 0 0x0: highest priority … 0x7: lowest priority

AXI_QOS_RDPRIn

AXI_QOS_RDPRIn is a read command priority mapping table register.

Offset Address	Register Name	Total Reset Value
0x208 + 0x10 x ports (ports = 0–8)	AXI_QOS_RDPRIn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rd_pri7			reserved	rd_pri6			reserved	rd_pri5			reserved	rd_pri4			reserved	rd_pri3			reserved	rd_pri2			reserved	rd_pri1			reserved	rd_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	rd_pri7	Same as rd_pri0
[27]	RO	reserved	Reserved
[26:24]	RW	rd_pri6	Same as rd_pri0
[23]	RO	reserved	Reserved
[22:20]	RW	rd_pri5	Same as rd_pri0
[19]	RO	reserved	Reserved
[18:16]	RW	rd_pri4	Same as rd_pri0

[15]	RO	reserved	Reserved
[14:12]	RW	rd_pri3	Same as rd_pri0
[11]	RO	reserved	Reserved
[10:8]	RW	rd_pri2	Same as rd_pri0
[7]	RO	reserved	Reserved
[6:4]	RW	rd_pri1	Same as rd_pri0
[3]	RO	reserved	Reserved
[2:0]	RW	rd_pri0	Priority of the read command when the mapping index is 0 0x0: highest priority … 0x7: lowest priority

AXI_QOS_ADPTn

AXI_QOS_ADPTn is a priority adaptation cycle mapping table register.

Offset Address	Register Name	Total Reset Value
0x20C + 0x10 x ports (ports = 0−8)	AXI_QOS_ADPTn	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23	22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6 5 4	3 2 1 0
Name	reserved	wr_adpt_high	reserved	wr_adpt_lvl	wr_adpt_low	reserved	rd_adpt_high	reserved	rd_adpt_lvl	rd_adpt_low
Reset	0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	wr_adpt_high	Write command priority adaptation cycle (high-level) 0x0: The priority adaptation function is disabled. 0x1−0xF: (*n* x 16) clock cycles **NOTE** The priority of a command is automatically increased by one level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one.
[23]	RO	reserved	Reserved

[22:20]	RW	wr_adpt_lvl	Write command priority adaptation cycle threshold 0x0−0x1: reserved 0x2−0x7: When the priority of a command is greater than or equal to the threshold, the command is mapped to the high-level cycle. Otherwise, the command is mapped to the low-level cycle. For example: 0x5: The priority adaptation cycle of write commands with priorities 2−5 is configured in wr_adpt_high, and that of write commands with priorities 6−7 is configured in wr_adpt_low.
[19:16]	RW	wr_adpt_low	Write command priority adaptation cycle (low-level) 0x0: The priority adaptation function is disabled. 0x1−0xF: (*n* x 16) clock cycles **NOTE** The priority of a command is automatically increased by one level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one.
[15:12]	RO	reserved	Reserved
[11:8]	RW	rd_adpt_high	Read command priority adaptation cycle (high-level) 0x0: The priority adaptation function is disabled. 0x1−0xF: (*n* x 16) clock cycles **NOTE** The priority of a command is automatically increased by one level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one.
[7]	RO	reserved	Reserved
[6:4]	RW	rd_adpt_lvl	Read command priority adaptation cycle threshold 0x0−0x1: reserved 0x2−0x7: When the priority of a command is greater than or equal to the threshold, the command is mapped to the high-level cycle. Otherwise, the command is mapped to the low-level cycle. For example: 0x5: The priority adaptation cycle of read commands with priorities 2−5 is configured in rd_adpt_high, and that of read commands with priorities 6−7 is configured in rd_adpt_low.
[3:0]	RW	rd_adpt_low	Read command priority adaptation cycle (low-level) 0x0: The priority adaptation function is disabled. 0x1−0xF: (*n* x 16) clock cycles **NOTE** The priority of a command is automatically increased by one level each time it reaches a priority adaptation cycle, until the priority becomes the second highest one.

AXI_OSTD_PRTn

AXI_OSTD_PRTn is a port command OSTD restriction register.

Offset Address	Register Name	Total Reset Value
0x300 + 0x10 x ports (ports = 0−8)	AXI_OSTD_PRTn	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							prt_ostd_lvl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:0]	RW	prt_ostd_lvl	Command OSTD threshold of a port 0x00: The number of command OSTDs of a port is not limited. 0x01−0x7F: maximum number of command OSTDs allowed by the port **NOTE** • In this document, the number of OSTDs is the number of commands in the back-end module QoSBuf. • In this document, the threshold cannot be greater than the command queue depth of the QoSBuf that is specified by setting parameters.

AXI_OSTD_PRT_STn

AXI_OSTD_PRT_STn is a port command OSTD statistics register.

Offset Address	Register Name	Total Reset Value
0x304 + 0x10 x ports (ports = 0−8)	AXI_OSTD_PRT_STn	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							prt_ostd_st
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:0]	RO	prt_ostd_st	Command OSTD statistics of a port

AXI_OSTD_GROUPn

AXI_OSTD_GROUPn is a command OSTD register for the port group.

Offset Address	Register Name	Total Reset Value
0x400 + 0x10 x groups (groups = 0–3)	AXI_OSTD_GROUPn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				group_ostd_sel												reserved								group_ostd_lvl							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	group_ostd_sel	Port select of a group When group_ostd_sel[n] is 0, port *n* is not selected. When group_ostd_sel[n] is 1, port *n* is selected. **NOTE** Only the selected ports are involved in the OSTD statistics of the port group.
[15:7]	RO	reserved	Reserved
[6:0]	RW	group_ostd_lvl	Command OSTD threshold of a port group 0x00: The number of command OSTDs of the port group is not limited. 0x01–0x7F: maximum number of accumulated command OSTDs allowed by the port group **NOTE** • The number of the command OSTDs of a port group is the sum of the command OSTDs of all the ports selected by the port group. • When the number of command OSTDs exceeds the threshold, all the ports in the port group are blocked.

AXI_OSTD_PRIn0

AXI_OSTD_PRIn0 is priority-based port group command OSTD restriction register 0.

Offset Address	Register Name	Total Reset Value
0x404 + 0x10 x groups (groups = 0−3)	AXI_OSTD_PRIn0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				pri3_ostd_lvl				reserved				pri2_ostd_lvl				reserved				pri1_ostd_lvl				reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:24]	RW	pri3_ostd_lvl	Priority 3 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[23]	RO	reserved	Reserved
[22:16]	RW	pri2_ostd_lvl	Priority 2 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[15]	RO	reserved	Reserved

[14:8]	RW	pri1_ostd_lvl	Priority 1 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[7:0]	RO	reserved	Reserved

AXI_OSTD_PRIn1

AXI_OSTD_PRIn1 is priority-based port group command OSTD restriction register 1.

Offset Address	Register Name	Total Reset Value
0x408 + 0x10 x groups (groups = 0−3)	AXI_OSTD_PRIn1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	pri7_ostd_lvl							reserved	pri6_ostd_lvl							reserved	pri5_ostd_lvl							reserved	pri4_ostd_lvl						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:24]	RW	pri7_ostd_lvl	Priority 7 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. **NOTE** • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[23]	RO	reserved	Reserved

[22:16]	RW	pri6_ostd_lvl	Priority 6 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. NOTE • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[15]	RO	reserved	Reserved
[14:8]	RW	pri5_ostd_lvl	Priority 5 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. NOTE • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.
[7]	RO	reserved	Reserved
[6:0]	RW	pri4_ostd_lvl	Priority 4 command OSTD threshold 0x00: The number of accumulated command OSTDs of the selected port group is not limited. 0x01−0x7F: When the number of accumulated command OSTDs of the selected port group reaches the threshold, only the commands whose priorities are higher than 1 are allowed. NOTE • The command OSTD statistics and restriction are based on the port group. • If the priority deliver function is enabled, the commands with low priorities may not be blocked because their priorities are increased.

AXI_OSTD_GROUP_STn

AXI_OSTD_GROUP_STn is a command OSTD statistics register for the port group.

Offset Address	Register Name	Total Reset Value
0x40C + 0x10 x groups (groups = 0–3)	AXI_OSTD_GROUP_STn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								group_ostd_st							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:0]	RO	group_ostd_st	Command OSTD statistics of a port group

AXI_PUSH_WRMIDn

AXI_PUSH_WRMIDn is a priority deliver enable register for write commands with the same MIDs.

Offset Address	Register Name	Total Reset Value
0x500 + 0x10 x ports (ports = 0–8)	AXI_PUSH_WRMIDn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_mid_sel																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wr_mid_sel	Bit match select of the write command MID (the lowest five bits) When wr_mid_sel[n] is 0, the priority deliver function is disabled for write commands with MID *n* in the QoSBuf. When wr_mid_sel[n] is 1, the priority deliver function is enabled for write commands with MID *n* in the QoSBuf.

AXI_PUSH_RDMIDn

AXI_PUSH_RDMIDn is a priority deliver enable register for read commands with the same MIDs.

Offset Address	Register Name	Total Reset Value
0x504 + 0x10 x ports (ports = 0−8)	AXI_PUSH_RDMIDn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_mid_sel																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rd_mid_sel	Bit match select of the read command MID (the lowest five bits) When rd_mid_sel[n] is 0, the priority deliver function is disabled for read commands with MID *n* in the QoSBuf. When rd_mid_sel[n] is 1, the priority deliver function is enabled for read commands with MID *n* in the QoSBuf.

AXI_STATUS

AXI_STATUS is a port operating mode register.

Offset Address	Register Name	Total Reset Value
0x600	AXI_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				axi_if_busy											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	axi_if_busy	Operating mode of each AXI port When axi_prt_busy[n] is 0, AXI port *n* is idle. When axi_prt_busy[n] is 1, AXI port *n* is processing commands or data.

AXI_INT_STATUS

AXI_INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x610	AXI_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				int_ports											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	int_ports	Interrupt source indicator When interrupt_ports[n] is 1, the interrupt source is port *n*. NOTE When the command does not pass the security permission check and the interrupt is enabled, the corresponding port generates interrupts.

4.1.6 QOSBUF Registers of the DDRC

4.1.6.1 Register Summary

Table 4-7 describes QoSBuf registers.

Table 4-7 Summary of QoSBuf registers (base address: 0x1211_4000)

Offset Address	Register	Description	Page
0x000	QOSB_PUSH_CTRL	QoSBuf push configuration register	4-38
0x004	QOSB_ADPT_CTRL	QoSBuf adaptation configuration register	4-38
0x008 + 0x4 x fids	QOSB_FLUX_ID	QoSBuf matched ID register for traffic statistics	4-39
0x024 + 0x4 x fids	QOSB_FLUX_ID_MASK	QoSBuf traffic statistics ID mask register	4-39
0x040	QOSB_FLUX_PRD	QoSBuf traffic statistical period register	4-40
0x044 + 0x4 x fgps	QOSB_FLUX_LVL	QoSBuf traffic statistical threshold register	4-40
0x064	QOSB_FLUX_EN	QoSBuf traffic statistics enable register	4-41
0x068 + 0x4 x chans	QOSB_BANK_CTRL	QoSBuf bank rotating control register	4-41
0x078 + 0x4 x chans	QOSB_GREEN_CTRL	QoSBuf green channel control register	4-42

Offset Address	Register	Description	Page
0x088	QOSB_BUF_BYP	QoSBuf bypass control register	4-43
0x08C + 0x4 x chans	QOSB_WBUF_CTRL	QoSBuf write command priority adjustment control register	4-44
0x09C	QOSB_WRTOUT0	QoSBuf write command timeout period register 0	4-45
0x0A0	QOSB_WRTOUT1	QoSBuf write command timeout period register 1	4-45
0x0A4	QOSB_WRTOUT2	QoSBuf write command timeout period register 2	4-46
0x0A8	QOSB_WRTOUT3	QoSBuf write command timeout period register 3	4-46
0x0AC	QOSB_RDTOUT0	QoSBuf read command timeout period register 0	4-47
0x0B0	QOSB_RDTOUT1	QoSBuf read command timeout period register 1	4-47
0x0B4	QOSB_RDTOUT2	QoSBuf read command timeout period register 2	4-48
0x0B8	QOSB_RDTOUT3	QoSBuf read command timeout period register 3	4-49
0x0BC	QOSB_WRTOUT_MAP	QoSBuf write command timeout mapping mode control register	4-49
0x0D0	QOSB_RDTOUT_MAP	QoSBuf read command timeout mapping mode control register	4-50
0x0D4	QOSB_WRAGE0	QoSBuf write command aging configuration register 0	4-51
0x0D8	QOSB_WRAGE1	QoSBuf write command aging configuration register 1	4-51
0x0DC	QOSB_RDAGE0	QoSBuf read command aging configuration register 0	4-52
0x0E0	QOSB_RDAGE1	QoSBuf read command aging configuration register 1	4-53
0x0E4	QOSB_WRAGE_MAP	QoSBuf write command aging mapping mode control register	4-54
0x0E8	QOSB_RDAGE_MAP	QoSBuf read command aging mapping mode control register	4-55
0x0EC	QOSB_ROWHIT_PRILVL	QoSBuf row-hit priority threshold register	4-55

Offset Address	Register	Description	Page
0x0F0	QOSB_ROWHIT_PRI	QoSBuf row-hit priority control register	4-57
0x0F4	QOSB_ROWHIT_CTRL	QoSBuf row-hit enable register	4-57
0x108	QOSB_CKG_CFG	QoSBuf clock control register	4-59
0x10C + 0x4 x chans	QOSB_DMC_LVL	QoSBuf threshold control register for commands that enter the DMC module	4-59
0x120	QOSB_CFG_PERF	QoSBuf performance statistics mode configuration register	4-60
0x124	QOSB_CMD_SUM	QoSBuf accumulated command count register	4-60
0x128	QOSB_SLOT_STAT0	QoSBuf queue status register 0	4-61
0x12C	QOSB_SLOT_STAT1	QoSBuf queue status register 1	4-61
0x130	QOSB_SLOT_STAT2	QoSBuf queue status register 2	4-62
0x134	QOSB_SLOT_STAT3	QoSBuf queue status register 3	4-62
0x140 + 0x4 x chans	QOSB_WBUF_STAT0	QoSBuf write buffer status register 0	4-62
0x150 + 0x4 x chans	QOSB_WBUF_STAT1	QoSBuf write buffer status register 1	4-63
0x160 + 0x4 x chans	QOSB_RDRBUF_STAT	Buffer status register for the Reorder module	4-63
0x170	QOSB_INTMSK	QoSBuf interrupt mask register	4-64
0x174	QOSB_RINT	QoSBuf raw interrupt register	4-64
0x178	QOSB_INTSTS	QoSBuf interrupt status register	4-65
0x180	QOSB_CMD_CNT	QoSBuf command statistics register	4-65
0x190 + 0x4 x chans	QOSB_RNK_CNT	QoSBuf command (in each rank) statistics register	4-66

Offset Address	Register	Description	Page
0x1A0 + 0x4 x chans	QOSB_BNK_CNT0	QoSBuf command (in each bank) statistics register 0	4-66
0x1B0 + 0x4 x chans	QOSB_BNK_CNT1	QoSBuf command (in each bank) statistics register 1	4-67
0x1C0 + 0x4 x chans	QOSB_BNK_CNT2	QoSBuf command (in each bank) statistics register 2	4-67
0x1D0 + 0x4 x chans	QOSB_BNK_CNT3	QoSBuf command (in each bank) statistics register 3	4-68
0x1E0	QOSB_OSTD_CNT	QoSBuf OSTD command (in each channel) statistics register	4-68
0x1E4	QOSB_WR_CMD_SUM	QoSBuf accumulated write command count register	4-68
0x1E8	QOSB_RD_CMD_SUM	QoSBuf accumulated read command count register	4-69
0x1F0	QOSB_TIMEOUT_MODE	QoSBuf timeout mode selection register	4-69
0x1F4	QOSB_WBUF_PRI_CTRL	QoSBuf write buffer priority adjustment control register	4-70
0x1F8	QOSB_RHIT_CTRL	QoSBuf row-hit priority adjustment control register	4-71

Table 4-8 describes the value ranges and meanings of variables in the offset addresses for QoSBuf registers.

Table 4-8 Variables in the offset addresses for QoSBuf registers

Variable	Value Range	Description
chans	0−1	Number of channels
fgps	0−7	Number of groups whose traffic statistics is collected
fids	0−6	Number of matched IDs during traffic statistics

4.1.6.2 Register Description

QOSB_PUSH_CTRL

QOSB_PUSH_CTRL is a QosBuf push configuration register.

Offset Address	Register Name	Total Reset Value
0x000	QOSB_PUSH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													mid_push_en	addr_push_en	id_push_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	mid_push_en	Push enable for commands with the same MID 0: disabled 1: enabled
[1]	RW	addr_push_en	Push enable for commands with the same address 0: disabled 1: enabled
[0]	RW	id_push_en	Push enable for commands with the same ID 0: disabled 1: enabled

QOSB_ADPT_CTRL

QOSB_ADPT_CTRL is a QoSBuf adaptation configuration register.

Offset Address	Register Name	Total Reset Value
0x004	QOSB_ADPT_CTRL	0x0000_0FF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												adpt_share_cnt																reserved			adpt_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:4]	RW	adpt_share_cnt	Adapt counter for lower bits. When the value of this counter decreases to 0, the counter for upper bits corresponding to each CMD decreases by 1.
[3:1]	RO	reserved	Reserved
[0]	RW	adpt_en	Adapt enable 0: disabled 1: enabled

QOSB_FLUX_ID

QOSB_FLUX_ID is a QoSBuf matched ID register for traffic statistics.

Offset Address	Register Name	Total Reset Value
0x008 + 0x4 x fids (fids = 0–6)	QOSB_FLUX_ID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_id																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flux_id	Matched ID for traffic statistics. The ID ranges from 0 to 6, and each ID corresponds to a statistics group. If the traffic ID matches none of the seven IDs, the traffic is included in the default group.

QOSB_FLUX_ID_MASK

QOSB_FLUX_ID_MASK is a QoSBuf traffic statistics ID mask register.

Offset Address	Register Name	Total Reset Value
0x024 + 0x4 x fids (fids = 0–6)	QOSB_FLUX_ID_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_id_mask																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flux_id_mask	QoSBuf traffic statistics ID mask, corresponding to QOSB_FLUX_ID 0: Bits of the corresponding ID are ignored. 1: Bits of the corresponding ID are compared.

QOSB_FLUX_PRD

QOSB_FLUX_PRD is a QoSBuf traffic statistical period register.

Offset Address	Register Name	Total Reset Value
0x040	QOSB_FLUX_PRD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																flux_prd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	flux_prd	Traffic statistical period

QOSB_FLUX_LVL

QOSB_FLUX_LVL is a QoSBuf traffic statistical threshold register.

Offset Address	Register Name	Total Reset Value
0x044 + 0x4 x fgps (fgps = 0–7)	QOSB_FLUX_LVL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flux_lvl																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	flux_lvl	Traffic statistical threshold. During the statistical period, the priority of the command is decreased to the lowest one when the traffic exceeds the threshold.

QOSB_FLUX_EN

QOSB_FLUX_EN is a QoSBuf traffic statistics enable register.

Offset Address	Register Name	Total Reset Value
0x064	QOSB_FLUX_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															flux_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	flux_en	Traffic statistics enable 0: disabled 1: enabled

QOSB_BANK_CTRL

QOSB_BANK_CTRL is a QoSBuf bank rotating control register.

Offset Address	Register Name	Total Reset Value
0x068 + 0x4 x chans (chans = 0−1)	QOSB_BANK_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved						ba_cnt_lvl	reserved	ba_intleav_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	ba_cnt_lvl	Bank conflict threshold. When the number of commands with the same bank address exceeds the threshold, bank conflict occurs. Otherwise, there is no bank conflict.
[3:1]	RO	reserved	Reserved
[0]	RW	ba_intleav_en	QoSBuf bank rotating enable 0: disabled 1: enabled

QOSB_GREEN_CTRL

QOSB_GREEN_CTRL is a QoSBuf green channel control register.

Offset Address	Register Name	Total Reset Value
0x078 + 0x4 x chans (chans = 0−1)	QOSB_GREEN_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved						green_lvl	reserved	green_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

[7:4]	RW	green_lvl	Green channel threshold. That is, the empty locations above this threshold are reserved for green channels. For example, if there are 12 DMC queues (queues 0−11) and the threshold is 9, queues 10 and 11 are reserved for green channels. NOTE • When this field is set to N, the actual number of allowed commands is (N + 1) because of the pipeline issue. • This register cannot be dynamically configured when it is being accessed.
[3:1]	RO	reserved	Reserved
[0]	RW	green_en	Green channel enable (channels are not controlled separately, which needs to be optimized later) 0: disabled 1: enabled

QOSB_BUF_BYP

QOSB_BUF_BYP is a QoSBuf bypass control register.

Offset Address	Register Name	Total Reset Value
0x088	QOSB_BUF_BYP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							qos_buf_byp
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	qos_buf_byp	QoSBuf bypass control x0: forcible non-bypass mode. That is, all the commands enter the QoSBuf module when the value is set to 00 or 10. 01: whether to bypass depends on the queue status in the DMC 11: forcible bypass mode. None of the commands enters the QoSBuf module. NOTE These modes need to be configured before the access. The dynamic configuration is forbidden during the access.

QOSB_WBUF_CTRL

QOSB_WBUF_CTRL is a QoSBuf write command priority adjustment control register.

Offset Address	Register Name	Total Reset Value
0x08C + 0x4 x chans (chans = 0−1)	QOSB_WBUF_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbuf_ptun_en	wbuf_pri2			wbuf_lvl2								reserved	wbuf_pri1			wbuf_lvl1								wbuf_lvl0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wbuf_ptun_en	Write command priority adjustment enable 0: disabled 1: enabled
[30:28]	RW	wbuf_pri2	Priority of write buffer threshold 2
[27:20]	RW	wbuf_lvl2	Write buffer threshold 2. When the number of commands increasingly reaches the threshold, if the priorities of the write commands are lower than wbuf_pri2, the priorities of the write commands are set to wbuf_pri2. If the priorities of the write commands are higher than wbuf_pri2, the priorities of the write commands are restored to their previous priorities. Note that the threshold cannot be dynamically configured. Otherwise, the write buffer adaptation function becomes invalid.
[19]	RO	reserved	Reserved
[18:16]	RW	wbuf_pri1	Priority of write buffer threshold 1 priority
[15:8]	RW	wbuf_lvl1	Write buffer threshold 1. When the number of commands increasingly or decreasingly reaches the threshold, if the priorities of the write commands are lower than wbuf_pri1, the priorities of the write commands are set to wbuf_pri1. If the priorities of the write commands are higher than wbuf_pri1, the priorities of the write commands are restored to their previous priorities. Note that the threshold cannot be dynamically configured. Otherwise, the write buffer adaptation function becomes invalid.
[7:0]	RW	wbuf_lvl0	Write buffer threshold 0. When the number of commands decreasingly reaches the threshold, the priorities of the write commands are decreased to the lowest priority. Note that the threshold cannot be dynamically configured. Otherwise, the write buffer adaptation function becomes invalid.

QOSB_WRTOUT0

QOSB_WRTOUT0 is QoSBuf write command timeout period register 0.

Offset Address	Register Name	Total Reset Value
0x09C	QOSB_WRTOUT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_tout3								wr_tout2								wr_tout1								wr_tout0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	wr_tout3	Write command timeout period (level 3) The configuration mode is the same as that of wr_tout0.
[23:16]	RW	wr_tout2	Write command timeout period (level 2) The configuration mode is the same as that of wr_tout0.
[15:8]	RW	wr_tout1	Write command timeout period (level 1) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout0	Write command timeout period (level 0) 0x0: The timeout function is disabled. 0x1−0xFF: *n* x 4 clock cycles **NOTE** When the timeout period is set to 8 bits, the actual count value is 10 bits. That is, the lower two bits are fixed at 0.

QOSB_WRTOUT1

QOSB_WRTOUT1 is QoSBuf write command timeout period register 1.

Offset Address	Register Name	Total Reset Value
0x0A0	QOSB_WRTOUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_tout7								wr_tout6								wr_tout5								wr_tout4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	wr_tout7	Write command timeout period (level 7) The configuration mode is the same as that of wr_tout0.
[23:16]	RW	wr_tout6	Write command timeout period (level 6) The configuration mode is the same as that of wr_tout0.

[15:8]	RW	wr_tout5	Write command timeout period (level 5) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout4	Write command timeout period (level 4) The configuration mode is the same as that of wr_tout0.

QOSB_WRTOUT2

QOSB_WRTOUT2 is QoSBuf write command timeout period register 2.

Offset Address	Register Name	Total Reset Value
0x0A4	QOSB_WRTOUT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_tout11								wr_tout10								wr_tout9								wr_tout8							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	wr_tout11	Write command timeout period (level 11) The configuration mode is the same as that of wr_tout0.
[23:16]	RW	wr_tout10	Write command timeout period (level 10) The configuration mode is the same as that of wr_tout0.
[15:8]	RW	wr_tout9	Write command timeout period (level 9) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout8	Write command timeout period (level 8) The configuration mode is the same as that of wr_tout0.

QOSB_WRTOUT3

QOSB_WRTOUT3 is QoSBuf write command timeout period register 3.

Offset Address	Register Name	Total Reset Value
0x0A8	QOSB_WRTOUT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wr_tout15								wr_tout14								wr_tout13								wr_tout12							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	wr_tout15	Write command timeout period (level 15) The configuration mode is the same as that of wr_tout0.

[23:16]	RW	wr_tout14	Write command timeout period (level 14) The configuration mode is the same as that of wr_tout0.
[15:8]	RW	wr_tout13	Write command timeout period (level 13) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout12	Write command timeout period (level 12) The configuration mode is the same as that of wr_tout0.

QOSB_RDTOUT0

QOSB_RDTOUT0 is QoSBuf read command timeout period register 0.

Offset Address	Register Name	Total Reset Value
0x0AC	QOSB_RDTOUT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_tout3								rd_tout2								rd_tout1								rd_tout0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rd_tout3	Read command timeout period (level 3) The configuration mode is the same as that of rd_tout0.
[23:16]	RW	rd_tout2	Read command timeout period (level 2) The configuration mode is the same as that of rd_tout0.
[15:8]	RW	rd_tout1	Read command timeout period (level 1) The configuration mode is the same as that of rd_tout0.
[7:0]	RW	rd_tout0	Read command timeout period (level 0) 0x0: The timeout function is disabled. 0x1−0xFF: *n* x 4 clock cycles **NOTE** When the timeout period is set to 8 bits, the actual count value is 10 bits. That is, the lower two bits are fixed at 0.

QOSB_RDTOUT1

QOSB_RDTOUT1 is QoSBuf read command timeout period register 1.

Offset Address	Register Name	Total Reset Value
0x0B0	QOSB_RDTOUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_tout7								rd_tout6								rd_tout5								rd_tout4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rd_tout7	Read command timeout period (level 7) The configuration mode is the same as that of rd_tout0.
[23:16]	RW	rd_tout6	Read command timeout period (level 6) The configuration mode is the same as that of rd_tout0.
[15:8]	RW	rd_tout5	Read command timeout period (level 5) The configuration mode is the same as that of rd_tout0.
[7:0]	RW	rd_tout4	Read command timeout period (level 4) The configuration mode is the same as that of rd_tout0.

QOSB_RDTOUT2

QOSB_RDTOUT2 is QoSBuf read command timeout period register 2.

Offset Address	Register Name	Total Reset Value
0x0B4	QOSB_RDTOUT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_tout11								rd_tout10								rd_tout9								rd_tout8							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rd_tout11	Read command timeout period (level 11) The configuration mode is the same as that of rd_tout0.
[23:16]	RW	rd_tout10	Read command timeout period (level 10) The configuration mode is the same as that of rd_tout0.
[15:8]	RW	rd_tout9	Read command timeout period (level 9) The configuration mode is the same as that of rd_tout0.
[7:0]	RW	rd_tout8	Read command timeout period (level 8) The configuration mode is the same as that of rd_tout0.

QOSB_RDTOUT3

QOSB_RDTOUT3 is QoSBuf read command timeout period register 3.

Offset Address	Register Name	Total Reset Value
0x0B8	QOSB_RDTOUT3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rd_tout15		rd_tout14		rd_tout13		rd_tout12	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	rd_tout15	Read command timeout period (level 15) The configuration mode is the same as that ofrd_tout0.
[23:16]	RW	rd_tout14	Read command timeout period (level 14) The configuration mode is the same as that ofrd_tout0.
[15:8]	RW	rd_tout13	Read command timeout period (level 13) The configuration mode is the same as that ofrd_tout0.
[7:0]	RW	rd_tout12	Read command timeout period (level 12) The configuration mode is the same as that ofrd_tout0.

QOSB_WRTOUT_MAP

QOSB_WRTOUT_MAP is a QoSBuf write command timeout mapping mode control register.

Offset Address	Register Name	Total Reset Value
0x0BC	QOSB_WRTOUT_MAP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	wrtout_map3	reserved	wrtout_map2	reserved	wrtout_map1	reserved	wrtout_map0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	wrtout_map3	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. wrtout_map3 indicates the position of bit 3 in the ID.
[23:21]	RO	reserved	Reserved

[20:16]	RW	wrtout_map2	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. wrtout_map2 indicates the position of bit 2 in the ID.
[15:13]	RO	reserved	Reserved
[12:8]	RW	wrtout_map1	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. wrtout_map1 indicates the position of bit 1 in the ID.
[7:5]	RO	reserved	Reserved
[4:0]	RW	wrtout_map0	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. wrtout_map0 indicates the position of bit 0 in the ID.

QOSB_RDTOUT_MAP

QOSB_RDTOUT_MAP is a QoSBuf read command timeout mapping mode control register.

Offset Address	Register Name	Total Reset Value
0x0D0	QOSB_RDTOUT_MAP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	rdtout_map3	reserved	rdtout_map2	reserved	rdtout_map1	reserved	rdtout_map0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	rdtout_map3	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. rdtout_map3 indicates the position of bit 3 in the ID.
[23:21]	RO	reserved	Reserved
[20:16]	RW	rdtout_map2	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. rdtout_map2 indicates the position of bit 2 in the ID.
[15:13]	RO	reserved	Reserved
[12:8]	RW	rdtout_map1	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. rdtout_map1 indicates the position of bit 1 in the ID.
[7:5]	RO	reserved	Reserved

[4:0]	RW	rdtout_map0	There are 16 levels of timeout periods. Four bits are selected from the ID and the level is determined based on the four bits. rdtout_map0 indicates the position of bit 0 in the ID.

QOSB_WRAGE0

QOSB_WRAGE0 is QoSBuf write command aging configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0D4	QOSB_WRAGE0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_age_prd7	wr_age_prd6	wr_age_prd5	wr_age_prd4	wr_age_prd3	wr_age_prd2	wr_age_prd1	wr_age_prd0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	wr_age_prd7	Write command aging cycle (level 7) For details, see wr_age_prd0.
[27:24]	RW	wr_age_prd6	Write command aging cycle (level 6) For details, see wr_age_prd0.
[23:20]	RW	wr_age_prd5	Write command aging cycle (level 5) For details, see wr_age_prd0.
[19:16]	RW	wr_age_prd4	Write command aging cycle (level 4) For details, see wr_age_prd0.
[15:12]	RW	wr_age_prd3	Write command aging cycle (level 3) For details, see wr_age_prd0.
[11:8]	RW	wr_age_prd2	Write command aging cycle (level 2) For details, see wr_age_prd0.
[7:4]	RW	wr_age_prd1	Write command aging cycle (level 1) For details, see wr_age_prd0.
[3:0]	RW	wr_age_prd0	Write command aging cycle (level 0) 0x0: The aging function is disabled. 0x1−0xF: (*n* x 16) clock cycles

QOSB_WRAGE1

QOSB_WRAGE1 is QoSBuf write command aging configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0D8	QOSB_WRAGE1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_age_prd15	wr_age_prd14	wr_age_prd13	wr_age_prd12	wr_age_prd11	wr_age_prd10	wr_age_prd9	wr_age_prd8
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	wr_age_prd15	Write command aging cycle (level 15) For details, see wr_age_prd0.
[27:24]	RW	wr_age_prd14	Write command aging cycle (level 14) For details, see wr_age_prd0.
[23:20]	RW	wr_age_prd13	Write command aging cycle (level 13) For details, see wr_age_prd0.
[19:16]	RW	wr_age_prd12	Write command aging cycle (level 12) For details, see wr_age_prd0.
[15:12]	RW	wr_age_prd11	Write command aging cycle (level 11) For details, see wr_age_prd0.
[11:8]	RW	wr_age_prd10	Write command aging cycle (level 10) For details, see wr_age_prd0.
[7:4]	RW	wr_age_prd9	Write command aging cycle (level 9) For details, see wr_age_prd0.
[3:0]	RW	wr_age_prd8	Write command aging cycle (level 8) For details, see wr_age_prd0.

QOSB_RDAGE0

QOSB_RDAGE0 is QoSBuf read command aging configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0DC	QOSB_RDAGE0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rd_age_prd7	rd_age_prd6	rd_age_prd5	rd_age_prd4	rd_age_prd3	rd_age_prd2	rd_age_prd1	rd_age_prd0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	rd_age_prd7	Read command aging cycle (level 7) For details, see rd_age_prd0.

[27:24]	RW	rd_age_prd6	Read command aging cycle (level 6) For details, see rd_age_prd0.
[23:20]	RW	rd_age_prd5	Read command aging cycle (level 5) For details, see rd_age_prd0.
[19:16]	RW	rd_age_prd4	Read command aging cycle (level 4) For details, see rd_age_prd0.
[15:12]	RW	rd_age_prd3	Read command aging cycle (level 3) For details, see rd_age_prd0.
[11:8]	RW	rd_age_prd2	Read command aging cycle (level 2) For details, see rd_age_prd0.
[7:4]	RW	rd_age_prd1	Read command aging cycle (level 1) For details, see rd_age_prd0.
[3:0]	RW	rd_age_prd0	Read command aging cycle (level 0) 0x0: The aging function is disabled. 0x1−0xF: (*n* x 16) clock cycles

QOSB_RDAGE1

QOSB_RDAGE1 is QoSBuf read command aging configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0E0	QOSB_RDAGE1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rd_age_prd15	rd_age_prd14	rd_age_prd13	rd_age_prd12	rd_age_prd11	rd_age_prd10	rd_age_prd9	rd_age_prd8
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	rd_age_prd15	Read command aging cycle (level 15) For details, see rd_age_prd0.
[27:24]	RW	rd_age_prd14	Read command aging cycle (level 14) For details, see rd_age_prd0.
[23:20]	RW	rd_age_prd13	Read command aging cycle (level 13) For details, see rd_age_prd0.
[19:16]	RW	rd_age_prd12	Read command aging cycle (level 12) For details, see rd_age_prd0.
[15:12]	RW	rd_age_prd11	Read command aging cycle (level 11) For details, see rd_age_prd0.

[11:8]	RW	rd_age_prd10	Read command aging cycle (level 10) For details, see rd_age_prd0.
[7:4]	RW	rd_age_prd9	Read command aging cycle (level 9) For details, see rd_age_prd0.
[3:0]	RW	rd_age_prd8	Read command aging cycle (level 8) For details, see rd_age_prd0.

QOSB_WRAGE_MAP

QOSB_WRAGE_MAP is a QoSBuf write command aging mapping mode control register.

Offset Address	Register Name	Total Reset Value
0x0E4	QOSB_WRAGE_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				wrage_map3				reserved				wrage_map2				reserved				wrage_map1				reserved				wrage_map0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	wrage_map3	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. wrage_map3 indicates the position of bit 3 in the ID.
[23:21]	RO	reserved	Reserved
[20:16]	RW	wrage_map2	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. wrage_map2 indicates the position of bit 2 in the ID.
[15:13]	RO	reserved	Reserved
[12:8]	RW	wrage_map1	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. wrage_map1 indicates the position of bit 1 in the ID.
[7:5]	RO	reserved	Reserved
[4:0]	RW	wrage_map0	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. wrage_map0 indicates the position of bit 0 in the ID.

QOSB_RDAGE_MAP

QOSB_RDAGE_MAP is a QoSBuf read command aging mapping mode control register.

Offset Address	Register Name	Total Reset Value
0x0E8	QOSB_RDAGE_MAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rdage_map3				reserved				rdage_map2				reserved				rdage_map1				reserved				rdage_map0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	rdage_map3	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. rdage_map3 indicates the position of bit 3 in the ID.
[23:21]	RO	reserved	Reserved
[20:16]	RW	rdage_map2	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. rdage_map2 indicates the position of bit 2 in the ID.
[15:13]	RO	reserved	Reserved
[12:8]	RW	rdage_map1	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. rdage_map1 indicates the position of bit 1 in the ID.
[7:5]	RO	reserved	Reserved
[4:0]	RW	rdage_map0	There are 16 levels of aging cycles. Four bits are selected from the ID and the level is determined based on the four bits. rdage_map0 indicates the position of bit 0 in the ID.

QOSB_ROWHIT_PRILVL

QOSB_ROWHIT_PRILVL is a QoSBuf row-hit priority threshold register.

Offset Address	Register Name	Total Reset Value
0x0EC	QOSB_ROWHIT_PRILVL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	ch3_rowhit_pri_lvl			reserved			ch2_rowhit_pri_lvl				reserved				ch1_rowhit_pri_lvl				reserved				ch0_rowhit_pri_lvl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:12]	RW	ch3_rowhit_pri_lvl	Channel 3 priority threshold If the current priority is lower than ch3_rohit_pri_lvl, the priority is changed to ch3_rowhit_pri1. If the current priority is higher than ch3_rohit_pri_lvl, the priority is changed to ch3_rowhit_pri0.
[11]	RO	reserved	Reserved
[10:8]	RW	ch2_rowhit_pri_lvl	Channel 2 priority threshold If the current priority is lower than ch2_rohit_pri_lvl, the priority is changed to ch2_rowhit_pri1. If the current priority is higher than ch2_rohit_pri_lvl, the priority is changed to ch2_rowhit_pri0.
[7]	RO	reserved	Reserved
[6:4]	RW	ch1_rowhit_pri_lvl	Channel 1 priority threshold If the current priority is lower than ch1_rohit_pri_lvl, the priority is changed to ch1_rowhit_pri1. If the current priority is higher than ch1_rohit_pri_lvl, the priority is changed to ch1_rowhit_pri0.
[3]	RO	reserved	Reserved
[2:0]	RW	ch0_rowhit_pri_lvl	Channel 0 priority threshold If the current priority is lower than ch0_rohit_pri_lvl, the priority is changed to ch0_rowhit_pri1. If the current priority is higher than ch0_rohit_pri_lvl, the priority is changed to ch0_rowhit_pri0.

QOSB_ROWHIT_PRI

QOSB_ROWHIT_PRI is a QoSBuf row-hit priority control register.

Offset Address	Register Name	Total Reset Value
0x0F0	QOSB_ROWHIT_PRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ch3_rowhit_pri1			reserved	ch3_rowhit_pri0			reserved	ch2_rowhit_pri1			reserved	ch2_rowhit_pri0			reserved	ch1_rowhit_pri1			reserved	ch1_rowhit_pri0			reserved	ch0_rowhit_pri1			reserved	ch0_rowhit_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	ch3_rowhit_pri1	See ch3_rowhit_pri_lvl.
[27]	RO	reserved	Reserved
[26:24]	RW	ch3_rowhit_pri0	See ch3_rowhit_pri_lvl.
[23]	RO	reserved	Reserved
[22:20]	RW	ch2_rowhit_pri1	See ch2_rowhit_pri_lvl.
[19]	RO	reserved	Reserved
[18:16]	RW	ch2_rowhit_pri0	See ch2_rowhit_pri_lvl.
[15]	RO	reserved	Reserved
[14:12]	RW	ch1_rowhit_pri1	See ch1_rowhit_pri_lvl.
[11]	RO	reserved	Reserved
[10:8]	RW	ch1_rowhit_pri0	See ch1_rowhit_pri_lvl.
[7]	RO	reserved	Reserved
[6:4]	RW	ch0_rowhit_pri1	See ch0_rowhit_pri_lvl.
[3]	RO	reserved	Reserved
[2:0]	RW	ch0_rowhit_pri0	See ch0_rowhit_pri_lvl.

QOSB_ROWHIT_CTRL

QOSB_ROWHIT_CTRL is a QoSBuf row-hit enable register.

Offset Address	Register Name	Total Reset Value
0x0F4	QOSB_ROWHIT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ch3_dual_flow_en	ch2_dual_flow_en	ch1_dual_flow_en	ch0_dual_flow_en	ch3_row_hit_en	ch2_row_hit_en	ch1_row_hit_en	ch0_row_hit_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	ch3_dual_flow_en	Channel 3 row-hit dual-stream enable 0: disabled 1: enabled
[6]	RW	ch2_dual_flow_en	Channel 2 row-hit dual-stream enable 0: disabled 1: enabled
[5]	RW	ch1_dual_flow_en	Channel 1 row-hit dual-stream enable 0: disabled 1: enabled
[4]	RW	ch0_dual_flow_en	Channel 0 row-hit dual-stream enable 0: disabled 1: enabled
[3]	RW	ch3_row_hit_en	Channel 3 row-hit enable 0: disabled 1: enabled
[2]	RW	ch2_row_hit_en	Channel 2 row-hit enable 0: disabled 1: enabled
[1]	RW	ch1_row_hit_en	Channel 1 row-hit enable 0: disabled 1: enabled
[0]	RW	ch0_row_hit_en	Channel 0 row-hit enable 0: disabled 1: enabled

QOSB_CKG_CFG

QOSB_CKG_CFG is a QoSBuf clock control register.

Offset Address	Register Name	Total Reset Value
0x108	QOSB_CKG_CFG	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															dyn_ck_gate
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	dyn_ck_gate	Dynamic clock gating for the QoSBuf module 0: The clock is always enabled. 1: The clock gating is automatic when the module is idle.

QOSB_DMC_LVL

QOSB_DMC_LVL is a QoSBuf threshold control register for commands that enter the DMC module.

Offset Address	Register Name	Total Reset Value
0x10C + 0x4 x chans (chans = 0–1)	QOSB_DMC_LVL	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dmc_cmd_full_lvl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	dmc_cmd_full_lvl	Number of QoSBuf commands that enter the DMC module. When this threshold is reached, the DMC queue is full. NOTE • When this field is set to *N*, the actual number of commands that enter the DMC module is (*N* + 1) because of the pipeline issue. • This register cannot be dynamically configured when it is being accessed.

QOSB_CFG_PERF

QOSB_CFG_PERF is a QoSBuf performance statistics mode register.

Offset Address	Register Name	Total Reset Value
0x120	QOSB_CFG_PERF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		perf_en	perf_mode	perf_prd																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	perf_en	Performance statistics enable 1: enabled 0: disabled **NOTE** When perf_mode is 0 and this bit is enabled, the performance statistics register starts the cyclic count. When perf_mode is 1, this bit is automatically cleared after the counting is complete.
[28]	RW	perf_mode	Performance statistical mode 0: continuous trigger mode. Counters related to performance statistics keep counting to ensure that no data overflows within 1s. 1: single trigger mode. When the performance statistical period reaches the value of perf_prd, the statistical result retains and the counting stops. **NOTE** The maximum statistical result retains after an overflow occurs.
[27:0]	RW	perf_prd	Performance statistical cycle 0x0: invalid 0x1−0xFFFFFFF: statistical cycle The actual statistical cycle is (perf_prd x 16 x tclk). tclk is the bus clock cycle of the DDRC. **NOTE** This configuration is valid only when perf_mode is 1. When perf_mode is 0, counters related to performance statistics keep counting.

QOSB_CMD_SUM

QOSB_CMD_SUM is a QoSBuf accumulated command count register.

Offset Address	Register Name	Total Reset Value
0x124	QOSB_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	qos_cmd_sum	Accumulated value of the commands that are temporarily stored in the QoSBuf in the cycle. The value is wrapped if an overflow occurs.

QOSB_SLOT_STAT0

QOSB_SLOT_STAT0 is QoSBuf queue status register 0.

Offset Address	Register Name	Total Reset Value
0x128	QOSB_SLOT_STAT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_l	Status of bits 0−31 in the QoSBuf cmd queue. If a bit is set to 1, there are commands stored in the corresponding slot; otherwise, the slot is empty.

QOSB_SLOT_STAT1

QOSB_SLOT_STAT1 is QoSBuf queue status register 1.

Offset Address	Register Name	Total Reset Value
0x12C	QOSB_SLOT_STAT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_m0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_m0	Status of bits 32−63 in the QoSBuf cmd queue. If a bit is set to 1, there are commands stored in the corresponding slot; otherwise, the slot is empty.

QOSB_SLOT_STAT2

QOSB_SLOT_STAT2 is QoSBuf queue status register 2.

Offset Address	Register Name	Total Reset Value
0x130	QOSB_SLOT_STAT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_m1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_m1	Status of bits 64−95 in the QoSBuf cmd queue. If a bit is set to 1, there are commands stored in the corresponding slot; otherwise, the slot is empty.

QOSB_SLOT_STAT3

QOSB_SLOT_STAT3 is QoSBuf queue status register 3.

Offset Address	Register Name	Total Reset Value
0x134	QOSB_SLOT_STAT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grp_cmd_valid_h																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	grp_cmd_valid_h	Status of bits 96−127 in the QoSBuf cmd queue. If a bit is set to 1, there are commands stored in the corresponding slot; otherwise, the slot is empty.

QOSB_WBUF_STAT0

QOSB_WBUF_STAT0 is QoSBuf write buffer status register 0.

Offset Address	Register Name	Total Reset Value
0x140 + 0x4 x chans (chans = 0−1)	QOSB_WBUF_STAT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	buf_ldata_valid_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	buf_ldata_valid_l	Status of write buffers 0−31 in the QoSBuf. If a bit is set to 1, a burst is stored in the corresponding buffer; otherwise, the data amount is less than a burst or the buffer is empty.

QOSB_WBUF_STAT1

QOSB_WBUF_STAT1 is QoSBuf write buffer status register 1.

Offset Address	Register Name	Total Reset Value
0x150 + 0x4 x chans (chans = 0−1)	QOSB_WBUF_STAT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	buf_ldata_valid_h																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	buf_ldata_valid_h	Status of write buffers 32−63 in the QoSBuf. If a bit is set to 1, a burst is stored in the corresponding buffer; otherwise, the data amount is less than a burst or the buffer is empty.

QOSB_RDRBUF_STAT

QOSB_RDRBUF_STAT is a buffer status register for the Reorder module.

Offset Address	Register Name	Total Reset Value
0x160 + 0x4 x chans (chans = 0−1)	QOSB_RDRBUF_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	e_vld																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	e_vld	Status of reorder buffers 0−31 in the Reorder. If a bit is set to 1, a burst is stored in the corresponding buffer; otherwise, the data amount is less than a burst or the buffer is empty.

QOSB_INTMSK

QOSB_INTMSK is a QoSBuf interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x170	QOSB_INTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															qos_stat_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	qos_stat_int_mask	QoSBuf command statistics interrupt mask enable 1: masked 0: enabled

QOSB_RINT

QOSB_RINT is a QoSBuf raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x174	QOSB_RINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															qos_stat_rint
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	INT_WC	qos_stat_rint	QoSBuf command statistics interrupt. Writing 1 clears the interrupt.

QOSB_INTSTS

QOSB_INTSTS is a QoSBuf interrupt status register.

Offset Address	Register Name	Total Reset Value
0x178	QOSB_INTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															qos_stat_intsts
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	INT	qos_stat_intsts	QoSBuf command statistics interrupt

QOSB_CMD_CNT

QOSB_CMD_CNT is a QoSBuf command statistics register.

Offset Address	Register Name	Total Reset Value
0x180	QOSB_CMD_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								qos_cmd_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	INT	qos_cmd_cnt	Number of commands in the QoSBuf, including those on the pipeline

QOSB_RNK_CNT

QOSB_RNK_CNT is a QoSBuf command (in each rank) statistics register.

Offset Address	Register Name	Total Reset Value
0x190 + 0x4 x chans (chans = 0−1)	QOSB_RNK_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rnk0_cmd_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	rnk0_cmd_cnt	Number of rank 0 commands in the current channel in the QoSBuf

QOSB_BNK_CNT0

QOSB_BNK_CNT0 is a QoSBuf command (in each bank) statistics register.

Offset Address	Register Name	Total Reset Value
0x1A0 + 0x4 x chans (chans = 0−1)	QOSB_BNK_CNT0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bnk3_cmd_cnt								bnk2_cmd_cnt								bnk1_cmd_cnt								bnk0_cmd_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	bnk3_cmd_cnt	Number of bank 3 commands in the current channel in the DMC

[23:16]	RO	bnk2_cmd_cnt	Number of bank 2 commands in the current channel in the DMC
[15:8]	RO	bnk1_cmd_cnt	Number of bank 1 commands in the current channel in the DMC
[7:0]	RO	bnk0_cmd_cnt	Number of bank 0 commands in the current channel in the DMC

QOSB_BNK_CNT1

QOSB_BNK_CNT1 is a QoSBuf command (in each bank) statistics register.

Offset Address	Register Name	Total Reset Value
0x1B0 + 0x4 x chans (chans = 0−1)	QOSB_BNK_CNT1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	bnk7_cmd_cnt		bnk6_cmd_cnt		bnk5_cmd_cnt		bnk4_cmd_cnt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	bnk7_cmd_cnt	Number of bank 7 commands in the current channel in the DMC
[23:16]	RO	bnk6_cmd_cnt	Number of bank 6 commands in the current channel in the DMC
[15:8]	RO	bnk5_cmd_cnt	Number of bank 5 commands in the current channel in the DMC
[7:0]	RO	bnk4_cmd_cnt	Number of bank 4 commands in the current channel in the DMC

QOSB_BNK_CNT2

QOSB_BNK_CNT2 is a QoSBuf command (in each bank) statistics register.

Offset Address	Register Name	Total Reset Value
0x1C0 + 0x4 x chans (chans = 0−1)	QOSB_BNK_CNT2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	bnk11_cmd_cnt		bnk10_cmd_cnt		bnk9_cmd_cnt		bnk8_cmd_cnt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	bnk11_cmd_cnt	Number of bank 11 commands in the current channel in the DMC
[23:16]	RO	bnk10_cmd_cnt	Number of bank 10 commands in the current channel in the DMC
[15:8]	RO	bnk9_cmd_cnt	Number of bank 9 commands in the current channel in the DMC
[7:0]	RO	bnk8_cmd_cnt	Number of bank 8 commands in the current channel in the DMC

QOSB_BNK_CNT3

QOSB_BNK_CNT3 is a QoSBuf command (in each bank) statistics register.

Offset Address	Register Name	Total Reset Value
0x1D0 + 0x4 x chans (chans = 0−1)	QOSB_BNK_CNT3	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	bnk15_cmd_cnt		bnk14_cmd_cnt		bnk13_cmd_cnt		bnk12_cmd_cnt	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	bnk15_cmd_cnt	Number of bank 15 commands in the current channel in the DMC
[23:16]	RO	bnk14_cmd_cnt	Number of bank 14 commands in the current channel in the DMC
[15:8]	RO	bnk13_cmd_cnt	Number of bank 13 commands in the current channel in the DMC
[7:0]	RO	bnk12_cmd_cnt	Number of bank 12 commands in the current channel in the DMC

QOSB_OSTD_CNT

QOSB_OSTD_CNT is a QoSBuf OSTD command (in each channel) statistics register.

Offset Address	Register Name	Total Reset Value
0x1E0	QOSB_OSTD_CNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				ch1_cmd_ostd		ch0_cmd_ostd	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RO	ch1_cmd_ostd	Number of OSTD commands in channel 1 in the QoSBuf
[7:0]	RO	ch0_cmd_ostd	Number of OSTD commands in channel 0 in the QoSBuf

QOSB_WR_CMD_SUM

QOSB_WR_CMD_SUM is a QoSBuf accumulated write command count register.

Offset Address	Register Name	Total Reset Value
0x1E4	QOSB_WR_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_wr_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	qos_wr_cmd_sum	Accumulated value of the write commands that are temporarily stored in the QoSBuf in the cycle. The value is wrapped if an overflow occurs.

QOSB_RD_CMD_SUM

QOSB_RD_CMD_SUM is a QoSBuf accumulated read command count register.

Offset Address	Register Name	Total Reset Value
0x1E8	QOSB_RD_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qos_rd_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	qos_rd_cmd_sum	Accumulated value of the read commands that are temporarily stored in the QoSBuf in the cycle. The value is wrapped if an overflow occurs.

QOSB_TIMEOUT_MODE

QOSB_TIMEOUT_MODE is a QoSBuf timeout mode selection register.

Offset Address	Register Name	Total Reset Value
0x1F0	QOSB_TIMEOUT_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timeout_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	timeout_mode	Read/Write command timeout mapping mode select 0: The timeout mode is mapped by using the ID and there are 16 levels of timeout periods. For details about the definition of each level, see QOSB_WRTOUT0 to QOSB_WRTOUT3 or QOSB_RDTOUT0 to QOSB_RDTOUT3. 1: The timeout mode is mapped by using the priority and there are eight levels of timeout periods. The levels in the priority mapping table are the same as the lower eight levels in the ID mapping table.

QOSB_WBUF_PRI_CTRL

QOSB_WBUF_PRI_CTRL is a QoSBuf write buffer priority adjustment control register.

Offset Address	Register Name	Total Reset Value
0x1F4	QOSB_WBUF_PRI_CTRL	0x0020_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbuf_hcnt																wbuf_lcnt															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wbuf_hcnt	The value of this field is used by the internal counter only when the number of write commands reaches the value of QOSB_WBUF_CTRL[wbuf_lvl2] (write buffer threshold 2). When the number reaches wbuf_lvl2, the internal counter starts counting. The priorities of the write commands in the write buffer are increased to pri2 until the count value reaches wbuf_hcnt. Note: pri2 indicates the priority of the write buffer threshold 2. For details, see QOSB_WBUF_CTRL[wbuf_pri2].

[15:0]	RW	wbuf_lcnt	The value of this field is used by the internal counter only when the number of write commands reaches the value of QOSB_WBUF_CTRL[wbuf_lvl2] (write buffer threshold 2) and the count value has already reached wbuf_hcnt. When the count value reaches wbuf_hcnt, the internal counter starts counting again. The priorities of the write commands are increased to pril1 until the count value reaches wbuf_lcnt. If the count value is 0, the priorities of the write commands are always pri2. Note: pri1 indicates the priority of the write buffer threshold 1. For details, see QOSB_WBUF_CTRL[wbuf_pri1].

QOSB_RHIT_CTRL

QOSB_RHIT_CTRL is a QoSBuf row-hit priority adjustment control register.

Offset Address	Register Name	Total Reset Value
0x1F8	QOSB_RHIT_CTRL	0x00FF_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rhit_hcnt																rhit_lcnt															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	rhit_hcnt	Time allowed to maintain the row-hit command stream Note: The row-hit command stream is forcibly disconnected when the time for maintaining the row-hit command stream reaches rhit_hcnt. Then the internal counter starts counting again, and the row-hit command stream is allowed to raise the arbitration request until the count value reaches rhit_lcnt.
[15:0]	RW	rhit_lcnt	Duration that the row-hit command stream is disconnected Note: The row-hit command stream is forcibly disconnected when the time for maintaining the row-hit command stream reaches rhit_hcnt. Then the internal counter starts counting again, and the row-hit command stream is allowed to raise the arbitration request until the count value reaches rhit_lcnt.

4.1.7 AWADDR_SRVLNC Registers of the DDRC

4.1.7.1 Register Summary

Table 4-9 describes AWADDR_SRVLNC registers.

Table 4-9 Summary of AWADDR_SRVLNC registers (base address: 0x1211_5000)

Offset Address	Register	Description	Page
0x000	AWADDR_SRVLNC_CLKCFG	Clock gating configuration register	4-72

Offset Address	Register	Description	Page
0x100 + 0x8 x addr_zones	AWADDR_SRVLNC_STARTN	Start address register for segment *n* in the monitored address area	4-73
0x104 + 0x8 x addr_zones	AWADDR_SRVLNC_ENDN	End address register for segment *n* in the monitored address area	4-73
0x200	AWADDR_SRVLNC_STATUS	Address pollution status register for the monitored 32-segment address areas	4-73

Table 4-10 describes the value ranges and meanings of variables in the offset addresses for AWADDR_SRVLNC registers.

Table 4-10 Variables in the offset addresses for AWADDR_SRVLNC registers

Variable	Value Range	Description
addr_zones	0–31	Number of monitored address areas

4.1.7.2 Register Description

AWADDR_SRVLNC_CLKCFG

AWADDR_SRVLNC_CLKCFG is a MUX clock gating configuration register.

Offset Address	Register Name	Total Reset Value
0x000	WADDR_SRVLNC_CLKCFG	0x0000_0007

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								detaddr_gt_en	apg_gt_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	detaddr_gt_en	Static clock gating for the address monitoring module 0: disabled 1: enabled
[0]	RW	apg_gt_en	Static clock gating for the register module in the address monitoring module 0: disabled 1: enabled

AWADDR_SRVLNC_STARTN

AWADDR_SRVLNC_STARTN is a start address register for segment *n* in the monitored address area.

Offset Address	Register Name	Total Reset Value
0x100 + 0x8 x addr_zones	AWADDR_SRVLNC _STARTN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	awaddr_srvlnc_start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	awaddr_srvlnc_start	Start address of segment *n* in the address area Note: The lower 4-bit addresses can be ignored.

AWADDR_SRVLNC_ENDN

AWADDR_SRVLNC_ENDN is an end address register for segment *n* in the monitored address area.

Offset Address	Register Name	Total Reset Value
0x104 + 0x8 x addr_zones	AWADDR_SRVLNC _ENDN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	awaddr_srvlnc_end																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	awaddr_srvlnc_end	End address of segment *n* in the address area Note: The lower 4-bit addresses can be ignored. The configured value is the actual end address + 1.

AWADDR_SRVLNC_STATUS

AWADDR_SRVLNC_STATUS is an address pollution status register for the monitored 32-segment address areas.

Offset Address	Register Name	Total Reset Value
0x200	AWADDR_SRVLNC_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addr_infect_st31	addr_infect_st30	addr_infect_st29	addr_infect_st28	addr_infect_st27	addr_infect_st26	addr_infect_st25	addr_infect_st24	addr_infect_st23	addr_infect_st22	addr_infect_st21	addr_infect_st20	addr_infect_st19	addr_infect_st18	addr_infect_st17	addr_infect_st16	addr_infect_st15	addr_infect_st14	addr_infect_st13	addr_infect_st12	addr_infect_st11	addr_infect_st10	addr_infect_st9	addr_infect_st8	addr_infect_st7	addr_infect_st6	addr_infect_st5	addr_infect_st4	addr_infect_st3	addr_infect_st2	addr_infect_st1	addr_infect_st0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	WC	addr_infect_st31	Monitoring status of segment 31 in the address area 0: There is no write command. 1: There is a write command.
[30]	WC	addr_infect_st30	Monitoring status of segment 30 in the address area 0: There is no write command. 1: There is a write command.
[29]	WC	addr_infect_st29	Monitoring status of segment 29 in the address area 0: There is no write command. 1: There is a write command.
[28]	WC	addr_infect_st28	Monitoring status of segment 28 in the address area 0: There is no write command. 1: There is a write command.
[27]	WC	addr_infect_st27	Monitoring status of segment 27 in the address area 0: There is no write command. 1: There is a write command.
[26]	WC	addr_infect_st26	Monitoring status of segment 26 in the address area 0: There is no write command. 1: There is a write command.
[25]	WC	addr_infect_st25	Monitoring status of segment 25 in the address area 0: There is no write command. 1: There is a write command.
[24]	WC	addr_infect_st24	Monitoring status of segment 24 in the address area 0: There is no write command. 1: There is a write command.

[23]	WC	addr_infect_st23	Monitoring status of segment 23 in the address area 0: There is no write command. 1: There is a write command.
[22]	WC	addr_infect_st22	Monitoring status of segment 22 in the address area 0: There is no write command. 1: There is a write command.
[21]	WC	addr_infect_st21	Monitoring status of segment 21 in the address area 0: There is no write command. 1: There is a write command.
[20]	WC	addr_infect_st20	Monitoring status of segment 20 in the address area 0: There is no write command. 1: There is a write command.
[19]	WC	addr_infect_st19	Monitoring status of segment 19 in the address area 0: There is no write command. 1: There is a write command.
[18]	WC	addr_infect_st18	Monitoring status of segment 18 in the address area 0: There is no write command. 1: There is a write command.
[17]	WC	addr_infect_st17	Monitoring status of segment 17 in the address area 0: There is no write command. 1: There is a write command.
[16]	WC	addr_infect_st16	Monitoring status of segment 16 in the address area 0: There is no write command. 1: There is a write command.
[15]	WC	addr_infect_st15	Monitoring status of segment 15 in the address area 0: There is no write command. 1: There is a write command.
[14]	WC	addr_infect_st14	Monitoring status of segment 14 in the address area 0: There is no write command. 1: There is a write command.
[13]	WC	addr_infect_st13	Monitoring status of segment 13 in the address area 0: There is no write command. 1: There is a write command.
[12]	WC	addr_infect_st12	Monitoring status of segment 12 in the address area 0: There is no write command. 1: There is a write command.

[11]	WC	addr_infect_st11	Monitoring status of segment 11 in the address area 0: There is no write command. 1: There is a write command.
[10]	WC	addr_infect_st10	Monitoring status of segment 10 in the address area 0: There is no write command. 1: There is a write command.
[9]	WC	addr_infect_st9	Monitoring status of segment 9 in the address area 0: There is no write command. 1: There is a write command.
[8]	WC	addr_infect_st8	Monitoring status of segment 8 in the address area 0: There is no write command. 1: There is a write command.
[7]	WC	addr_infect_st7	Monitoring status of segment 7 in the address area 0: There is no write command. 1: There is a write command.
[6]	WC	addr_infect_st6	Monitoring status of segment 6 in the address area 0: There is no write command. 1: There is a write command.
[5]	WC	addr_infect_st5	Monitoring status of segment 5 in the address area 0: There is no write command. 1: There is a write command.
[4]	WC	addr_infect_st4	Monitoring status of segment 4 in the address area 0: There is no write command. 1: There is a write command.
[3]	WC	addr_infect_st3	Monitoring status of segment 3 in the address area 0: There is no write command. 1: There is a write command.
[2]	WC	addr_infect_st2	Monitoring status of segment 2 in the address area 0: There is no write command. 1: There is a write command.
[1]	WC	addr_infect_st1	Monitoring status of segment 1 in the address area 0: There is no write command. 1: There is a write command.
[0]	WC	addr_infect_st0	Monitoring status of segment 0 in the address area 0: There is no write command. 1: There is a write command.

4.1.8 DMC Registers of the DDRC

4.1.8.1 Register Summary

Table 4-11 describes DMC registers.

Table 4-11 Summary of DMC registers (Base address: 0x1211_8000)

Offset Address	Register	Description	Page
0x000	DDRC_CTRL_SREF	DDRC self-refresh control register	4-81
0x00C	DDRC_CTRL_SFC	DDRC software configuration command start register	4-81
0x010	DDRC_CTRL_PERF	DDRC performance statistics control register	4-82
0x020	DDRC_CFG_SREF	DDR self-refresh configuration register	4-82
0x024	DDRC_CFG_INIT	DDR initialization configuration register	4-84
0x028	DDRC_CFG_PD	DDR power-down status register	4-84
0x02C	DDRC_CFG_AREF	DDRC auto-refresh mode register	4-86
0x040	DDRC_CFG_WORKMODE	DDRC operating mode register	4-87
0x044	DDRC_CFG_WORKMODE2	DDRC operating mode register	4-88
0x050	DDRC_CFG_DDRMODE	DDR operating mode register	4-89
0x058	DDRC_CFG_SCRAMB	DDR data scrambling configuration register	4-92
0x060 + 0x4 x rnks	DDRC_CFG_RNKVOL	DDRC-controlled DDR capacity configuration register	4-94
0x0A0+ 0x4 x rnks	DDRC_CFG_ODT	DDR ODT configuration register	4-95
0x0F0	DDRC_CFG_EMRS01	DDR mode register 0 and mode register 1	4-95
0x0F4	DDRC_CFG_EMRS23	DDR mode register 2 and mode register 3	4-96
0x100	DDRC_CFG_TIMING0	DDRC timing parameter register 0	4-97
0x104	DDRC_CFG_TIMING1	DDRC timing parameter register 1	4-98
0x108	DDRC_CFG_TIMING	DDRC timing parameter register 2	4-99

Offset Address	Register	Description	Page
	2		
0x10C	DDRC_CFG_TIMING 3	DDRC timing parameter register 3	4-100
0x110	DDRC_CFG_TIMING 4	DDRC timing parameter register 4	4-101
0x114	DDRC_CFG_TIMING 5	DDRC timing parameter register 5	4-101
0x118	DDRC_CFG_TIMING 6	DDRC timing parameter register 6	4-102
0x120	DDRC_CFG_NXT_TI MING0	DDRC timing parameter register 0 for switching the frequency	4-103
0x124	DDRC_CFG_NXT_TI MING1	DDRC timing parameter register 1 for switching the frequency	4-104
0x128	DDRC_CFG_NXT_TI MING2	DDRC timing parameter register 2 for switching the frequency	4-105
0x12C	DDRC_CFG_NXT_TI MING3	DDRC timing parameter register 3 for switching the frequency	4-106
0x130	DDRC_CFG_NXT_TI MING4	DDRC timing parameter register 4 for switching the frequency	4-107
0x134	DDRC_CFG_NXT_TI MING5	DDRC timing parameter register 5 for switching the frequency	4-108
0x138	DDRC_CFG_NXT_TI MING6	DDRC timing parameter register 6 for switching the frequency	4-108
0x140	DDRC_CFG_BLDAT A	DDRC pre-received write data configuration register	4-109
0x144	DDRC_CFG_DMCLV L	DDRC command queue depth threshold configuration register	4-110
0x200	DDRC_CFG_DDRPH Y	DDR I/O configuration register	4-110
0x20C	DDRC_CFG_SFC_TI M	DDRC software configuration DDR command timing register	4-111
0x210	DDRC_CFG_SFC	DDRC software DDR command attribute register	4-111
0x214	DDRC_CFG_SFC_AD DR0	Read/Write memory address register 0 for the software configuration module	4-113
0x21C	DDRC_CFG_SFC_WD ATA0	Write data register 0 for the software configuration module	4-113

Offset Address	Register	Description	Page
0x220	DDRC_CFG_SFC_WDATA1	Write data register 1 for the software configuration module	4-114
0x224	DDRC_CFG_SFC_WDATA2	Write data register 2 for the software configuration module	4-114
0x228	DDRC_CFG_SFC_WDATA3	Write data register 3 for the software configuration module	4-114
0x254	DDRC_CFG_STADAT	DDRC data statistics control register	4-115
0x258	DDRC_CFG_DATMIN	DMC data counting minimum threshold register	4-116
0x25C	DDRC_CFG_DATMAX	DMC data counting maximum threshold register	4-116
0x260	DDRC_CFG_STACMD	DDR performance statistics mode register	4-117
0x264	DDRC_CFG_CMDMIN	DMC command counting minimum threshold register	4-118
0x268	DDRC_CFG_CMDMAX	DMC command counting maximum threshold register	4-118
0x270	DDRC_CFG_PERF	DDRC performance statistics mode register	4-119
0x274	DDRC_CFG_STAID	DDRC performance statistics command ID register	4-120
0x278	DDRC_CFG_STAIDMSK	DDR performance statistics command ID mask register	4-120
0x280	DDRC_INTMSK	DDRC interrupt mask register	4-121
0x284	DDRC_RINT	DDRC raw interrupt register	4-122
0x288	DDRC_INTSTS	DDRC interrupt status register	4-123
0x290	DDRC_CURR_STATUS	DDRC status register	4-123
0x294	DDRC_CURR_FUNC	DDRC FUNC module status register	4-124
0x298	DDRC_CURR_FUNC2	DDRC FUNC2 module status register	4-125
0x2A0	DDRC_CURR_EXECST	DDRC command state machine status register	4-126
0x2A4	DDRC_CURR_WGFIFOST	DDRC write data FIFO status register	4-126
0x380	DDRC_HIS_FLUX_W	DDRC all write command traffic	4-127

Offset Address	Register	Description	Page
	R	statistics register	
0x384	DDRC_HIS_FLUX_RD	DDRC all read command traffic statistics register	4-127
0x388	DDRC_HIS_FLUX_WCMD	DDRC all write command count register	4-128
0x38C	DDRC_HIS_FLUX_RCMD	DDRC all read command count register	4-128
0x390	DDRC_HIS_FLUXID_WR	DDRC specified ID write traffic statistics registers	4-128
0x394	DDRC_HIS_FLUXID_RD	DDRC specified ID read traffic statistics registers	4-129
0x0398	DDRC_HIS_FLUXID_WCMD	DDRC all ID write command count register	4-129
0x039C	DDRC_HIS_FLUXID_RCMD	DDRC all ID read command count register	4-130
0x3A0	DDRC_HIS_WLATCNT0	DDRC specified ID write command latency statistics register 0	4-130
0x3A4	DDRC_HIS_WLATCNT1	DDRC specified ID write command latency statistics register 1	4-131
0x3A8	DDRC_HIS_RLATCNT0	DDRC specified ID read command latency statistics register 0	4-131
0x3AC	DDRC_HIS_RLATCNT1	DDRC specified ID read command latency statistics register 1	4-132
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	Read channel inherent latency register	4-133
0x3B8	DDRC_STACMD_RPT	Read pointer to the DMC accumulated command count register	4-133
0x3BC	DDRC_HIS_CMD_SUM	DMC accumulated command count register	4-134
0x4A8	DDRC_HIS_SFC_RDATA0	Software configuration read data register 0	4-134
0x4AC	DDRC_HIS_SFC_RDATA1	Software configuration read data register 1	4-134
0x4B0	DDRC_HIS_SFC_RDATA2	Software configuration read data register 2	4-135

Offset Address	Register	Description	Page
0x4B4	DDRC_HIS_SFC_RDATA3	Software configuration read data register 3	4-135

4.1.8.2 Register Description

DDRC_CTRL_SREF

DDRC_CTRL_SREF is a DDRC self-refresh control register.

Offset Address	Register Name	Total Reset Value
0x000	DDRC_CTRL_SREF	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														sref_done	sref_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	sref_done	DDR PHY self-refresh done 0: normal operating mode 1: The transition from 0 to 1 indicates that the DDR PHY completes all required operations after exiting the self-refresh status and the DMC can accept new requests.
[0]	RW	sref_req	SDRAM self-refresh request 0: exit the self-refresh status 1: enter the self-refresh status

DDRC_CTRL_SFC

DDRC_CTRL_SFC is a DDRC software configuration command start register.

Offset Address	Register Name	Total Reset Value
0x00C	DDRC_CTRL_SFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_req

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	cmd_req	Request of executing the configuration command of the DDRC 0: The command is not executed or the parameter is automatically cleared after the command is executed. 1: The command is requested to be executed.

DDRC_CTRL_PERF

DDRC_CTRL_PERF is a DDRC performance statistics enable register.

Offset Address	Register Name	Total Reset Value
0x010	DDRC_CTRL_PERF	0x0014_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															perf_en
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	perf_en	Performance statistics mode 0: disabled 1: enabled **NOTE** When perf_mode is 0 and this bit is enabled, the performance statistics register starts cyclic counting. When perf_mode is 1, this bit is automatically cleared after counting is complete.

DDRC_CFG_SREF

DDRC_CFG_SREF is a DDRC self-refresh configuration register.

Offset Address	Register Name	Total Reset Value
0x020	DDRC_CFG_SREF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asref_en																sref_arefnum				reserved			clk_switch	reserved			sref_odis	reserved			sref_cc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	asref_en	SDRAM automatic self-refresh enable 1: enabled 0: disabled **NOTE** Each rank corresponds to one control bit. The rank automatically enters the self-refresh status only when DDRC_CFG_PD[PD_EN] and the asref_en corresponding to the rank are valid. This function is not supported in this version.
[15:12]	RW	sref_arefnum	Number of self-refresh operations initiated after DDR3 SDRAM exits the self-refresh status during the DFS process 0x0: No self-refresh operation is initiated. 0x1–0xF: *n*
[11:9]	RO	reserved	Reserved
[8]	RW	clk_switch	DDRC low-power clock switch. Whether to back press AXI interface command when the DDRC enters the low-power status (DDR self-refresh) 0: The interface commands are not back pressed, and an error is returned directly. 1: The interface commands are back pressed, and the original command is executed after the clock is switched.
[7:5]	RO	reserved	Reserved
[4]	RW	sref_odis	Output disable for the DDR command and data I/O in self-refresh mode 0: enabled 1: disabled **NOTE** The configuration is a static configuration. It is recommended that this bit be set to 1 to disable the output of the DDR command and data I/O after the DDR enters the self-refresh status. It is recommended that this bit be set to 0 to enable the output of the DDR command and data I/O before the DDR exits the self-refresh status.
[3:1]	RO	reserved	Reserved

[0]	RW	sref_cc	SDRAM clock control in self-refresh mode 0: The SDRAM clock is enabled. 1: The SDRAM clock is disabled.

DDRC_CFG_INIT

DDRC_CFG_INIT is a DDR initialization configuration register.

Offset Address	Register Name	Total Reset Value
0x024	DDRC_CFG_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							wrlvl_en	init_arefnum							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	init_arefnum	Number of auto-refresh operations when the DDR3 SDRAM is being initialized 0x0–0x2: two 0x3–0xF: *n*

DDRC_CFG_PD

DDRC_CFG_PD is a DDR power-down status register.

Offset Address	Register Name	Total Reset Value
0x028	DDRC_CFG_PD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	asref_prd												t_clk_cke				pd_prd												reserved		pd_ac	pd_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	asref_prd	SDRAM self-refresh cycle. When the DDRC does not receive any command in consecutive asref_prd cycles, it forces the SDRAM to enter the self-refresh status. When a command is received, the DDRC forces the SDRAM to exit the self-refresh status. 0x0−0xFFF: (n x 16) clock cycles **NOTE** This field is valid only when asref_en is 1.
[19:16]	RW	t_clk_cke	Relationship between CLK and CKE 0x0−0x7: Delay relative to CKE when the DDR PHY disables the DDR3 clock. The delay is related to the DDR PHY. **NOTE** This field can be set to 0 when the clock is disabled.
[15:4]	RW	pd_prd	SDRAM power-down cycle. When the DDRC does not receive any command in consecutive pd_prd cycles, it forces the SDRAM to enter the power-down status. When a command is received, the DDRC forces the SDRAM to exit the power-down status. 0x00: not enter the power-down status 0x01−0xFFF: *n* clock cycles **NOTE** This field is valid only when pd_en is 1.
[3:2]	RO	reserved	Reserved
[1]	RW	pd_ac	SDRAM address command dynamic disable in power-down mode 1: disable the pin output 0: enable the pin output **NOTE** This field is valid when pd_en is enabled. The control pins do not include CKE, ODT, CSN, and RESET_N.
[0]	RW	pd_en	Automatic power-down enable for the SDRAM 1: enabled 0: disabled

DDRC_CFG_AREF

DDRC_CFG_AREF is a DDRC auto-refresh mode register.

Offset Address	Register Name	Total Reset Value
0x02C	DDRC_CFG_AREF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aref_alarm_num								reserved				aref_alarm_en	aref_dual_rank	aref_opt	aref_mode				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	aref_alarm_num	The auto-refresh command is forced to be transmitted if a specific number of auto-refresh commands cannot be transmitted. 0x0–0xFF: lack of (*n* + 1) auto-refresh commands **NOTE** Only one auto-refresh command is considered when *n* is 255 because the upper bits are lost after the bits of the 8-bit counter are carried. In optimization mode (when aref_opt is 1), an alarm is generated when the number of postponed commands is greater than or equal to 15.
[7:5]	RO	reserved	Reserved
[4]	RW	aref_alarm_en	Auto-refresh loss alarm enable (AREF function) 0: disabled 1: enabled
[3]	RW	aref_dual_rank	REF command transmit mode select 0: The REF commands are transmitted to only one rank each time. 1: The REF commands are transmitted to two ranks each time.
[2]	RW	aref_opt	Auto-refresh optimization enable 1: enabled 0: disabled When this function is enabled, it is recommended that aref_mode be set to 00. The DMC dynamically detects whether the DDR is idle during each auto-refresh. If the DDR is idle, the AREF commands are transmitted; otherwise, the DMC waits until nine AREF cycles are reached. Then the DMC forcibly terminates the DDR access and inserts AREF commands.

[1:0]	RW	aref_mode	Auto-refresh mode 00: An auto-refresh operation is performed every one tREFI cycle. 01: Three auto-refresh operations are performed every three tREFI cycles. 10: Four auto-refresh operations are performed every five tREFI cycles. 11: Eight auto-refresh operations are performed every nine tREFI cycles. Optimized auto-refresh mode 11: The maximum number of postponed commands is 8. 10: The maximum number of postponed commands is 4. 01: The maximum number of postponed commands is 2. 00: The maximum number of postponed commands is 1.

DDRC_CFG_WORKMODE

DDRC_CFG_WORKMODE is a DDRC operating mode register.

Offset Address	Register Name	Total Reset Value
0x040	DDRC_CFG_WORKMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		hdr_mode	read_mode	addr_mode		intlv_en	wrap_en	reserved				apre_en	func_clkon	data_clkon	cmd_clkon	clk_ratio
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	hdr_mode	DFI interface mode select 0: SDR mode 1: HDR mode The Hi3521A supports only the HDR mode.
[12]	RW	read_mode	DDRC read mode 0: associated read mode 1: delay read mode The associated read mode is a mode in which the DDRC samples data based on the data valid signal from the PHY. The delay read mode is a mode in which the DDRC samples the data from the PHY after the internal delay of the DDRC.

[11:10]	RW	addr_mode	DDR address line reverse mode select 00: The address is set to all 1s when the DDR is idle. 01: The status of the previous command is retained when the DDR is idle. 10: The status opposite to the previous status is restored when the DDR is idle. 11: reserved
[9]	RW	intlv_en	DMC burst interleave enable 0: disabled 1: enabled
[8]	RW	wrap_en	Wrap command optimization enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	apre_en	Auto-precharge enable 0: disabled 1: enabled
[3]	RW	func_clkon	Functional module clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[2]	RW	data_clkon	Data channel clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[1]	RW	cmd_clkon	Command channel clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[0]	RW	clk_ratio	Operating mode of the DDRC 0: The ratio of the DDRC frequency to the PHY frequency is 1:1. 1: The ratio of the frequency of the DDRC to the frequency of the PHY is 1:2. NOTE This field is fixed at 1 in this version.

DDRC_CFG_WORKMODE2

DDRC_CFG_WORKMODE2 is a DDRC operating mode register.

Offset Address	Register Name	Total Reset Value
0x044	DDRC_CFG_WORKMODE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				openpage_time												rank_disable															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:16]	RW	openpage_time	Open page delay control 0x0−0x1: The open page function is disabled. 0x2−0x3fff: open page delay **NOTE** The open page function is disabled when DDRC_CFG_WORKMODE[apre_en] is enabled.
[15:0]	RW	rank_disable	Rank disable 0: normal operating mode 1: The auto-refresh/power-down/self-refresh function of a rank is disabled.

DDRC_CFG_DDRMODE

DDRC_CFG_DDRMODE is a DDR operating mode register.

Offset Address	Register Name	Total Reset Value
0x050	DDRC_CFG_DDRMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			bank_mode	reserved			bank_xor	asref_zqc_en	sref_zqc_en		rank	rank_mode			odt_on	zqc_en	reserved		scramb_en	eserved		bc_en	eserved		eserved		brstlen	brstlen2	reserved		mem_width		dram_type			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved

[30:28]	RW	bank_mode	Bank interleaving mode For 8-bit bus width: 000: 8-byte banks are interleaved. 001: 16-byte banks are interleaved. … 111: 1 KB banks are interleaved. For 16-bit bus width: 000: 16-byte banks are interleaved. 001: 32-byte banks are interleaved. … 111: 2 KB banks are interleaved. For 32-bit bus width: 000: 32-byte banks are interleaved. 001: 64-byte banks are interleaved. … 111: 4 KB banks are interleaved. For 64-bit bus width: 000: 64-byte banks are interleaved. 001: 128-byte banks are interleaved. … 111: 8 KB banks are interleaved. **NOTE** When the AXI is set to a non-zero value, this field must be set to 000 and the AXI configuration mode is used. When the AXI is set to 000, the DMC configuration mode is used.
[27:26]	RO	reserved	Reserved
[25:24]	RW	bank_xor	Scrambling enable for the bank address and row address 00: disabled 01: The bank address and offset address 0 are scrambled. 10: The bank address and offset address 1 are scrambled. 11: The bank address and offset address 2 are scrambled.
[23]	RW	asref_zqc_en	SDRAM ZQ enable when the ASREF exits. 0: disabled 1: enabled
[22]	RW	sref_zqc_en	SDRAM ZQ enable when the SREF exits. 0: disabled 1: enabled **NOTE** • This field is valid only for the DDR3 SDRAM and is set to 0 by default. • In addition, the value of this field cannot be dynamically changed during the self-refresh exit process.

[21:20]	RW	rank	Number of DDRC ranks 00: 1 01: 2 10: 3 11: 4 NOTE When the number of external DDR ranks is greater than 4, this field is used to control four groups of ranks (0−3, 4−7, 8−11, and 12−16).
[19:18]	RW	rank_mode	Rank interleaving mode 00: single rank mode 01: single rank mode 10: Two ranks are interleaved. 11: Four ranks are interleaved. NOTE Multiple ranks can be interleaved only when the configuration of these ranks is the same; otherwise, unpredictable errors may occur.
[17]	RW	odt_on	Whether the ODT signal output to the SDRAM is fixed 0: The signal is automatically controlled by the DDRC. 1: The output is fixed at the wodt configuration of rank 0.
[16]	RW	zqc_en	AREF ZQ command enable 0: disabled 1: enabled
[15]	RO	reserved	Reserved
[14]	RW	scramb_en	Data scrambling enable (The scrambling code is generated by using the address, and exclusive ORed with the data to reduce synchronous inversion). 0: disabled 1: enabled
[13]	RO	reserved	Reserved
[12]	RW	bc_en	DDR3 burst chop mode 0: disabled 1: enabled
[11]	RO	reserved	Reserved. This bit must be fixed at 1'b0.
[10:9]	RO	reserved	Reserved

[8]	RW	brstlen	Burst length of the DDRC When brstlen2 is set to 0: 1: BL8 0: BL4 When brstlen2 is set to 1: 1: BL32 0: BL16 The burst length of the DDR3 SDRAM can be set to only burst 8. **NOTE** The burst length is related to the clock ratio of the DMC to the PHY. The burst length is BLx/n (x indicates the burst type, that is, 4, 8, 16, or 32. n indicates that the clock ratio of the DMC to the PHY is 1:n). For example, when the clock ratio is 1:2, to set the DDRC burst length to BL32, set brstlen to 0 and brstlen2 to 1.
[7]	RW	brstlen2	Burst length 2 of the DDRC 1: extended mode 0: basic mode This field works with brstlen.
[6]	RO	reserved	Reserved
[5:4]	RW	mem_width	Bit width of the storage data bus 00: 8 bits 01: 16 bits 10: 32 bits 11: 64 bits
[3:0]	RW	dram_type	External memory type 110: DDR3 Other values: reserved

DDRC_CFG_SCRAMB

DDRC_CFG_SCRAMB is a DDR data scrambling configuration register.

Offset Address	Register Name	Total Reset Value
0x058	DDRC_CFG_SCRAMB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dbi_low_act	rd_dbi_en	wr_dbi_en	reserved												scramb_seed_type	reserved			scramb_seed_sort		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	dbi_low_act	DBI active level 0: active high 1: active low
[17]	RW	rd_dbi_en	Read DBI enable 0: disabled 1: enabled
[16]	RW	wr_dbi_en	Read DBI enable 0: disabled 1: enabled
[15:5]	RO	reserved	Reserved
[4]	RW	scramb_seed_type	Address mode for scrambling 0: Use the CS and BA for scrambling. 1: Use the CS, BA, and low bits of the row address for scrambling.
[3]	RO	reserved	Reserved
[2:0]	RW	scramb_seed_sort	Address arrangement mode for scrambling 000: CS_BA_COL arrangement 001: CS_COL_BA arrangement 010: COL_CS_BA arrangement 011: COL_BA_CS arrangement 100: BA_CS_COL arrangement 101: BA_COL_CS arrangement Other values: reserved

DDRC_CFG_RNKVOL

DDRC_CFG_RNKVOL is a DDRC-controlled DDR capacity configuration register.

Offset Address	Register Name	Total Reset Value
0x060	DDRC_CFG_RNKVOL	0x0000_0022

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															mem_x4	reserved			mem_map	reserved			mem_bank	reserved			mem_row			reserved			mem_col
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	mem_x4	4-bit external component combination mode 0: 8-/16-/32-bit external components are combined. 1: 4-bit external components are combined.
[15:14]	RO	reserved	Reserved
[13:12]	RW	mem_map	Address translation mode of the SDRAM 00: {Rank, Row, Ba, Col, DW} = AXI_Address 01: {Rank, Ba, Row, Col, DW}= AXI_Address 10: {Rank, Row, Ba, Col, cs, Col, DW}= AXI_Address 11: {Rank, Ba, Row, Col, cs, Col, DW}= AXI_Address This parameter can be set to 10 or 11 only when DDRC_CONFIG1[dual_ch] is valid. When there are multiple ranks, the configuration must be the same for each rank. This field must be set to 00 in the current version.
[11:10]	RO	reserved	Reserved
[9:8]	RW	mem_bank	Number of banks of a single SDRAM 00: 4 banks 01: 8 banks 10:16 banks 11: reserved
[7]	RO	reserved	Reserved

[6:4]	RW	mem_row	Bit width of the row address of a single SDRAM 000: 11 bits 001: 12 bits 010: 13 bits 011: 14 bits 100: 15 bits 101: 16 bits Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	mem_col	Bit width of the column address of a single SDRAM 000: 8 bits 001: 9 bits 010: 10 bits 011: 11 bits 100: 12 bits Other values: reserved

DDRC_CFG_ODT

DDRC_CFG_ODT is a DDR ODT configuration register.

Offset Address	Register Name	Total Reset Value
0x0A0	DDRC_CFG_ODT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rodt																wodt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rodt	ODT read enable for other RANKs when the current RANK transmits the read command 1: enabled 0: disabled
[15:0]	RW	wodt	ODT write enable for other RANKs when the current RANK transmits the write command 1: enabled 0: disabled

DDRC_CFG_EMRS01

DDRC_CFG_EMRS01 is a configuration register for DDR mode register 0 and mode register 1.

Offset Address	Register Name	Total Reset Value
0x0F0	DDRC_CFG_EMRS01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs1																mrs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs1	DDR3 SDRAM extended mode register 1 This field corresponds to valid bits 13−0 of mode register 1 (MR1) in the DDR3 SDRAM user manual. MR1[15:14] of most DDRs are not used. DDRC_CFG_EMRS01[31:30] are reserved and set to 2'b00. For details about MR1, see the DDR3 SDRAM user manual.
[15:0]	RW	mrs	DDR3 SDRAM mode register This field corresponds to valid bits 13−0 of mode register 0 (MR0) in the DDR3 SDRAM user manual. MR0[15:14] of most DDRs are not used. DDRC_CFG_EMRS01[15:14] are reserved and set to 2'b00. For details about MR0, see the DDR3 SDRAM user manual.

DDRC_CFG_EMRS23

DDRC_CFG_EMRS23 is a configuration register for DDR mode register 2 and mode register 3.

Offset Address	Register Name	Total Reset Value
0x0F4	DDRC_CFG_EMRS23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs3																emrs2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs3	DDR3 SDRAM extended mode register 3 This field corresponds to valid bits 13−0 of mode register 3 (MR3) in the DDR3 SDRAM user manual. MR3[15:14] of most DDRs are not used. DDRC_CFG_EMRS23[31:30] are reserved and set to 2'b00. For details about MR3, see the DDR3 SDRAM user manual.

[15:0]	RW	emrs2	DDR3 SDRAM extended mode register 2 This field corresponds to valid bits 13−0 of mode register 2 (MR2) in the DDR3 SDRAM user manual. MR2[15:14] of most DDRs are not used. DDRC_CFG_EMRS23[15:14] are reserved and set to 2'b00. For details about MR2, see the DDR3 SDRAM user manual.

DDRC_CFG_TIMING0

DDRC_CFG_TIMING0 is DDRC timing parameter register 0.

Offset Address	Register Name	Total Reset Value
0x100	DDRC_CFG_TIMING0	0xFFFF_FF3F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2 1 0
Name	tmrd	trrd	trp	trcd	trc		reserved	tras	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0	1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Number of wait cycles for the load mode register (LMR) command. The value is tMRD for the DDR3. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[27:24]	RW	trrd	Number of wait cycles from ACT bank A to ACT bank B 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[23:19]	RW	trp	Number of wait cycles for the disable command (PRE period) 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[18:14]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write command 0x0–0x3: 3 clock cycles 0x4–0xF: *n* clock cycles
[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command 0x00–0x01: 1 clock cycle 0x02–0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved

[5:0]	RW	tras	Number of wait cycles from the ACT bank command to the disable command (PRE) 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles Others: Reserved.

DDRC_CFG_TIMING1

DDRC_CFG_TIMING1 is DDRC timing parameter register 1.

Offset Address	Register Name	Total Reset Value
0x084	DDRC_CFG_TIMING1	0xFF22_15FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsre								trtw				twl				tcl						reserved		trfc							
Reset	1	1	1	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command 0x0: reserved 0x01–0xFF: (*n* x 4) clock cycles This field is set to the larger value between tXSDLL and tXS for the DDR3 SDRAM.
[23:20]	RW	trtw	Delay from the last read data command to the first write data command 0x0–0x1: 1 clock cycle 0x2–0xF: (*n* + 1) clock cycles **NOTE** In DDR3 mode, the field value depends on the latency of the board, package, and I/O.
[19:15]	RW	twl	Number of wait cycles from the write command to the write data command 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles For example, 0x3 indicates three clock cycles. **NOTE** The clock cycle is the DDR3 clock cycle.

[14:10]	RW	tcl	Column address strobe (CAS) latency from the read command to the read data operation 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles **NOTE** The clock cycle is the DDR3 clock cycle.
[9]	RO	reserved	Reserved
[8:0]	RW	trfc	Number of wait cycles for the AREF period or AREF to the ACT command. The field value is set to the maximum value of max{trfc, tzqcs}. 0x00: reserved 0x01–0x1FF: *n* clock cycles

DDRC_CFG_TIMING2

DDRC_CFG_TIMING2 is DDRC timing parameter register 2.

Offset Address	Register Name	Total Reset Value
0x108	DDRC_CFG_TIMING2	0xF303_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				reserved								tfaw				reserved	taref										
Reset	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of retaining the self-refresh mode 0x0: reserved 0x1–0xF: *n* clock cycles The field value must be the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE.
[27:24]	RW	twtr	Number of wait cycles for the last write data to the write-to-read command 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles For example, 0x3 indicates three clock cycles.
[23:18]	RO	reserved	Reserved
[17:12]	RW	tfaw	Number of clock cycles for four consecutive activation commands 0x00–0x3F: *n* clock cycles For example, 0x14 indicates 20 clock cycles.

[11]	RO	reserved	Reserved
[10:0]	RW	taref	Number of auto-refresh cycles 0x000: forbidden 0x001–0x7FF: The auto-refresh cycle of the SDRAM is (16 x *n*) clock cycles. For example, 0x008 indicates 128 (16 x 8) clock cycles. The interval tREFI is 7800/16/tclk. Tclk is twice the running cycle of the SDRAM.

DDRC_CFG_TIMING3

DDRC_CFG_TIMING3 is DDRC timing parameter register 3.

Offset Address	Register Name	Total Reset Value
0x10C	DDRC_CFG_TIMING3	0xFFFF_E0F2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd												tzqinit								taond				txard				trtp			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles 0x000: The ZQCS command is forbidden. 0x001–0x3FF: (*n* x 128) AREF cycles The number of ZQCS command cycles is equal to (*n* x 128) taref clock cycles.
[21:13]	RW	tzqinit	Number of ZQ initialization delay cycles 0x0–0x1FF: (n x 4) clock cycles The value needs to be set to the larger value between tZQINIT and tDLLK.
[12:8]	RW	taond	Number of ODT enable/disable cycles In DDR3 mode, this value is set to tWL – 2 (tWL is DDRC_CFG_TIMING1[twl]).
[7:4]	RW	txard	Number of wait cycles of exiting the DDR low-power mode 0x0–0xF: n clock cycles (in decimal) For example, 0x7 indicates seven clock cycles. The field value is the maximum value among tXP, tXARD, tXARDS, and tXS. In DDR3 mode, the field value is the larger value between tXP and tCKE.
[3:0]	RW	trtp	Wait delay from the read command to the disable command 000–010: 2 clock cycles

			011–111: *n* clock cycles Trtp is calculated as follows: Trtp = AL + BL/2 + Max (trtp, 2) – 2

DDRC_CFG_TIMING4

DDRC_CFG_TIMING4 is DDRC timing parameter register 4.

Offset Address	Register Name	Total Reset Value
0x110	DDRC_CFG_TIMING4	0x01FF_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tmod				twlo				reserved															
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:20]	RW	tmod	Delay from the MRS command to ODT and ZQCL validity 0x0–0x1: 1 clock cycle 0x2–0x1F: *n* clock cycles
[19:0]	RO	reserved	Reserved

DDRC_CFG_TIMING5

DDRC_CFG_TIMING5 is DDRC timing parameter register 5.

Offset Address	Register Name	Total Reset Value
0x114	DDRC_CFG_TIMING5	0x1113_FF1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tzqcs								reserved				twr			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:8]	RW	tzqcs	ZQCS calibration delay cycle 0x0−0xFF: (*n* x 2) clock cycles The field value must be greater than or equal to 10 because of the DMC design.
[7:5]	RO	reserved	Reserved
[4:0]	RW	twr	Number of wait cycles of write recovery 0x0−0x1: one clock cycle 0x2−0x1F: *n* clock cycles **NOTE** When the DFS is required, tWR must be set based on the highest chip frequency that may be used. tWR cannot be changed when the DDR frequency changes.

DDRC_CFG_TIMING6

DDRC_CFG_TIMING6 is DDRC timing parameter register 6.

Offset Address	Register Name	Total Reset Value
0x118	DDRC_CFG_TIMING6	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								trrd_l				twtr_l				tccd_l				todt_sft				tcksrx				tcksre			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	trrd_l	Number of trrd wait cycles between bank groups 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles
[19:16]	RW	twtr_l	Number of twtr wait cycles between bank groups 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles
[15:12]	RW	tccd_l	Number of tccd wait cycles between bank groups 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles
[11:8]	RO	reserved	Reserved
[7:4]	RW	tcksrx	tCKSRX for the DDR3. Number of advanced valid beats before the DDR exits the self-refresh status. 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles

[3:0]	RW	tcksre	tCKSRE for the DDR3. Number of beats to be retained after the DDR enters the self-refresh status. 0x0−0x1: one clock cycle 0x2−0xF: *n* clock cycles

DDRC_CFG_NXT_TIMING0

DDRC_CFG_NXT_TIMING0 is DDRC timing parameter register 0 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x120	DDRC_CFG_NXT_TIMING0	0xFFFF_FF3F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2 1 0
Name	tmrd	trrd	trp	trcd	trc		reserved		tras
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0	1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Number of wait cycles for the loading command of the LMR 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[27:24]	RW	trrd	Number of wait cycles from ACT bank A to ACT bank B 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[23:19]	RW	trp	Number of wait cycles for the disable command (PRE period) 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[18:14]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write command 0x0−0x3: three clock cycles 0x4−0xF: *n* clock cycles
[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command 0x00–0x01: one clock cycle 0x02−0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved

[5:0]	RW	tras	Number of wait cycles from the ACT bank command to the disable command (PRE) 0x00−0x01: one clock cycle 0x02−0x3F: *n* clock cycles tras is obtained from DDR user manuals. If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value. If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

DDRC_CFG_NXT_TIMING1

DDRC_CFG_NXT_TIMING1 is DDRC timing parameter register 1 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x124	DDRC_CFG_NXT_TIMING1	0xFF22_15FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsre								trtw				twl				tcl						reserved		trfc							
Reset	1	1	1	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command 0x0: one clock cycle 0x01–0xFF: (*n* x 4) clock cycles When the DDR3 SDRAM is used, the value is set to tXSDLL.
[23:20]	RW	trtw	Delay from the last read data command to the first write data command 0x0 and 0x1: one clock cycle 0x2−0xF: (*n* + 1) clock cycles
[19:15]	RW	twl	Number of wait cycles from the write command to the data write operation 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles For example, 0x3 indicates three clock cycles. **NOTE** The clock cycle is the DDR3 clock cycle.

[14:10]	RW	tcl	Column address strobe latency (CL) from the read command to the data read operation 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles **NOTE** The clock cycle is the DDR3 clock cycle.
[9]	RO	reserved	Reserved
[8:0]	RW	trfc	Number of wait cycles for the AREF period or AREF to the ACT command. The field value is set to the maximum value of max{trfc, tzqcs}. 0x00−0x01: one clock cycle 0x02-0xFF: *n* clock cycles

DDRC_CFG_NXT_TIMING2

DDRC_CFG_NXT_TIMING2 is DDRC timing parameter register 2 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x128	DDRC_CFG_NXT_TIMING2	0xF303_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				reserved				tfaw								reserved	taref										
Reset	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of retaining the low-power mode 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles The field value must be the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE.
[27:24]	RW	twtr	Number of wait cycles for the last data write operation to the write-to-read command 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles For example, 0x3 indicates three clock cycles.
[23:18]	RO	reserved	Reserved

[17:12]	RW	tfaw	Number of clock cycles for four consecutive activation commands 0x00−0x3F: *n* clock cycles For example, 0x14 indicates 20 clock cycles.
[11]	RO	reserved	Reserved
[10:0]	RW	taref	Number of auto-refresh cycles 0x000: auto-refresh disabled 0x001–0x7FF: The auto-refresh cycle of the SDRAM is (16 x *n*) clock cycles. For example, 0x008 indicates 128 (16 x 8) clock cycles. The interval tREF is 7800/16/tclk. Tclk is the running cycle of the SDRAM.

DDRC_CFG_NXT_TIMING3

DDRC_CFG_NXT_TIMING3 is DDRC timing parameter register 3 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x12C	DDRC_CFG_NXT_TIMING3	0xFFDF_F0F2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd												tzqinit								taond				txard				trtp			
Reset	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles 0x000: The ZQCS command is disabled. 0x001−0x3FF: (*n* x 128) AREF cycles The time of ZQCS command cycles is equal to (*n* x 128) taref clock cycles.
[21:13]	RW	tzqinit	Number of ZQ initialization delay cycles 0x0–0x1ff: (*n* x 4) clock cycles The value needs to be set to the larger value between tZQINIT and tDLLK.
[12:8]	RW	taond	Number of ODT enable/disable cycles In DDR3 mode, the value is set to tWL − 2 (tWL is DDRC_CFG_TIMING1[twl]).
[7:4]	RW	txard	Number of wait cycles of exiting the DDR low-power mode 0x0–0xF: (*n* x 2) clock cycles. *n* indicates a decimal value. For example, 0x7 indicates 14 clock cycles. The field value is the maximum value among tXP, tXARD, tXARDS, and tXS.

			In DDR3 mode, when the register is set to tXS, txard only needs to be set to an equivalent clock cycle of 10 ns.
[3:0]	RW	trtp	Wait delay from the read command to the disable command 0000−0010: two clock cycles 0011–1111: n clock cycles Trtp = AL + BL/2 + Max (trtp, 2) – 2

DDRC_CFG_NXT_TIMING4

DDRC_CFG_NXT_TIMING4 is DDRC timing parameter register 4 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x130	DDRC_CFG_NXT_TIMING4	0x01FF_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tmod				twlo				reserved				twldqsen				reserved				twlmrd			
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	Reserved
[24:20]	RW	tmod	Delay from the MRS command to ODT valid 0x0 and 0x1: one clock cycle 0x02−0x1F: *n* clock cycles
[19:16]	RW	twlo	DDR3 write level status delay parameter 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles The parameter is equal to twlo + twloe.
[15:14]	RO	reserved	Reserved
[13:8]	RW	twldqsen	DDR3 write level start delay 0x0 and 0x1: one clock cycle 0x2−0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved
[5:0]	RW	twlmrd	Delay of the initial valid DDR3 write level DQS 0x0 and 0x1: one clock cycle 0x2−0x3F: *n* clock cycles

DDRC_CFG_NXT_TIMING5

DDRC_CFG_NXT_TIMING5 is DDRC timing parameter register 5 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x134	DDRC_CFG_NXT_TIMING5	0x1113_FF1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tzqcs								reserved				twr			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15:8]	RW	tzqcs	ZQCS calibration delay period 0x0−0xFF: (*n* + 1) clock cycles
[7:5]	RW	reserved	Reserved
[4:0]	RW	twr	Number of wait cycles of write recovery 0x0 and 0x1: one clock cycle 0x2−0x1F: *n* clock cycles **NOTE** When DFS is required, tWR must be set based on the maximum chip frequency that may be used. tWR cannot be changed when the DDR frequency changes.

DDRC_CFG_NXT_TIMING6

DDRC_CFG_NXT_TIMING6 is DDRC timing parameter register 6 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x138	DDRC_CFG_NXT_TIMING6	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								trrd_l				twtr_l				tccd_l				reserved				tcksrx				tcksre			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:20]	RW	trrd_l	Number of trrd wait cycles between bank groups 0x0–0x1: one clock cycle 0x2–0xF: *n* clock cycles
[19:16]	RW	twtr_l	Number of twtr wait cycles between bank groups 0x0–0x1: one clock cycle 0x2–0xF: *n* clock cycles
[15:12]	RW	tccd_l	Number of tccd wait cycles between bank groups 0x0–0x1: one clock cycle 0x2–0xF: *n* clock cycles **NOTE** This field is used to configure the cycle of the DDR clock domain.
[11:8]	RO	reserved	Reserved
[7:4]	RW	tcksrx	tCKSRX for the DDR3. Number of advanced valid beats before the DDR exits the self-refresh status. 0x0–0x1: one clock cycle 0x2–0xF: *n* clock cycles
[3:0]	RW	tcksre	tCKSRE for the DDR3. Number of beats to be retained after the DDR enters the self-refresh status. 0x0–0x1: one clock cycle 0x2–0xF: *n* clock cycles

DDRC_CFG_BLDATA

DDRC_CFG_BLDATA is a DDRC pre-received write data configuration register.

Offset Address	Register Name	Total Reset Value
0x140	DDRC_CFG_BLDATA	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												bl_data			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	bl_data	Number of DMC data segments corresponding to each DDR command in the current mode 0x0–0xF: *n* data segments

DDRC_CFG_DMCLVL

DDRC_CFG_DMCLVL is a DDRC command queue depth threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x144	DDRC_CFG_DMCLVL	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				mbist_que_level				reserved				que_level			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:8]	RW	mbist_que_level	Number of command buffers started by the DMC when the MTEST or MCLR function is used 0x0: 1 0x1−0x10: 1−16. The maximum value is related to the code.
[7:5]	RO	reserved	Reserved
[4:0]	RW	que_level	Depth of the command register FIFO in the DMC 0x1−0x10: depth of *n* commands Other values: reserved

DDRC_CFG_DDRPHY

DDRC_CFG_DDRPHY is a DDR I/O configuration register.

Offset Address	Register Name	Total Reset Value
0x200	DDRC_CFG_DDRPHY	0x001F_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												wr_busy_dly				reserved				phy_upden	trdlat							reserved				phy_zqen	reserved							rcv_pdr
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved

[20:16]	RW	wr_busy_dly	Gating enable for the data beat in the PHY The value of this field must be greater than (WL + 2). This field can be set to 0x1F in scenarios that do not have high requirements on power consumption.
[15:13]	RO	reserved	Reserved
[12]	RW	phy_upden	Enable of the DDRC response to dfi_phyupd_en of the DDR PHY 0: disabled 1: enabled
[11:8]	RW	trdlat	Inherent delay of the DDR PHY 0x0−0xF: (*n* + 1) clock cycles This field needs to be set to 8 when synopsys3/2phy is used.
[7:0]	RO	reserved	Reserved

DDRC_CFG_SFC_TIM

DDRC_CFG_SFC_TIM is a DDRC software DDR configuration command timing register.

Offset Address	Register Name	Total Reset Value
0x20C	DDRC_CFG_SFC_TIM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																wait_time															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	wait_time	Wait period after the DDR command configured by the SFC is executed. This field is valid only when DDRC_CFG_SFC[wait_en] is 1.

DDRC_CFG_SFC

DDRC_CFG_SFC is a DDRC software DDR command attribute register.

Offset Address	Register Name	Total Reset Value
0x210	DDRC_CFG_SFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wait_en	pre_dis	reserved																										cmd_type			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wait_en	Enable for exiting a period after the command execution is complete 0: disabled 1: enabled The wait period is configured in DDRC_CFG_SFC_TIM.
[30]	RW	pre_dis	Precharge command transmit disable 0: The precharge command is transmitted before the SFC command. 1: The precharge command is not transmitted before the SFC command, and the corresponding command is transmitted directly.
[29:4]	RO	reserved	Reserved
[3:0]	RW	cmd_type	DDR command configuration 0000: enter the deep power-down status 0001: exit the deep power down mode 0010: LMR command 0011: ZQCL command. In LPDDRX mode, the ZQ type is controlled by setting cmd_mrs. When cmd_mrs is 0xFF, 0x56, and 0xC3, the ZQ type is ZQINIT, ZQCS, and ZQRESET respectively. When cmd_mrs is set to other values, the ZQ type is ZQCL. 0100: write command 0101: read command 0110: precharge all command 0111: read MRS command 1000: AREF command 1001: enter the self-refresh status 1010: exit the self-refresh status 1011: reserved 1111: DFI_CTRL_UPD_REQ/DFI_CTRL_UPD_ACK handshake for requesting the PHY to enter the refresh mode (this operation is not supported in this version)

DDRC_CFG_SFC_ADDR0

DDRC_CFG_SFC_ADDR0 is read/write memory address register 0 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x214	DDRC_CFG_SFC_ADDR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sfc_row																				sfc_col											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	sfc_row	Row address for the memory that is read or written by the software configuration module The maximum address bit width is related to the specifications of the connected component.
[11:0]	RW	sfc_col	Column address for the memory that is read or written by the software configuration module **NOTE** The DDRC access address must be aligned based on the current DMC bit width. For example, if the current DMC bit width is 128 bits: When the 64-/72-bit external DDR is connected, the DMC addresses are accessed based on {sfc_col[15:1], 1'b0}. When the 32-/36-bit external DDR is connected, the DMC addresses are accessed based on {sfc_col[15:2]0.2'b0}.

DDRC_CFG_SFC_WDATA0

DDRC_CFG_SFC_WDATA0 is write data configuration register 0 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x21C	DDRC_CFG_SFC_WDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata0	Bits 31−0 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA1

DDRC_CFG_SFC_WDATA1 is write data configuration register 1 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x220	DDRC_CFG_SFC_WDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata1	Bits 63−32 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA2

DDRC_CFG_SFC_WDATA2 is write data configuration register 2 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x224	DDRC_CFG_SFC_WDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata2	Bits 95−64 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA3

DDRC_CFG_SFC_WDATA3 is write data configuration register 3 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x228	DDRC_CFG_SFC_WDATA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata3																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata3	Bits 127−96 of the written data of the software configuration module

DDRC_CFG_STADAT

DDRC_CFG_ STADAT is a DDRC data statistics control register.

Offset Address	Register Name	Total Reset Value
0x254	DDRC_CFG_ STADAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	dat_stat_en	dat_stat_mode		dat_stat_prd																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	dat_stat_en	DDR data statistics enable 0: disabled 1: enabled **NOTE** When dat_stat _mode is 0 and this bit is enabled, the performance statistics register starts cyclic counting. When dat_stat _mode is 1, this bit is automatically cleared after the counting is complete.
[29:28]	RW	dat_stat_mode	Data statistical mode 2'b00: continuous trigger mode. Counters related to performance statistics keep counting to ensure that no data overflows within 1s. 2'b01: single trigger mode. When the performance statistical period reaches the value of perf_prd, the statistical result retains and the counting stops. When the statistical period is reached, an interrupt is reported. 2'b10: threshold-based trigger mode. When the statistical period is reached, if the counting value is within the threshold, no interrupt is reported. In this case, a counting is started again until the counting value exceeds the threshold. Then an interrupt is reported and the counting stops. **NOTE** When dat_stat_mode is set to 2'b01 or 2'b10, the statistical result retains after an overflow occurs. When dat_stat_mode is set to 2'b00, the statistical value is wrapped after an overflow occurs.

[27:0]	RW	dat_stat_prd	Data statistical period 0x0–0x1: invalid 0x2–0xFFFFFFF: statistical period The actual statistical period is (load_stat_prd x 16 x tclk). tclk is the bus clock cycle of the DDRC. **NOTE** This configuration is valid only when load_stat_mode is 2'b01 or 2'b10. When load_stat_mode is 0, counters related to performance statistics keep counting.

DDRC_CFG_DATMIN

DDRC_CFG_DATMIN is a DMC data counting minimum threshold register.

Offset Address	Register Name	Total Reset Value
0x258	DDRC_CFG_ DATMIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dmc_dat_min																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	dmc_dat_min	Minimum threshold for data statistics. When the data statistical value is less than or equal to this threshold, an interrupt is reported. **NOTE** The threshold is a multiple of 32. That is, if this field is set to *n*, the actual threshold is *n* x 32.

DDRC_CFG_DATMAX

DDRC_CFG_DATMAX is a DMC data counting maximum threshold register.

Offset Address	Register Name	Total Reset Value
0x25c	DDRC_CFG_ DATMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dmc_dat_max																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27:0]	RW	dmc_dat_max	Maximum threshold for data statistics. When the data statistical value is greater than or equal to this threshold, an interrupt is reported. **NOTE** The threshold is a multiple of 32. That is, if this field is set to *n*, the actual threshold is *n* x 32.

DDRC_CFG_STACMD

DDRC_CFG_STACMD is a DDR performance statistics mode register.

Offset Address	Register Name	Total Reset Value
0x260	DDRC_CFG_ STACMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		load_stat_en		Load_stat_mode				load_stat_prd																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	load_stat_en	DDR load statistics enable 0: disabled 1: enabled **NOTE** When dat_stat_mode is 0 and this bit is enabled, the performance statistics register starts cyclic counting. When load_stat_mode is 1, this bit is automatically cleared after the counting is complete.
[29:28]	RW	load_stat _mode	Load statistical mode 2'b00: continuous trigger mode. Counters related to performance statistics keep counting to ensure that no data overflows within 1s. 2'b01: single trigger mode. When the performance statistical period reaches the value of perf_prd, the statistical result retains and the counting stops. When the statistical period is reached, an interrupt is reported. 2'b10: threshold-based trigger mode. When the statistical period is reached, if the counting value is within the threshold, no interrupt is reported. In this case, a counting is started again until the counting value exceeds the threshold. Then an interrupt is reported and the counting stops. **NOTE** If the load statistical result exceeds the maximum counting value, the statistical result is wrapped after an overflow occurs.

[27:0]	RW	load_stat_prd	Load statistical period 0x0–0x1: invalid 0x2–0xFFFFFFF: statistical period The actual statistical cycle is (perf_prd x 16 x tclk). tclk is the bus clock cycle of the DDRC. NOTE This configuration is valid only when perf_mode is 1. When perf_mode is 0, counters related to performance statistics keep counting.

DDRC_CFG_CMDMIN

DDRC_CFG_CMDMIN is a DMC command counting minimum threshold register.

Offset Address	Register Name	Total Reset Value
0x264	DDRC_CFG_ CMDMIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dmc_cmd_min																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	dmc_cmd_min	Minimum threshold for command statistics. When the command statistical value is less than or equal to this threshold, an interrupt is reported. NOTE The threshold is a multiple of 32. That is, if this field is set to *n*, the actual threshold is *n* x 32.

DDRC_CFG_CMDMAX

DDRC_CFG_CMDMAX is a DMC command counting maximum threshold register.

Offset Address	Register Name	Total Reset Value
0x268	DDRC_CFG_ CMDMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dmc_cmd_max																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27:0]	RW	dmc_cmd_max	Maximum threshold for command statistics. When the command statistical value is greater than or equal to this threshold, an interrupt is reported. NOTE The threshold is a multiple of 32. That is, if this field is set to *n*, the actual threshold is *n* x 32.

DDRC_CFG_PERF

DDRC_CFG_PERF is a DDRC performance statistics mode register.

Offset Address	Register Name	Total Reset Value
0x270	DDRC_CFG_PERF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		flux_en	perf_mode	perf_prd																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	flux_en	DMC traffic monitoring enable 0: disabled 1: enabled When traffic monitoring is enabled, the statistics module provides the number of cycles occupied by the DDR interface by ID to each request port. The traffic can be controlled by using this field and the port traffic setting function.
[28]	RW	perf_mode	Performance statistical mode 0: continuous trigger mode. The performance counter continues to count. This ensures no overflow within 1s in continuous count mode. 1: single trigger mode. When the performance statistics time reaches perf_prd, the count value is retained and counting stops. NOTE The maximum statistical result retains after an overflow occurs.

[27:0]	RW	perf_prd	Performance statistics cycle 0x0–0x1: invalid 0x2–0xFFFFFFF: statistical cycles The actual statistics cycle is (perf_prd x 16 x tclk). tclk is the bus clock cycle of the DDRC. **NOTE** This field is valid only when perf_mode is 1. When perf_mode is 0, the performance counter keeps on counting.

DDRC_CFG_STAID

DDRC_CFG_STAID is a DDRC performance statistics command ID register.

Offset Address	Register Name	Total Reset Value
0x274	DDRC_CFG_STAID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sta_id															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	sta_id	Performance statistics by a specified ID. This field works with sta_idmask.

DDRC_CFG_STAIDMSK

DDRC_CFG_STAIDMSK is a DDR performance statistics command ID mask register.

Offset Address	Register Name	Total Reset Value
0x278	DDRC_CFG_STAIDMSK	0x0000_1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sta_idmask															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	sta_idmask	Specified ID mask The DDRC performance statistics register collects statistics only for specified ID commands. Cmd_id (ID of the command in the DDRC) & sta_idmask = sta_id

DDRC_INTMSK

DDRC_INTMSK is a DDRC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x280	DDRC_INTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			rdtimeout_int_mask	reserved		load_int_mask	reserved			sref_err_int_mask	reserved			flux_int_mask	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	rdtimeout_int_mask	DDR PHY read data timeout interrupt mask enable 0: not masked 1: masked
[11:10]	RO	reserved	Reserved
[9]	RW	load_int_mask	DDR load statistical period reach interrupt mask enable 0: not masked 1: masked
[8:6]	RO	reserved	Reserved
[5]	RW	sref_err_int_mask	Command interface access error interrupt mask enable in DDR self-refresh mode 0: not masked 1: masked
[4:2]	RO	reserved	Reserved
[1]	RW	flux_int_mask	DDR FLUX statistical period reach interrupt mask enable 0: not masked 1: masked
[0]	RO	reserved	Reserved

DDRC_RINT

DDRC_RINT is a DDRC raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x284	DDRC_RINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															aref_alarm_rint	reserved			rdtimeout_rint	reserved		load_rint	reserved			sref_err_rint	reserved			flux_rint	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	INT_WC	aref_alarm_rint	DDR AREF command error raw interrupt. Writing 1 clears the interrupt.
[15:13]	RO	reserved	Reserved
[12]	INT_WC	rdtimeout_rint	DDR PHY read data timeout raw interrupt. Writing 1 clears the interrupt.
[11:10]	RO	reserved	Reserved
[9]	INT_WC	load_rint	DDR load statistical period reach interrupt. Writing 1 clears the interrupt.
[8:6]	RO	reserved	Reserved
[5]	INT_WC	sref_err_rint	Self-refresh interface command access interrupt. Writing 1 clears the interrupt.
[4:2]	RO	reserved	Reserved
[1]	RW	flux_rint	DDR FLUX statistics period reach interrupt. Writing 1 clears the interrupt.
[0]	RO	reserved	Reserved

DDRC_INTSTS

DDRC_INTSTS is a DDRC interrupt status register.

Offset Address	Register Name	Total Reset Value
0x288	DDRC_INTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															aref_alarm_intsts	reserved			rdtimeout_intsts	reserved		load_intsts	reserved			sref_err_intsts	reserved			flux_intsts	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	INT	aref_alarm_intsts	DDR AREF command error interrupt
[15:13]	RO	reserved	Reserved
[12]	INT	rdtimeout_intsts	DDR PHY read data timeout interrupt
[11:10]	RO	reserved	Reserved
[9]	INT	load_intsts	DDR load statistical period reach interrupt
[8:6]	RO	reserved	Reserved
[5]	INT	sref_err_intsts	Self-refresh interface command access interrupt
[4:2]	RO	reserved	Reserved
[1]	RW	flux_intsts	DDR FLUX statistics period reach interrupt
[0]	RO	reserved	Reserved

DDRC_CURR_STATUS

DDRC_CURR_STATUS is a DDRC status register.

Offset Address	Register Name	Total Reset Value
0x290	DDRC_CURR_STATUS	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							busy_func	reserved			busy_dmc	reserved			busy

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	busy_func	Status of the DDRC FUNC module. This field is in the SREF status during reset. 0: idle 1: A command is being processed.
[7:5]	RO	reserved	Reserved
[4]	RO	busy_dmc	Status of the DDRC DMC 0: idle 1: A command is being processed.
[3:1]	RO	reserved	Reserved
[0]	RO	busy	Overall status of the DDRC 0: idle 1: A command is being processed.

DDRC_CURR_FUNC

DDRC_CURR_FUNC is a DDRC FUNC module status register.

Offset Address	Register Name	Total Reset Value
0x294	DDRC_CURR_FUNC	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			in_sfc	reserved			aref_opt_stat	reserved							in_sref
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	in_sfc	DDRC SFC status 0: idle 1: An SFC command is being processed.
[11:9]	RO	reserved	Reserved

[8]	RO	aref_opt_stat	Auto-refresh optimization mode status 1: The DDR is in optimization mode. 0: The DDR exits the optimization mode **NOTE** Before the DDR SDRAM enters the self-refresh status through configuration or requests over the csysreq interface, ensure that the DDR SDRAM exits the auto-refresh optimization mode. This is because some postponed commands may not be transmitted in self-refresh optimization mode.
[7:1]	RO	reserved	Reserved
[0]	RO	in_sref	DDR self-refresh status 0: normal 1: self-refresh.

DDRC_CURR_FUNC2

DDRC_CURR_FUNC2 is a DDRC FUNC2 module status register.

Offset Address	Register Name	Total Reset Value
0x298	DDRC_CURR_FUNC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_ct																dmc_cv															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	in_asref	DDRC automatic self-refresh status 1: automatic self-refresh status 0: normal status Each bit represents a rank.
[15:0]	RO	in_pd	DDRC power-down status 1: power-down status 0: normal status Each bit represents a rank.

DDRC_CURR_EXECST

DDRC_CURR_EXECST is a DDRC command state machine status register.

Offset Address	Register Name	Total Reset Value
0x2A0	DDRC_CURR_EXECST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_ct																dmc_cv															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dmc_ct	Controller command type 0: read command 1: write command
[15:0]	RO	dmc_cv	Controller command validity flag 0: invalid 1: valid

DDRC_CURR_WGFIFOST

DDRC_CURR_WGFIFOST is a DDRC write data FIFO status register.

Offset Address	Register Name	Total Reset Value
0x2A4	DDRC_CURR_WGFIFOST	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wgntfifo_e
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wgntfifo_e	WGNT_FIFO empty or full status. The empty status indicates that all written data is received, and the non-empty status indicates that the written data is not completely received. 0: not empty 1: empty

DDRC_HIS_FLUX_WR

DDRC_HIS_FLUX_WR is a DDRC all write command traffic statistics register.

Offset Address	Register Name	Total Reset Value
0x380	DDRC_HIS_FLUX_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_wr	Write traffic statistics of all masters with the IDs of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_RD

DDRC_HIS_FLUX_RD is a DDRC all read command traffic statistics register.

Offset Address	Register Name	Total Reset Value
0x384	DDRC_HIS_FLUX_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_rd	Read traffic statistics of all masters with the IDs of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_WCMD

DDRC_HIS_FLUX_WCMD is a DDRC all write command count register.

Offset Address	Register Name	Total Reset Value
0x388	DDRC_HIS_FLUX_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_wr_cmd	Write command count of the masters with all IDs of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_RCMD

DDRC_HIS_FLUX_RCMD is a DDRC all read command count register.

Offset Address	Register Name	Total Reset Value
0x38C	DDRC_HIS_FLUX_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_rd_cmd	Read command count of the masters with all IDs of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_WR

DDRC_HIS_FLUXID_WR is a DDRC specified ID write traffic statistics registers.

Offset Address	Register Name	Total Reset Value
0x390	DDRC_HIS_FLUXID_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_wr	Write traffic statistics of the master with the specified ID of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** The unit is the DMC data bit width (128 bits).

DDRC_HIS_FLUXID_RD

DDRC_HIS_FLUXID_RD is a DDRC specified ID read traffic statistics registers.

Offset Address	Register Name	Total Reset Value
0x394	DDRC_HIS_FLUXID_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_rd	Read traffic statistics of the master with the specified ID of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** The unit is the DMC data bit width (128 bits).

DDRC_HIS_FLUXID_WCMD

DDRC_HIS_FLUXID_WCMD is a DDRC all ID write command count register.

Offset Address	Register Name	Total Reset Value
0x0398	DDRC_HIS_FLUXID_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_wr_cmd	Read traffic statistics of the master based on specified IDs. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_RCMD

DDRC_HIS_FLUXID_RCMD is a DDRC all ID read command count register.

Offset Address	Register Name	Total Reset Value
0x039C	DDRC_HIS_FLUXID_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_rd_cmd	Read command count of the master based on specified IDs. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_WLATCNT0

DDRC_HIS_WLATCNT0 is DDRC specified ID write command latency statistics register 0.

Offset Address	Register Name	Total Reset Value
0x3A0	DDRC_HIS_WLATCNT0	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wlatcnt_max																wlatcnt_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	wlatcnt_max	Maximum latency of the write command with the specified ID of the DDRC This field is cleared when the next statistics start.
[15:0]	RO	wlatcnt_min	Minimum latency of the write command with the specified ID of the DDRC. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_WLATCNT1

DDRC_HIS_WLATCNT1 is DDRC specified ID write command latency statistics register 1.

Offset Address	Register Name	Total Reset Value
0x3A4	DDRC_HIS_WLATCNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wlatcnt_all																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	wlatcnt_all	Accumulated latency of the write command with the specified ID in the statistics cycle (the results of the lower four bits are ignored) When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** Software can obtain the average latency of the write command with the specified ID by dividing wlatcnt_all by fluxid_wr_cmd.

DDRC_HIS_RLATCNT0

DDRC_HIS_RLATCNT0 is a DDRC specified ID read command latency statistics register 0.

Offset Address	Register Name	Total Reset Value
0x3A8	DDRC_HIS_RLATCNT0	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rlatcnt_max																rlatcnt_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	rlatcnt_max	Maximum latency of the read command with the specified ID of the DDRC The actual maximum read latency is rlatcnt_max plus inhere_rlatcnt. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.
[15:0]	RO	rlatcnt_min	Minimum latency of the read command with the specified ID of the DDRC Note that the actual minimum read latency is rlatcnt_min plus inhere_rlatcnt. The maximum value is retained if an overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_RLATCNT1

DDRC_HIS_RLATCNT1 is DDRC specified ID read command latency statistics register 1.

Offset Address	Register Name	Total Reset Value
0x3AC	DDRC_HIS_RLATCNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rlatcnt_all																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rlatcnt_all	Accumulated latency of the read command with the specified ID in the statistics cycle (the results of the lower four bits are ignored) When perf_mode is 0, the value is wrapped when an overflow occurs. When perf_mode is 1, the value is retained when an overflow occurs. This field is cleared when the next statistics start. **NOTE** Software can obtain the average latency of the read command with the specified ID by using rlatcnt_all/fluxid_rd_cmd+inhere_rlatcnt.

DDRC_HIS_INHERE_RLAT_CNT

DDRC_HIS_INHERE_RLAT_CNT is a read channel inherent latency register.

Offset Address	Register Name	Total Reset Value
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																inhere_rlatcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	inhere_rlatcnt	Inherent latency of the read data channel for the DDRC and PHY. The actual latency can be obtained only by using this register and rlatcnt_min, rlatcnt_max, rlatcnt_all, and fluxid_rd_cmd.

DDRC_STACMD_RPT

DDRC_STACMD_RPT is the read pointer to the DMC accumulated command count register.

Offset Address	Register Name	Total Reset Value
0x3B8	DDRC_STACMD_RPT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													stacmd_rpt		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	stacmd_rpt	In threshold-based statistical mode, the latest eight load statistical results are stored. This pointer is used to indicate the statistical result that the read DDRC_HIS_CMD_SUM value points to. 000: latest statistical result 001: second to the latest statistical result … 111: latest seventh statistical result

DDRC_HIS_CMD_SUM

DDRC_HIS_CMD_SUM is a DDRC accumulated command count register.

Offset Address	Register Name	Total Reset Value
0x3BC	DDRC_HIS_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_cmd_sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dmc_cmd_sum	Accumulated value of the commands that are temporarily stored in the DMC in the cycle. The value is wrapped if an overflow occurs.

DDRC_HIS_SFC_RDATA0

DDRC_HIS_SFC_RDATA0 is SFC read data register 0.

Offset Address	Register Name	Total Reset Value
0x4A8	DDRC_HIS_SFC_RDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rdata0	Bits 31−0 of the data read by the SFC

DDRC_HIS_SFC_RDATA1

DDRC_HIS_SFC_RDATA1 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4AC	DDRC_HIS_SFC_RDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rdata1	Bits 63−32 of the data read by the SFC

DDRC_HIS_SFC_RDATA2

DDRC_HIS_SFC_RDATA2 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4B0	DDRC_HIS_SFC_RDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rdata2	Bits 95−64 of the data read by the SFC

DDRC_HIS_SFC_RDATA3

DDRC_HIS_SFC_RDATA3 is software configuration read data register 3.

Offset Address	Register Name	Total Reset Value
0x4B4	DDRC_HIS_SFC_RDATA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata3	Bits 127−96 of the data read by the SFC

4.1.9 DDR PHY Registers

4.1.9.1 Register Summary

NOTE

The variable *n* in the offset addresses for DDR PHY registers indicates the data block ID and ranges from 0 to 3.

Table 4-12 describes DDR PHY registers.

Table 4-12 Summary of DDR PHY registers (base address: 0x1211_C000)

Offset Address	Register	Description	Page
0x000	REVISION	PHY control block version register	4-141
0x004	PHYINITCTRL	PHY initialization control register	4-142

Offset Address	Register	Description	Page
0x008	PHYINITSTATUS	PHY status register	4-144
0x00C	PHYCLKGATED	PHY clock gating control register	4-145
0x010	PHYTIMER0	PHY timing parameter register	4-147
0x014	PHYTIMER1	DRAM CKE low initialization register	4-147
0x018	PLLCTRL	Timing parameter register for the PLL in both address/command and data block	4-148
0x01C	PLLTIMER	PLL address/command and data block control register	4-149
0x020	DLYMEASCTRL	Read delay line delay measurement control register	4-149
0x024	IMPCTRL	ZQ calibration control register	4-150
0x028	IMPSTATUS	ZQ calibration result register	4-151
0x02C	DRAMCFG	DRAM system configuration register	4-152
0x030	DRAMTIMER0	DRAM timing parameter register 0	4-153
0x034	DRAMTIMER1	DRAM timing parameter register 1	4-154
0x038	DRAMTIMER2	DRAM timing parameter register 2	4-155
0x03C	DRAMTIMER3	DRAM timing parameter register 3	4-155
0x040	DRAMTIMER4	DRAM write leveling timing parameter register	4-156
0x044	ODTCR	Rank ODT control register while reading or writing to particular ranks	4-156
0x048	TRAINCTRL0	Training control register	4-157
0x04C	RANKEN	Training rank control register	4-159
0x0050	TRAINMADDR	Data training memory start address register	4-160
0x0054	BISTCTRL	Built-in self test (BIST) behavior register	4-160
0x0058	BISTDATA0	DRAM loopback test BIST data register 0	4-162
0x005C	BISTDATA1	DRAM loopback test BIST data register 1	4-162
0x0060	BISTSTATUS	BIST test result and status register	4-163
0x0064	MODEREG01	Mode register content register 1	4-164
0x0068	MODEREG23	Mode register content register 2	4-164
0x006C	DETPATTERN	Write/Read DET pattern register	4-165
0x0070	MISC	Miscellaneous control register	4-166

Offset Address	Register	Description	Page
0x0074	RNK2RNK	Rank-to-rank delay control register	4-168
0x0078	PHYCTRL0	PHY control register 0	4-168
0x007C	PHYDBG	PHY debug register	4-169
0x0080	RETCTRL0	Retraining control register	4-169
0x0084	DMSEL	DM swap selection register	4-170
0x0088	IOCTL	I/O control register	4-171
0x008C	DQSSEL	PHY DQ swap register	4-171
0x0090	PHYCTRL1	AC PHY control register	4-172
0x0094	DXNCKCTRL	PLL phase selection register	4-173
0x0098	PHYPLLCTRL_AC	PHY PLL control register 1	4-173
0x009C	PHYPLLCTRL_DX	PHY PLL control register 2	4-174
0x00A0	SWTMODE	S/W training mode register	4-175
0x00A4	SWTWLDQS	Write DQS issue register during S/W write leveling training	4-175
0x00A8	SWTRLT	S/W training result register	4-176
0x00AC	PHYCTRL2	PHY control register 2	4-176
0x00B0	IOCTL1	PHY I/O control register 1	4-177
0x00B4	IOCTL2	PHY I/O control register 2	4-177
0x00B8	BISTTIMER	Code update period register during BIST running	4-178
0x00D0	TRAINCTRL1	Data training control register 1	4-179
0x00D4	TRAINCTRL2	Data training control register 2	4-180
0x00D8	REGBANKCTRL	Register bank control register	4-181
0x00DC	TRAINCTRL3	Data training control register 3	4-181
0x100	ACBISTCTRL0	Comparison control register 0 while BIST activated	4-183
0x104	ACBISTCTRL1	Comparison control register 1 while BIST activated	4-184
0x108	ACBISTSTS0	BIST test result and status register 0	4-185
0x10C	ACBISTSTS1	BIST test result and status register 1	4-186
0x120	ACCMDBDL0	AC command bit delay line configuration register 0	4-186

Offset Address	Register	Description	Page
0x124	ACCMDBDL1	AC command bit delay line configuration register 1	4-186
0x128	ACCMDBDL2	AC command bit delay line configuration register 2	4-187
0x12C	ACCMDBDL3	AC command bit delay line configuration register 3	4-187
0x130	ACCMDBDL4	AC command bit delay line configuration register 4	4-188
0x134	ACCMDBDL5	AC command bit delay line configuration register 5	4-188
0x138	ACCMDBDL6	AC command bit delay line configuration register 6	4-189
0x13C	ACCMDBDL7	AC command bit delay line configuration register 7	4-189
0x140	ACADDRBDL0	AC address bit delay line configuration register 0	4-190
0x144	ACADDRBDL1	AC address bit delay line configuration register 1	4-190
0x148	ACADDRBDL2	AC address bit delay line configuration register 2	4-191
0x14C	ACADDRBDL3	AC address bit delay line configuration register 3	4-191
0x150	ACADDRBDL4	AC address bit delay line configuration register 4	4-192
0x154	ACADDRBDL5	AC address bit delay line configuration register 5	4-192
0x158	ACADDRBDL6	AC address bit delay line configuration register 6	4-193
0x15C	ACADDRBDL7	AC address bit delay line configuration register 7	4-193
0x160	ACADDRBDL8	AC address bit delay line configuration register 8	4-194
0x164	ACADDRBDL9	AC address bit delay line configuration register 9	4-194
0x168	ACCLKBDL	AC clock bit delay line configuration register	4-195
0x170	ACPHYCTL0	AC block PHY control register 0	4-195
0x174	ACPHYCTL1	AC block PHY control register 1	4-196

Offset Address	Register	Description	Page
0x178	ACPHYCTL2	AC block PHY control register 2	4-197
0x17C	ACPHYCTL3	AC block PHY control register 3	4-198
0x180	ACPHYCTL4	AC block PHY control register 4	4-199
0x184	ACPHYCTL5	AC block PHY control register 5	4-200
0x188	ACPHYCTL6	AC block PHY control register 6	4-201
0x018C	ACPHYCTL7	AC block PHY control register 7	4-201
0x0190	ACDEBUG	PHY debugging register	4-202
0x0194	ACPHYRSVDC	AC block PHY reserved control pin register 1	4-203
0x0198	ACPHYRSVDS	AC block PHY reserved control pin register 2	4-203
0x019C	ACPHYCTL8	AC block PHY control register 8	4-204
0x1A0	ACCMDBDL8	AC command bit delay line configuration register 8	4-204
0x1A4	ACCMDBDL9	AC command bit delay line configuration register 9	4-205
0x1A8	ACCMDBDL10	AC command bit delay line configuration register 10	4-205
0x1AC	ACCMDBDL11	AC command bit delay line configuration register 11	4-206
0x01B0	ACPHYDCC	AC block PHY DCC control register	4-206
0x01B4	ACPHYCTL9	AC block PHY control register 9	4-207
0x01C0	CATTIMER0	CA training timer 0 register	4-208
0x01C4	CATTIMER1	CA training timer 1 register	4-209
0x01C8	CATCONFIG	CA training configuration register	4-209
0x01CC	CATRESULT	CA training result register (for debugging)	4-211
0x01D0	PHYDQRESULT	SW CA training DQ result (from PHY) register	4-211
0x01D4	ADDRPHBOUND	CA training address phase boundary register	4-211
0x01D8	SWCATPATTERN_P	SW CA training pattern register for the positive CK edge	4-213
0x01DC	SWCATPATTERN_N	SW CA training pattern register for the negative CK edge	4-213

Offset Address	Register	Description	Page
0x01E4	LPCTRL	Low-power control register	4-213
0x200 + *n* x 0x80	DXNBISTCTRL	Loopback data comparison control register during BIST of data blocks	4-215
0x204 + *n* x 0x80	DXNBISTSTS	BIST test result and status register	4-216
0x208 + *n* x 0x80	DXNCTRL	Data block control register	4-217
0x210 + *n* x 0x80	DXNWDQNBDL0	Data block bit delay configuration register 0	4-217
0x214 + *n* x 0x80	DXNWDQNBDL1	Data block bit delay configuration register 1	4-218
0x218 + *n* x 0x80	DXNWDQNBDL2	Data block bit delay configuration register 2	4-219
0x21C + *n* x 0x80	DXNRDQNBDL0	Data block bit delay configuration register 3	4-219
0x220 + *n* x 0x80	DXNRDQNBDL1	Data block bit delay configuration register 4	4-220
0x224 + *n* x 0x80	DXNRDQNBDL2	Data block bit delay configuration register 5	4-221
0x22C + *n* x 0x80	DXNRDQSDLY	Local delay line control register	4-221
0x230 + *n* x 0x80	DXNWDQSDLY	Write leveling DQS delay control register	4-222
0x234 + *n* x 0x80	DXNWDQDLY	Write leveling delay line control register	4-222
0x238 + *n* x 0x80	DXNWLSL	Extra system latency addition control register	4-223
0x23C + *n* x 0x80 + *m* x 0x400	DXNRDQSGDLY	Local delay line control register	4-223
0x240 + *n* x 0x80	DXPHYCTRL	DX PHY control register	4-224
0x248 + *n* x 0x80	DXNGDS	Latch enable register	4-225
0x24C + *n* x 0x80	DXNCLKBDL	Data block clock bit delay line configuration register	4-225
0x250 + *n* x 0x80	DXNRDBOUND	Read data eye boundary register	4-226

Offset Address	Register	Description	Page
0x254 + *n* x 0x80	DXNWRBOUND	Write data eye boundary register	4-226
0x258 + *n* x 0x80	DXNOEBDL	Output enable delay line control register	4-227
0x260 + *n* x 0x80	DXNMISCCTRL0	Data block PHY miscellaneous control register 0	4-227
0x264 + *n* x 0x80	DXNMISCCTRL1	Data block PHY miscellaneous control register 1	4-228
0x268 + *n* x 0x80	DXDEBUG0	Data block PHY debug signal register 0	4-229
0x26C + *n* x 0x80	DXDEBUG1	Data block PHY debug signal register 1	4-230
0x270 + *n* x 0x80	DXPHYRSVD	Data block PHY reserved control pin register	4-230
0x274 + *n* x 0x80	DXNMISCCTRL2	Data block PHY miscellaneous control register 2	4-231
0x278 + *n* x 0x80	DXDEBUGCONFIG	Data block PHY debugging control register	4-232
0x27C + *n* x 0x80	DXNDCC	Data block PHY DCC control register	4-233

4.1.9.2 Register Description

REVISION

REVISION is a PHY control block version register.

Offset Address	Register Name	Total Reset Value
0x000	REVISION	0x0000_0012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																major								minor							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RO	major	Major version of the PHY control block.
[7:0]	RO	minor	Minor version of the PHY control block.

PHYINITCTRL

PHYINITCTRL is a PHY initialization control register.

NOTE

Writing to this register has no effect if init_en is 1.

Offset Address	Register Name	Total Reset Value
0x004	PHYINITCTRL	0x0000_000E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctl_cke_bypass	reserved															phyconn_rst	pack_rst	phy_rst	dram_rst	cat_en	dram_init_en	wdet_en	rdet_en	wl2_en	gdst_en	gt_en	wl_en	zcal_en	dlymeas_en	pll_init_en	init_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Access	Name	Description
[31]	RW	ctl_cke_bypass	PACK CKE bypass function enable. 1'b1: CKE is controlled by MC even when PACK controls the DFI interface. 1'b0: CKE is controlled by PACK when PACK controls the DFI interface.
[30:16]	RO	reserved	Reserved.
[15]	RW	phyconn_rst	PHY counter reset. This field is used to set the PHY counter reset signal. To issue a reset signal to PHY counter, this field should be set to 1. To end the reset signal to PHY counter, this field should be cleared. Note that the reset signal connects to the A/C block counter and the counter of all of the data blocks.
[14]	RW	pack_rst	PACK reset. This field is used to issue reset to all the digital circuits of the PACK including the register file. If this field is set to 1, all of the digital parts (including control registers) of the PHY will be set to default value. The reset will be automatically executed, and this bit will be cleared after reset is complete.
[13]	RW	phy_rst	PHY reset. This field is used to set PHY reset signal. To issue a reset signal to the PHY, this field should be set to 1. To end the reset signal to the PHY, this field should be cleared. Note that the reset signal connects to the A/C block and all of the data blocks.

[12]	RW	dram_rst	DRAM reset. This field is used to initiate the DRAM reset sequence. If this field is set to 1, RESET# and CKE will be pulled low for t_dram_rst. After t_dram_rst, the CKE RESET# is pulled to high while keeping CKE at low for t_cke_low. After t_cke_low, CKE is pulled to high, and after t_cke_high, this field is cleared automatically. For LPDDR2/LPDDR3, only CKE will be active during DRAM reset sequence.
[11]	RW	cat_en	HW CA training enable. Writing 1 to this field starts the HW CA training sequence. This field will be cleared after CA training is complete. Note that the CA training applies only to LPDDR3.
[10]	RW	dram_init_en	DRAM initialization enable. This field is used to control whether the internal DRAM initialization sequence is executed after PHY initialization is complete. For LPDDR2/LPDDR3, this field will complete the initial sequence including tINIT3−tINIT5 & tZQC.
[9]	RW	wdet_en	Write data eye training enable. Writing 1 to this field starts the write data eye training sequence. This field will be cleared after the write data eye training is complete.
[8]	RW	rdet_en	Read data eye training enable. Writing 1 to this field starts the read data eye training sequence. This field will be cleared after the read data eye training is complete.
[7]	RW	wl2_en	Second write leveling enable. Writing 1 to this field starts write latency adjustment. This field will be cleared after adjustment is complete. Note that write leveling adjustment applies only to DDR3.
[6]	RW	gdst_en	PHY read data latch train enable. Writing 1 to this field starts the read data latch position training. This field will be cleared after write leveling is complete.
[5]	RW	gt_en	Gate training enable. Writing 1 to this field starts the gate training sequence. This field will be cleared after the gate training is complete.
[4]	RW	wl_en	Write leveling enable. Writing 1 to this field starts the write leveling sequence. This field will be cleared after write leveling is complete. Note that write leveling applies only to DDR3.
[3]	RW	zcal_en	Impedance calibration enable. This field is used to specify whether impedance calibration is executed. This bit will be cleared after impedance calibration is complete.

[2]	RW	dlymeas_en	Delay measurement enable. This field is used to enable initial delay measurement of the activated read delay line. If it is set to 1, delay measurement is enabled.
[1]	RW	pll_init_en	PLL initialization enable. If this field is used to activate the PLL initialization. If it is set to 1, the PLL is reset and waiting for a period of time for PLL to be locked.
[0]	RW	init_en	PHY initialization enable. Writing 1 to this field triggers the PHY initialization sequence. The exact initialization executed is specified in bits 1−15 of this register. If PHY initialization is complete, this bit will be cleared. Note that writing 0 to this field has no effect.

PHYINITSTATUS

PHYINITSTATUS is a PHY status register.

Offset Address	Register Name	Total Reset Value
0x008	PHYINITSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					cat_err	wdet_err	rdet_err	wl2_err	gdst_err	gt_err	wl_err	zcal_err	dlymeas_err	pll_lock_err	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RWC	cat_err	CA training error. This field indicates whether an error occurs during CA training. Writing 1 to this field clears the error status.
[9]	RWC	wdet_err	Write data eye calibration error. This field indicates whether an error occurs during write data eye calibration. Writing 1 to this field clears the error status.
[8]	RWC	rdet_err	Read data eye calibration error. This field indicates whether an error occurs during read data eye calibration. Writing 1 to this field clears the error status.
[7]	RWC	wl2_err	Write leveling adjustment error. This field indicates whether an error occurs during write leveling adjustment. Writing 1 to this field clears the error status.

[6]	RWC	gdst_err	PHY read data latch train error. This field indicates whether an error occurs during read data latch training. Writing 1 to this field clears the error status.
[5]	RWC	gt_err	Gate training error. This field indicates whether an error occurs during gate training. Writing 1 to this field clears the error status.
[4]	RWC	wl_err	Write leveling error. This field indicates whether an error occurs during write leveling. Writing 1 to this field clears the error status.
[3]	RWC	zcal_err	Impedance calibration error. This field indicates whether an error occurs during impedance calibration. Writing 1 to this field clears the error status.
[2]	RWC	dlymeas_err	Delay measurement fail. This field indicates whether one of the initial delay measurements fails. Writing 1 to this field clears the error status.
[1]	RWC	pll_lock_err	PLL locked fail. This field indicates whether one of the PLLs within the PHY fails to assert locked flag after t_pll_lock timer. Writing 1 to this field clears the error status.
[0]	RO	reserved	Reserved.

PHYCLKGATED

PHYCLKGATED is a PHY clock gating control register.

Offset Address	Register Name	Total Reset Value
0x000C	PHYCLKGATED	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	byp_pll_lock	reserved																		dx_phgated_men	dx_phclkgated	dx_phgated_en	ck_phy_clkgated	ac_phy_clkgated	reserved				dx_phy_clkgated			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	byp_pll_lock	PLL lock bypass. The user can assert this field to bypass the PLL lock signal when re-locking the PLL in the bypass mode (DFS) or when the PLL lock signal cannot be used. 0: use the PLL lock to gate the PHY clocks to prevent clock glitch 1: bypass the PLL lock (do not use the PLL lock signal to gate the PHY clocks)
[30:13]	RO	reserved	Reserved.
[12]	RW	dx_phgated_men	PHY phase clock gated manual control enable. This field takes effect only when dx_phgated_en is 1'b0. If dx_phgated_en is high and this field is high, the user can use dx_phclkgated to manually control the clock gating of the PHY phase clock. 0: disabled 1: enabled
[11]	RW	dx_phclkgated	PHY phase clock gated control. This field takes effect only when dx_phgated_en is 1'b0. If dx_phgated_en is '1b1, this field is used, and the gated function is automatically controlled by PACK FSM. 0: The clock is disabled. 1: The clock is enabled.
[10]	RW	dx_phgated_en	PHY phase clock gated function (automatically controlled by PACK FSM) enable. 0: disabled 1: enabled
[9]	RW	ck_phy_clkgated	Dedicated clock gated control for the output CK and related circuits. 0: The clock is gated. 1: The clock is enabled. **NOTE** This field is automatically set to 1 when the PLL is locked without error.

[8]	RW	ac_phy_clkgated	Clock gated for the circuits in AC block except CK and CK related circuits. 0: The clock is gated. 1: The clock is enabled. **NOTE** This field is automatically set to 1 when the PLL is locked without error.
[7:4]	RO	reserved	Reserved.
[3:0]	RW	dx_phy_clkgated	Clock gated for circuits in data blocks. 0: The clock is gated. 1: The clock is enabled. **NOTE** This field is automatically set to 1 when the PLL is locked without error.

PHYTIMER0

PHYTIMER0 is a PHY timing parameter register. The timing parameters are required by the PHY.

Offset Address	Register Name	Total Reset Value
0x010	PHYTIMER0	0x2710_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_dram_cke_high																				reserved				t_dram_reset							
Reset	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RW	t_dram_cke_high	DRAM CKE high initialization. This field specifies the number of PCLK clock cycles of the first DRAM command from CKE pulled to high (LPDDR2/LPDDR3 tINIT3).
[11:8]	RO	reserved	Reserved.
[7:0]	RW	t_dram_reset	DDR3 DRAM reset. This field is used to specify the time issuing reset signaling to the DRAM (number of PCLK clock cycles).

PHYTIMER1

PHYTIMER1 is a DRAM CKE low initialization register.

Offset Address	Register Name	Total Reset Value
0x014	PHYTIMER1	0x0000_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																t_dram_cke_low															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	t_dram_cke_low	DRAM CKE low initialization. This field specifies the number of PCLK clock cycles during which CKE should be kept low after power is reset and the clock is stable.

PLLCTRL

PLLCTRL is a timing parameter register for the PLL in both address/command and data block.

Offset Address	Register Name	Total Reset Value
0x018	PLLCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										pll_freq_range		reserved		pll_pwdn		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.
[5:4]	RW	pll_freq_range	PLL frequency range select. This field specifies the frequency input range of the PLLs.
[3]	RO	reserved	Reserved.
[2:0]	RW	pll_pwdn	PLL power down. This field is used to set the power-down status of the PLL input. If this field is set to 1, the PLL power-down pin is activated. Writing 0 to this field will remove the deactivated PLL power down pin. Bit[2] for AC PLL Bit[1] for DX1 (DATA1) PLL Bit[0] for DX0 (DATA0) PLL

PLLTIMER

PLLTIMER is a PLL address/command and data block control register.

Offset Address	Register Name	Total Reset Value
0x01C	PLLTIMER	0x4E20_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_pll_lock																reserved								t_pll_rst							
Reset	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	t_pll_lock	PLL lock time. This field specifies the number of PCLK clock cycles waiting for the PLL to be locked.
[15:8]	RO	reserved	Reserved.
[7:0]	RW	t_pll_rst	PLL reset time. This field specifies the number of PCLK clock cycles to issue reset to the PLL.

DLYMEASCTRL

DLYMEASCTRL is a read delay line delay measurement control register.

Offset Address	Register Name	Total Reset Value
0x020	DLYMEASCTRL	0x0000_0471

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dly_track_limit								reserved	phy_autoref_en	dynamic_dqsen	dynamic_dqsgen	dynamic_dqsgth		dly_track_type	dly_meas_type
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	0	0	1

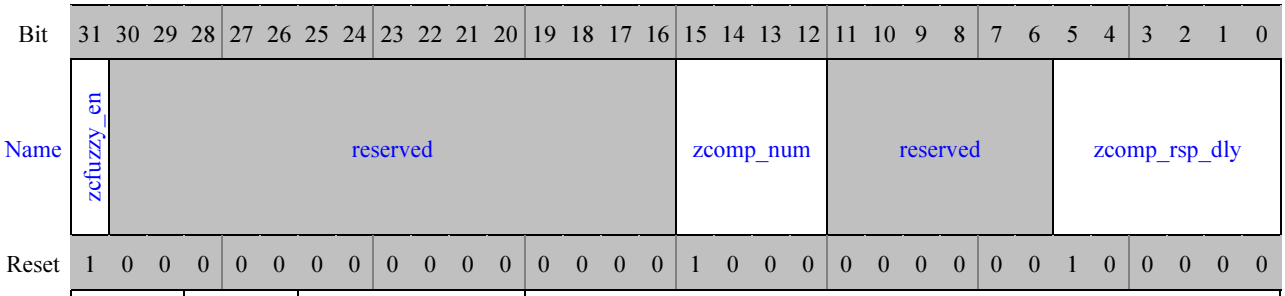
Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved.
[14:8]	RW	dly_track_limit	Delay tracking limit. This field specifies the maximum number of accumulated taps allowed while dynamic tracking.
[7]	RO	reserved	Reserved.

[6]	RW	phy_autoref_en	PHY auto-refresh tracking enable.
[5]	RW	dynamic_dqsen	Dynamic DQS tracking enable. This field should be set to high during delay measurement.
[4]	RW	dynamic_dqsgen	Dynamic DQSG tracking enable.
[3:2]	RW	dynamic_dqsgth	Dynamic DQSG update threshold. This field specifies the number of taps accumulated before the RDQSG delay line is updated. 0: update every 4 times 1: update every 2 times 2 or 3: update each time
[1]	RW	dly_track_type	Delay tracking type. This field specifies whether priority updated from the PHY is used during dynamic tracking. If this field is set to 1, the priority updated from the PHY is used.
[0]	RW	dly_meas_type	Delay measurement type. This field specifies whether the delay measurement is for one clock cycle or half a clock cycle. If this field is set to 1, a full clock cycle is measured.

IMPCTRL

IMPCTRL is a ZQ calibration control register.

Offset Address	Register Name	Total Reset Value
0x024	IMPCTRL	0x8000_8020



Bits	Access	Name	Description
[31]	RW	zcfuzzy_en	ZQ comparator result selection by weighted method. When this function is disabled, the precision is improved but ZQ comparison may fail. When this function is enabled, ZQ comparison is successful. 0: disabled 1: enabled (default)
[30:16]	RO	reserved	Reserved.

[15:12]	RW	zcomp_num	ZQ comparator iteration time. This field specifies the iteration time of zcomp changing detection.
[11:6]	RO	reserved	Reserved.
[5:0]	RW	zcomp_rsp_dly	ZQ comparator response time. This field specifies the delay of the zcomp result after zctrl is used.

IMPSTATUS

IMPSTATUS is a ZQ calibration status register.

Offset Address	Register Name	Total Reset Value
0x028	IMPSTATUS	0x0020_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				zcode_pdrv_cal				pdrv_cal_result	reserved			zcode_pdrv				reserved				zcode_ndrv_cal				ndrv_cal_result	reserved			zcode_ndrv			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30:24]	RO	zcode_pdrv_cal	P-drive impedance calibration code. This field shows the p-drive calibration code during impedance calibration.
[23]	RO	pdrv_cal_result	P-drive calibration result. This field specifies the ZQ calibration result. The valid values are as follows: 0: calibration done with OK. 1: calibration done with error. Writing 1 to this field clears this field.
[22]	RO	reserved	Reserved.
[21:16]	RW	zcode_pdrv	P-drive impedance control code. This field is used to specify the p-drive impedance control code. This register is updated by the user or is updated each time the ZQ calibration is complete.
[15]	RO	reserved	Reserved.
[14:8]	RO	zcode_ndrv_cal	N-drive impedance calibration code. This field shows the n-driver calibration code during impedance calibration.

[7]	RO	ndrv_cal_result	N-drive calibration result. This field specifies the ZQ calibration result. The valid values are as follows: 0: calibration done with OK. 1: calibration done with error Writing 1 to this field clears this field.
[6]	RO	reserved	Reserved.
[5:0]	RW	zcode_ndrv	N-drive impedance control code. This field is used to specify the n-drive impedance control code. This register is updated by the user or is updated each time the ZQ calibration is complete.

DRAMCFG

DRAMCFG is a DRAM system configuration register.

Offset Address	Register Name	Total Reset Value
0x02C	DRAMCFG	0x0000_0405

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					lpddr23_zqc_en	lpddr23_mrw1617_en	lpddr23_pre_en	reserved	maddr_mir	ma2t	nosra	reserved	dcfg_type		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved.
[10]	RW	lpddr23_zqc_en	LPDDR2/LPDDR3 initialization ZQC (init) enable. 0: disabled 1: issue ZQC(init) commands during initialization sequence rank by rank (default).
[9]	RW	lpddr23_mrw1617_en	LPDDR2/LPDDR3 initialization MRW16/17 enable. 0: disabled (default) 1: issue MRW16 then MRW17 commands during initialization sequence

[8]	RW	lpddr23_pre_en	LPDDR2/LPDDR3 initialization precharge all enable. 0: disabled (default) 1: issue the precharge all command before the reset command during initialization sequence
[7]	RO	reserved	Address mirroring. This bit should be set to 0 in single rank configuration
[6]	RW	maddr_mir	Address mirroring. This bit should be set to 0 in single rank configuration
[5]	RW	ma2t	Two cycles on address/command. This field specifies whether the 2T timing should be used by the PHY controller that internally generates the DRAM command.
[4]	RW	nosra	No simultaneous rank access. This field specifies whether simultaneously rank access in the same clock cycle is allowed. If it set to 1, the rank access will be taken in turn. Note that this field can be enabled only when the number of ranks is 2 or 4. This field should be set to 0 in single rank configuration
[3]	RO	reserved	Reserved.
[2:0]	RW	dcfg_type	DRAM type selection. This field specifies the DDR RAM type. The valid values are as follows: 010: DDR3 101: LPDDR2/LPDDR3 Other values: reserved

DRAMTIMER0

DRAMTIMER0 is a DRAM timing parameter register.

NOTE

The command delay specified in this register applies only to the command issued by the PHY controller internally.

Offset Address	Register Name	Total Reset Value
0x030	DRAMTIMER0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	t_rc	t_rrd	t_ras	t_rcd	t_rp	t_wtr	t_rtp	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RW	t_rc	Activated to activated on same bank command delay.

[25:22]	RW	t_rrd	Activated to activated on different bank command delay.
[21:16]	RW	t_ras	Activated to precharge command delay.
[15:12]	RW	t_rcd	Activated to read/write delay.
[11:8]	RW	t_rp	Precharge command period. The unit is two clock cycles.
[7:4]	RW	t_wtr	Write to read command delay.
[3:0]	RW	t_rtp	Read to precharge command delay.

DRAMTIMER1

Offset Address	Register Name	Total Reset Value
0x034	DRAMTIMER1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		t_rtw						t_rfc								reserved		t_faw						t_mod				t_mrd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:25]	RW	t_rtw	Read to write command delay. This field specifies whether to insert extra cycles between read and write commands to compensate tdqsck. This value should be 3 for the common condition when DDR3 is used. This value should be 6 for the common condition when LPDDR2/LPDDR3 is used.
[24:16]	RW	t_rfc	Refresh to refresh command delay.
[15]	RO	reserved	Reserved.
[14:9]	RW	t_faw	Four-bank activated period. This field applies only to the 8-bank device.
[8:4]	RW	t_mod	Load mode register to non load mode register command delay. This field is used as max (t_mod, t_mrd) in DDR3, max (t_mrw, tmrd) in LPDDR3, and t_mrw in LPDDR2.
[3:0]	RW	t_mrd	Load mode register to load mode register command delay. Not used.

DRAMTIMER2

Offset Address	Register Name	Total Reset Value
0x038	DRAMTIMER2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_ccd	reserved	t_dllk										t_cke				reserved	t_xp							t_xs							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	t_ccd	Read to read and write to write command delay. 0 = BL/2 (for DDR3, this value should be 4) 1 = BL/2 + 1 (for DDR3, this value should be 5)
[30]	RO	reserved	Reserved.
[29:20]	RW	t_dllk	DLL lock time.
[19:16]	RW	t_cke	CKE minimum pulse width.
[15]	RO	reserved	Reserved.
[14:10]	RW	t_xp	Power down exit delay.
[9:0]	RW	t_xs	Self refresh exit delay.

DRAMTIMER3

Offset Address	Register Name	Total Reset Value
0x03C	DRAMTIMER3	0x0010_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	t_wr				t_wl				t_init5														t_zcal									
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	t_wr	Write recovery cycle.
[27:24]	RW	t_wl	Write latency (AL + CWL).
[23:10]	RW	t_init5	LPDDR device initialization time. This field specifies the time during which the LPDDR sets the DAI bit to 1.

[9:0]	RW	t_zcal	ZQ calibration to command delay. This field specifies the number of clock cycles to wait after initial ZQ calibration. For DDR3 ZQ normal operation full calibration, this value is divided by 2. For DDR3 ZQ initialization calibration, this value is divided by 4. For LPDDR2/3, this field specifies the value of tZQINIT during initialization.

DRAMTIMER4

DRAMTIMER4 is a DRAM write leveling timing parameter register. This register applies only to the DDR3/LPDDR3 SDRAM.

Offset Address	Register Name	Total Reset Value
0x040	DRAMTIMER4	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5 4	3 2 1 0
Name	reserved	t_odton	reserved		t_odt	t_wlo		reserved		t_wlmrd
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	t_odton	ODT turn-on latency (number of cycles from write command to assert of ODT).
[23:16]	RO	reserved	Reserved.
[15:12]	RW	t_odt	ODT turn-on cycles.
[11:7]	RW	t_wlo	Write leveling output delay. This field specifies the write leveling output delay in cycles (dficlk cycle).
[6]	RO	reserved	Reserved.
[5:0]	RW	t_wlmrd	Write leveling mode programmed (load mode register) to first DQS/DQS# rising edge delay (dficlk cycle).

ODTCR

ODTCR is a rank ODT control register while reading or writing to particular ranks.

Offset Address	Register Name	Total Reset Value
0x044	ODTCR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																wodt_rank3				wodt_rank2				wodt_rank1				wodt_rank0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:12]	RW	wodt_rank3	Write rank 3 ODT control. This field specifies the ODT issued while write on rank 3. The valid bit width is the number of ranks.
[11:8]	RW	wodt_rank2	Write rank 2 ODT control. This field specifies the ODT issued while write on rank 2. The valid bit width is the number of ranks.
[7:4]	RW	wodt_rank1	Write rank 1 ODT control. This field specifies the ODT issued while write on rank 1. The valid bit width is the number of ranks.
[3:0]	RW	wodt_rank0	Write rank 0 ODT control. This field specifies the ODT issued while write on rank 0. The valid bit width is the number of ranks.

TRAINCTRL0

TRAINCTRL0 is a training control register.

Offset Address	Register Name	Total Reset Value
0x048	TRAINCTRL0	0xD044_1080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_eye_opening	dtrerrstop	gtds_rspdly						dqsg_cstep		dqsgrt_chk						dqsgrt_shft				dqsgsl_mrgn								dtr_rank			
Reset	1	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	skip_eye_opening	Skip eye opening of data eye training. This field specifies whether the eye opening should be skipped. If this field is set to 1, the eye opening before data eye training is skipped. If this field is set to 0, the eye opening is executed before data eye training.
[30]	RW	dtrerrstop	Data training error stop. This field controls whether the data training is terminated if an error occurs. The data training is stopped if this bit is set to 1. If this bit set to 0, the training will continue even an error occurs. The error status is recorded no matter when this field is set to 0 or 1.
[29:24]	RW	gtds_rspdly	Gate/Read latch training response delay. This field specifies the waiting time to check the response from PHY while gate and read latch training is performed (dficlk cycle).
[23:22]	RW	dqsg_cstep	Gate training coarse tuning step (the unit is phase). The recommended values are 0x0−0x2. 2'd0: step = 1 2'd1: step = 2 (default) 2'd2: step = 3 2'd3: step = 4
[21:16]	RW	dqsgrt_chk	Gate retraining check window. This field specifies the delta value to be checked during gate retraining check. The delta is added/subtracted to/from the read DQS gate. This position is checked to determine whether gating phase adjustment is required. The phase movement is the configured value multiple by 2. Note that 3'b000 is reserved and should not be used. The recommended values are 0x1−0x3.

[15:10]	RW	dqsgrt_shft	Gate retraining shift window. This field specifies the value to be shifted if gate phase adjustment is required after gate retraining checks. The phase movement is the configured value multiple by 2. Note that 3'b000 is reserved and should not be used. The recommended value is dqsgrt_chk.
[9:4]	RW	dqsgsl_mrgn	Read DQS gate margin. This field specifies the margin to be reserved after the DQS gate training. The number of phases specified in this field is decreased to create DQS gating margin. The valid values are as follows: 6'b00100: 1/4 cycle 6'b01000: 1/2 cycle (recommended) 6'b01100: 3/4 cycle 6'b10000: 1 cycle Other values: reserved
[3:0]	RW	dtr_rank	Training rank. This field specifies the rank used for training. After the training, this field is used to select the source of rank specific settings.

RANKEN

RANKEN is a training rank control register.

Offset Address	Register Name	Total Reset Value
0x04C	RANKEN	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rank_en															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	rank_en	Training rank enable. This field specifies whether the dtr_rank is enabled. 0: disabled 1: enabled (default) Bit 0 indicates rank 0. Bit 1 indicates rank 1. ... Bit 15 indicates rank 15. The maximum number of ranks is specified by the system.

TRAINMADDR

TRAINMADDR is a data training memory start address register. The minimum space required for the data training is 64 bytes, and the allocated memory must be 64-byte-aligned.

Offset Address	Register Name	Total Reset Value
0x0050	TRAINMADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dtrow																dtcol												reserved	dtbank		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	dtrow	Data training row address. This field is used to configure the memory row address required for the data training.
[15:4]	RW	dtcol	Data training column address. This field is used to configure the column address required for the data training. The field should be 0.
[3]	RO	reserved	Reserved.
[2:0]	RW	dtbank	Data training bank address. This field is used to configure the memory bank address required for the data training.

BISTCTRL

BISTCTRL is a BIST behavior register.

Offset Address	Register Name	Total Reset Value
0x0054	BISTCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bist_fail_stop								reserved						bist_pat		reserved		bist_mode			reserved		bist_op
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	bist_fail_stop	BIST stop error count. This field specifies the number of failures at which the BIST should be stopped. If this field is set to 0x00, the BIST will run infinite until the BIST operation is stopped or reset. If a non-zero value is specified, the BIST is stopped while the accumulated errors reach the count specified in this field.
[15:10]	RO	reserved	Reserved.
[9:8]	RW	bist_pat	BIST pattern generation. This field specifies the BIST pattern generated for test. Note that bist_pat can be changed only when bist_done is 1. 00: walking 0 01: walking 1 10: LFSR-based random generation 11: user programmed
[7]	RO	reserved	Reserved.
[6:4]	RW	bist_mode	BIST mode select. This field specifies the BIST mode. The valid values are as follows: 000: pattern generated only 100: loopback before output buffer 101: loopback after output buffer 110: DRAM read/write mode Other values: reserved Note that bist_mode can be changed only when bist_done is 1. When the data loopback mode is selected, swapwl_en/swap_en must be set to all zeros (no swap).
[3:2]	RO	reserved	Reserved.

[1:0]	RW	bist_op	During Reg write, this field is used for selecting the BIST operation. The valid values are as follows: 00: BIST stop 01: BIST run 10: BIST reset 11: reserved Writing the Reset clears all the status registers, and this field is cleared to BIST Stop. During Reg read, this field is for BIST active status (only bit 0 is valid, and bit1 is read as 1'b0). 0: BIST inactive 1: BIST active

BISTDATA0

BISTDATA0 is DRAM loopback test BIST data register 0.

NOTE

This register is valid only when bist_pat is set to "User Defined."

Offset Address	Register Name	Total Reset Value
0x0058	BISTDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bist_data_b3								bist_data_b2								bist_data_b1								bist_data_b0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	bist_data_b3	BIST data byte 3. This field is used as the fourth beat of burst during BIST test
[23:16]	RW	bist_data_b2	BIST data byte 2. This field is used as the third beat of burst during BIST test.
[15:8]	RW	bist_data_b1	BIST data byte 1. This field is used as the second beat of burst during BIST test.
[7:0]	RW	bist_data_b0	BIST data byte 0. This field is used as the first beat of burst during BIST test.

BISTDATA1

BISTDATA1 is DRAM loopback test BIST data register 1.

Offset Address	Register Name	Total Reset Value
0x005C	BISTDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bist_data_b7								bist_data_b6								bist_data_b5								bist_data_b4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	bist_data_b7	BIST data byte 7. This field is used as the eighth beat of burst during BIST test
[23:16]	RW	bist_data_b6	BIST data byte 6. This field is used as the sixth beat of burst during BIST test.
[15:8]	RW	bist_data_b5	BIST data byte 5. This field is used as the fifth beat of burst during BIST test.
[7:0]	RW	bist_data_b4	BIST data byte 4. This field is used as the fourth beat of burst during BIST test.

BISTSTATUS

BISTSTATUS is a BIST test result and status register.

Offset Address	Register Name	Total Reset Value
0x0060	BISTSTATUS	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													bist_dxerr	bist_acerr	bist_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2]	RO	bist_dxerr	BIST error on DX blocks. This bit shows whether any error occurs on the DXn during BIST test.
[1]	RO	bist_acerr	BIST error on AC block. This bit shows whether any error occurs on the AC during BIST test.

[0]	RO	bist_done	BIST done. This field shows whether the BIST is complete. Note that if the BIST Stop Error Count field (bist_fail_stop) is set to 0, this field is never asserted.

MODEREG01

MODEREG01 is mode register content register 1.

Offset Address	Register Name	Total Reset Value
0x0064	MODEREG01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mr1																mr0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mr1	Mode register 1. For DDR/DDR2/DDR3/LPDDR, this field specifies the content of extend mode register 1. For LPDDR2/LPDDR3, this field defines the content of MR3/MR9 (mode register). bit[31:24]: MR9 OP bit[23:16]: MR3 OP
[15:0]	RW	mr0	Mode register 0. For DDR/DDR2/DDR3/LPDDR, this field specifies the content of mode register 0. For LPDDR2/LPDDR3, this field defines the mode registers MR1/MR2. bit[15:8]: MR2 OP bit[7:0]: MR1 OP

MODEREG23

MODEREG23 is mode register content register 2.

Offset Address	Register Name	Total Reset Value
0x0068	MODEREG23	0xFF0A_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mr3																mr2															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mr3	Mode register 3. For DDR/DDR2/DDR3, this field specifies extend mode register 3. For LPDDR2/LPDDR3, this field is for the ZQ commands. bit[31:24]: OP bit[23:16]: MA The ZQ commands are issued rank by rank after tINIT5. bit[31:24]: MR10 OP bit[23:16]: MR10 MA
[15:0]	RW	mr2	Mode register 2. For DDR/DDR2/DDR3, this field specifies extend mode register 2. For LPDDR2/LPDDR3, this field specifies MR16/MR17. bit[15:8]: MR17 OP bit[7:0]: MR16 OP

DETPATTERN

DETPATTERN is a write/read DET pattern register.

NOTE

These fields are used to fine-tune the training procedure. You are advised not to modify them.

Offset Address	Register Name	Total Reset Value
0x006C	DETPATTERN	0x00FF_AA55

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								det_patFF								det_patAA								det_pat55							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RW	det_patFF	DET pattern 2.
[15:8]	RW	det_patAA	DET pattern 1.

[7:0]	RW	det_pat55	DET pattern 0.

MISC

MISC is a miscellaneous control register.

Offset Address	Register Name	Total Reset Value
0x0070	MISC	0x0008_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	swapdfibyte_en		swapwl_en			swapdm_en		swapaddr_en		swap_en		cfg_dlyupd	addr_delay	swap_en_msb	addr_toggle	scramb_en	reserved				cfg_rl				reserved				cfg_wl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	swapdfibyte_en	Swap DFI byte lane. 00: no swap 01: swap
[29:27]	RW	swapwl_en	Swap WL/CA result. 000: no swap 001: swap 1 010: swap 2 011: swap 3 100: swap 4 Note: When the data BIST loopback mode is selected, this field must be set to 0x0.
[26:25]	RW	swapdm_en	Swap DM bus. 00: no swap 01: 16-bit T2 swap
[24:23]	RW	swapaddr_en	Swap address bus. 00: no swap 01: 32-bit flyby-4, flyby-2 swap 10: 16-bit T-2 swap

[22:21]	RW	swap_en	Swap DQ bus bit[1:0]. 000: no swap 001: swap 1 010: swap 2 011: swap 3 100: swap 4 NOTE When the data BIST loopback mode is selected, this field must be set to 0x0.
[20]	RW	cfg_dlyupd	Transparent mode for the delay update module. When this bit is set to 1, the delay setting in registers are applied to the PHY immediately.
[19]	RW	addr_delay	Add 1-T delay on address/command. This bit must be set to 1 when CWL is 5.
[18]	RW	swap_en_msb	Swap DQ bus bit[2]. 000: no swap 001: swap 1 010: swap 2 011: swap 3 100: swap 4 NOTE When the data BIST loopback mode is selected, this field must be set to 0x0.
[17]	RW	addr_toggle	Toggle address bus every clock cycle. This bit is set to 1 only for the burn-in test.
[16]	RW	scramb_en	Data scrambler enable. Set this field to 1 to enable data scramble function
[15:12]	RO	reserved	Reserved.
[11:7]	RW	cfg_rl	PHY read latency. It defines the number of cycles from read command to assert of rddata_en and is equal to CL + AL − 2 (for LPDDR2/3, the field should be RL-2).
[6:5]	RO	reserved	Reserved.
[4:0]	RW	cfg_wl	PHY write latency. It defines the number of cycles from write command to assert of wrdata_en and is equal to CWL + AL − 1 (for LPDDR2/3, the field should be WL + 1). If the DFI clock ratio is 1:2, cfg_wl must be greater than or equal to 2.

RNK2RNK

RNK2RNK is a rank-to-rank delay control register.

Offset Address	Register Name	Total Reset Value
0x0074	RNK2RNK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												trnkwtr				trnkrtw				trnkrtr				trnkwtw							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved.
[19:15]	RW	trnkwtr	Delay from write to read command targeted to different ranks.
[14:10]	RW	trnkrtw	Delay from read to write command targeted to different ranks.
[9:5]	RW	trnkrtr	Delay from read to read command targeted to different ranks.
[4:0]	RW	trnkwtw	Delay from write to write command targeted to different ranks.

PHYCTRL0

PHYCTRL0 is PHY control register 0.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x0078	PHYCTRL0	0x0000_3980

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		resetoen	csoen	ckeoen	ckoen				cmdoen	reserved			lp_ck_sel	sel_pos_rx	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13]	RW	resetoen	Set this field to default value.
[12]	RW	csoen	Set this field to default value.
[11]	RW	ckeoen	Set this field to default value.
[10:8]	RW	ckoen	Set this field to default value.
[7]	RW	cmdoen	Set this field to default value.

[6:5]	RO	reserved	Set this field to default value.
[4:3]	RW	lp_ck_sel	Set this field to default value.
[2]	RW	sel_pos_rx	PHY output trigger edge select. 0: falling edge 1: rising edge
[1:0]	RO	reserved	Reserved.

PHYDBG

PHYDBG is a PHY debug register.

Offset Address	Register Name	Total Reset Value
0x007C	PHYDBG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dqsb_gated_error								reserved								dqs_gated_error							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RO	dqsb_gated_error	DQSN gated error flag. This error flag can be cleared only by issuing PHY reset.
[15:8]	RO	reserved	Reserved.
[7:0]	RO	dqs_gated_error	DQS gated error flag. This error flag can be cleared only by issuing PHY reset.

RETCTRL0

RETCTRL0 is a retraining control register.

Offset Address	Register Name	Total Reset Value
0x0080	RETCTRL0	0x0001_2400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	retrain_thrd																reserved	gtrten	retrain_en	phyupd_resp												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	retrain_thrd	Retraining threshold. The PHY counts the number of AREFs issued by MC. When the number reaches the threshold, the retraining operation is triggered to be started. Only a non-zero value is valid.
[15]	RO	reserved	Reserved.
[14]	RW	gtrten	Gate retraining active. This field controls whether the gate retraining is executed during retraining on-going. This field should be asserted only after the initial gate training is complete.
[13]	RW	retrain_en	PHY retraining enable. This field controls whether the PHY is enabled to request memory controller for retraining.
[12:0]	RW	phyupd_resp	PHY update response latency. When the PHY asserts dfi_phyupd_req to MC, MC should assert dfi_phyupd_ack no later than the number of cycles configured by the response latency.

DMSEL

DMSEL is a DM swap selection register.

Offset Address	Register Name	Total Reset Value
0x0084	DMSEL	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dxctl_dmswap_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	dxctl_dmswap_sel	bit[3:2]: DM1 swap select bit[1:0]: DM0 swap select

IOCTL

IOCTL is an I/O control register.

Offset Address	Register Name	Total Reset Value
0x0088	IOCTL	0x4BFF_F801

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	odtsel_dqs				odtsel				ronsel_ck				ronsel_ac2t				ronsel_ac1t				ronsel_dqs				ronsel				reserved								aciopldn	dxiopldn	diff_dqs_en	
Reset	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:29]	RW	odtsel_dqs	Set this field to default value.
[28:26]	RW	odtsel	Set this field to default value.
[25:23]	RW	ronsel_ck	Set this field to default value.
[22:20]	RW	ronsel_ac2t	Set this field to default value.
[19:17]	RW	ronsel_ac1t	Set this field to default value.
[16:14]	RW	ronsel_dqs	Set this field to default value.
[13:11]	RW	ronsel	Set this field to default value.
[10]	RO	reserved	Set this field to default value.
[9:3]	RO	reserved	Reserved.
[2]	RW	aciopldn	Set this field to default value.
[1]	RW	dxiopldn	Set this field to default value.
[0]	RW	diff_dqs_en	Differential DQS enable.

DQSSEL

DQSSEL is a PHY DQ swap register.

Offset Address	Register Name	Total Reset Value
0x008C	DQSSEL	0xFF00_FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dqswap_sel																															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dqswap_sel	DQ swap in PHY. Each bit determines the relative DQS with DQ. 0: relative to DQS0 1: relative to DQS1

PHYCTRL1

PHYCTRL1 is an AC PHY control register.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x0090	PHYCTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ac_pll_cal	ac_pll_calm	ac_pll_calt	ac_pll_lt	ac_pll_sp			ac_pll_cpi				ac_pll_init	ac_pll_testen	ac_pll_testpem	ac_pll_thrm	reserved																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved.
[30]	RW	ac_pll_cal	The value 0x0 is recommended.
[29]	RW	ac_pll_calm	The value 0x0 is recommended.
[28]	RW	ac_pll_calt	The value 0x0 is recommended.
[27:26]	RW	ac_pll_lt	The value 0x0 is recommended.
[25:23]	RW	ac_pll_sp	The value 0x2 is recommended.
[22:20]	RW	ac_pll_cpi	The value 0x4 is recommended.
[19]	RW	ac_pll_init	The value 0x0 is recommended.
[18]	RW	ac_pll_testen	The value 0x0 is recommended.

[17]	RW	ac_pll_testpem	The value 0x0 is recommended.
[16]	RW	ac_pll_thrm	The value 0x0 is recommended.
[15:0]	RO	reserved	Reserved.

DXNCKCTRL

DXNCKCTRL is a PLL phase selection (within the PHY) register. You are advised not to modify this register.

Offset Address	Register Name	Total Reset Value
0x0094	DXNCKCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dx_ckd2				dx_ck0p_mclk			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved.
[5:3]	RW	dx_ckd2	Set this field to default value.
[2:0]	RW	dx_ck0p_mclk	Set this field to default value.

PHYPLLCTRL_AC

PHYPLLCTRL_AC is PHY PLL control register 1.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x0098	PHYPLLCTRL_AC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ac_pll_lock	reserved																							ac_pll_test							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	ac_pll_lock	AC PLL lock signal. 0: not locked 1: locked
[30:8]	RO	reserved	Reserved.
[7:0]	RW	ac_pll_test	AC PLL test mode. 0: normal mode 1: test mode

PHYPLLCTRL_DX

PHYPLLCTRL_DX is PHY PLL control register 2.

Offset Address	Register Name	Total Reset Value
0x009C	PHYPLLCTRL_DX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dx_pll_lock				reserved												dx_pll_test															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	dx_pll_lock	ND: number of data PHY blocks DX PLL lock signals for each byte lane 0: not locked 1: locked
[27:16]	RO	reserved	Reserved.
[15:0]	RW	dx_pll_test	PLL test for 16-bit data block bit[7:0]: 16-bit block 0 bit[15:8]: 16-bit block 1

SWTMODE

SWTMODE is an S/W training mode register.

Offset Address	Register Name	Total Reset Value
0x00A0	SWTMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wl_wdqs_gated	reserved																													sw_gtmode	sw_wlmode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wl_wdqs_gated	Write leveling WDQS strobe disable when the related PH/BDL is tuned to prevent glitch. 0: not gated 1: gated (disable WDQS strobe)
[30:2]	RO	reserved	Reserved.
[1]	RW	sw_gtmode	Set this bit to 1 when performing S/W gate training or GDS training.
[0]	RW	sw_wlmode	Set this bit to 1 when performing S/W write leveling training.

SWTWLDQS

SWTWLDQS is a write DQS issue register during S/W write leveling training.

Offset Address	Register Name	Total Reset Value
0x00A4	SWTWLDQS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sw_wl_dqs
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.

[0]	WO	sw_wl_dqs	Writing 1 to this bit once issues one DQS pulse from the PHY to DRAM.

SWTRLT

SWTRLT is an S/W training result register.

Offset Address	Register Name	Total Reset Value
0x00A8	SWTRLT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								gds_result								gt_result								wl_dq_result							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved.
[23:16]	RO	gds_result	Each bit corresponds to one byte lane.
[15:8]	RO	gt_result	Each bit corresponds to one byte lane.
[7:0]	RO	wl_dq_result	Each bit corresponds to one byte lane.

PHYCTRL2

PHYCTRL2 is PHY control register 2.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x00AC	PHYCTRL2	0x0000_000B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											phy_dyn_pupden	phy_dummypad_use	phy_odten_gated	phy_gateidc	phy_dqsgerror
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4]	RW	phy_dyn_pupden	DATA16BIT_blk.reg_dynamic_PUPDEN_16b control.

[3]	RW	phy_dummypad_use	DATA16BIT_blk.reg_dummypad_use control.
[2]	RW	phy_odten_gated	DATA16BIT_blk.reg_ODTEN_Gated control.
[1]	RW	phy_gatetdc	DATA16BIT_blk.BUFRESETCONTN_gated_TDC control.
[0]	RW	phy_dqsgerror	DATA16BIT_blk.BUFRESETCONTN_gated_DQSGERROR control.

IOCTL1

IOCTL1 is I/O PHY control register 1.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x00B0	IOCTL1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ioctl_squeach_pd	reserved	ioctl_genvref_pd		ioctl_genvref_ie		ioctl_popmode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved.
[27:24]	RW	ioctl_squeach_pd	Set this field to default value.
[23:18]	RO	reserved	Reserved.
[17:12]	RW	ioctl_genvref_pd	Set this field to default value.
[11:6]	RW	ioctl_genvref_ie	Set this field to default value.
[5:0]	RW	ioctl_popmode	Set this field to default value.

IOCTL2

IOCTL2 is I/O PHY control register 2.

NOTE

Register in this field are connected to PHY interface directly

Offset Address	Register Name	Total Reset Value
0x00B4	IOCTL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		ioctl_genvref_refsel_2						ioctl_genvref_refsel_1				ioctl_genvref_refsel_0				ioctl_genvref_rangel_1				ioctl_genvref_rangel_0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved.
[29:24]	RW	ioctl_genvref_refsel_2	Set this field to default value.
[23:18]	RW	ioctl_genvref_refsel_1	Set this field to default value.
[17:12]	RW	ioctl_genvref_refsel_0	Set this field to default value.
[11:6]	RW	ioctl_genvref_rangel_1	Set this field to default value.
[5:0]	RW	ioctl_genvref_rangel_0	Set this field to default value.

BISTTIMER

BISTTIMER is a code update period register during BIST running.

Offset Address	Register Name	Total Reset Value
0x00B8	BISTTIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bstupdt_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

[15:0]	RW	bstupdt_timer	BIST update code timer. This field controls the code update period. If this field is programmed to a non-zero value, the BIST is temporarily stopped, and the internal delay code is updated to the PHY when the timer reaches the configured value. The BIST will continue if the code update is complete. If this field is programmed to zero, the update code mechanism is disabled.

TRAINCTRL1

TRAINCTRL1 is data training control register 1.

Offset Address	Register Name	Total Reset Value
0x00D0	TRAINCTRL1	0xF036_F026

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdet_lbs_en	rdet_ds_en	rdet_rbs_en	rdet_av_en	reserved	rdet_rb_backtap							rdet_samp_num				wdet_lbs_en	wdet_ds_en	wdet_rbs_en	wrdet_av_en	reserved				wdet_rb_backtap				wdet_samp_num			
Reset	1	1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	1	1	1	0	0	0	0	0	0	1	0	0	1	1	0

Bits	Access	Name	Description
[31]	RW	rdet_lbs_en	Read DET left boundary search enable.
[30]	RW	rdet_ds_en	Read DET deskew enable.
[29]	RW	rdet_rbs_en	Read DET right boundary search enable.
[28]	RW	rdet_av_en	Read DET average stage enable
[27]	RO	reserved	Reserved.
[26:20]	RW	rdet_rb_backtap	Read DET right boundary back tap. This field is used to offset (+) the rdqsbdl before the right boundary search is started to overcome meta-sable zone.
[19:16]	RW	rdet_samp_num	Read DET sample number control. The multiple sample is used to overcome the meta situations. Valid value: 1−15
[15]	RW	wdet_lbs_en	Write DET left boundary search enable.
[14]	RW	wdet_ds_en	Write DET deskew enable.
[13]	RW	wdet_rbs_en	Write DET right boundary search enable.
[12]	RW	wrdet_av_en	Write DET average stage enable.

[11:8]	RO	reserved	Reserved.
[7:4]	RW	wdet_rb_backtap	Write DET right boundary back tap. This field is used to offset (−) the wdqphase before the right boundary search is started to overcome meta-sable zone.
[3:0]	RW	wdet_samp_num	Write DET sample number control. The multiple sample is used to overcome the meta situations. Valid value: 1−15

TRAINCTRL2

TRAINCTRL2 is data training control register 2.

Offset Address	Register Name	Total Reset Value
0x00D4	TRAINCTRL2	0x0000_CC55

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdet_method_sel	mrr_pat_order			mrr_bl4	reserved		gds_automrg_en	mrr_pat_mask								mrr_pat_B								mrr_pat_A							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[31]	RW	rdet_method_sel	Read DET method select. 0: write-then-read 1: MRR32/40 (only for LPDDR3)
[30:28]	RW	mrr_pat_order	MRR pattern order. If MRR is used in the read DET, PACK will issue three MRR commands. The order is indicated by bit 2 -> bit 1 -> bit 0. 0: MRR32 1: MRR40
[27]	RW	mrr_bl4	MRR burst 4 indicator. If MRR is used in the read DET, PACK needs to know whether MRR burst is 4 (LPDDR2) or 8 (LPDDR3). 0: MRR32/40 burst length = 8 (default) 1: MRR32/40 burst length = 4
[26:25]	RO	reserved	Reserved.
[24]	RW	gds_automrg_en	GDS training/retraining auto tuning enable. 0: disable GDS auto margin tuning (will increase GDS when GDS training/retraining is complete) 1: enable GDS auto margin tuning (default)

[23:16]	RW	mrr_pat_mask	MRR pattern mask. 0: not masked 1: masked (does not compare data)
[15:8]	RW	mrr_pat_B	MRR40 pattern. This field should comply with the LPDDR2/LPDDR3 specifications.
[7:0]	RW	mrr_pat_A	MRR32 pattern. This field should comply with the LPDDR2/LPDDR3 specifications.

REGBANKCTRL

REGBANKCTRL is register bank control register.

Offset Address	Register Name	Total Reset Value
0x00D8	REGBANKCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														op_sel	wr_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved.
[1]	RW	op_sel	Register bank select related to DFS. 0: bank 0 for PHY operating 1: bank 1 for PHY operating
[0]	RW	wr_sel	Register bank select related to DFS. 0: bank 0 while APB read/write 1: bank 1 while APB read/write

TRAINCTRL3

TRAINCTRL3 is data training control register 3.

Offset Address	Register Name	Total Reset Value
0x00DC	TRAINCTRL3	0x8002_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exd_gtres_en	reserved														gdsrt_backtap	reserved				rpat_cnt_num_open				reserved				rpat_cnt_num			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	exd_gtres_en	Extended gate result enable. When this field is set as high, the PACK will use additional information (EN_DQSx_regread) to help extend the gate result in the "fine tune stage of gate training" and "gate retraining." 0: disabled 1: enabled (default)
[30:19]	RO	reserved	Reserved.
[18:16]	RW	gdsrt_backtap	GDS retraining back tap. This field controls the number of back taps during GDS retraining. The value range is 1−7. The recommended value range is 1−2.
[15:12]	RO	reserved	Reserved.
[11:8]	RW	rpat_cnt_num_open	RDET pattern length control for eye open. This field is used to set the pattern length for eye open. The same RDET pattern will be extended as the following settings (field value + 1): 0x0: pattern length = 1 0x1: pattern length = 2 ... 0xF: pattern length = 16
[7:4]	RO	reserved	Reserved.
[3:0]	RW	rpat_cnt_num	RDET pattern length control. This field is used to set the pattern length. The same RDET pattern will be extended as the following settings (field value + 1): 0x0: pattern length = 1 0x1: pattern length = 2 ... 0xF: pattern length = 16

ACBISTCTRL0

ACBISTCTRL0 is comparison control register 0 while BIST activated.

Offset Address	Register Name	Total Reset Value
0x100	ACBISTCTRL0	0x4000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ac_rdffsel			aclpbk_tg	acbist_en	rst_cmp_mask	cs_cmp_mask				ras_cmp_mask	cas_cmp_mask	we_cmp_mask	ba_cmp_mask			addr_cmp_mask															
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	ac_rdffsel	AC loopback read latch select.
[28]	RW	aclpbk_tg	AC loopback toggle control. The user should not modify this bit. It is related to the analog PHY design. 0: 28LPP PHY (default) 1: 40PHY
[27]	RW	acbist_en	BIST enable. This field specifies whether the AC block is included for loopback test while bist_op is set to BIST Enable.
[26]	RW	rst_cmp_mask	RST loopback compare mask. This field controls whether the comparison of the loopback data on the RST bit is disabled. 0: not compared 1: compared
[25:22]	RW	cs_cmp_mask	CS loopback compare mask. This field controls whether the comparison of the loopback data on the CS bits is disabled. 0: not compared 1: compared
[21]	RW	ras_cmp_mask	RAS loopback compare mask. This field controls whether the comparison of the loopback data on RAS is disabled. 0: not compared 1: compared

[20]	RW	cas_cmp_mask	CAS loopback compare mask. This field controls whether the comparison of the loopback data on CAS is disabled. 0: not compared 1: compared
[19]	RW	we_cmp_mask	Write enable loopback compare mask. This field controls whether the comparison of the loopback data on WE is disabled. 0: not compared 1: compared
[18:16]	RW	ba_cmp_mask	Bank address loopback compare mask. This field controls whether the comparison of the loopback data on bank address bits is disabled. 0: not compared 1: compared
[15:0]	RW	addr_cmp_mask	Memory address loopback compare mask. This field controls whether the comparison of the loopback data on address bits is disabled. 0: not compared 1: compared

ACBISTCTRL1

ACBISTCTRL1 is comparison control register 1 while BIST activated.

Offset Address	Register Name	Total Reset Value
0x104	ACBISTCTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ac_lfsr_seed								cke_cmp_mask				odt_cmp_mask			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	ac_lfsr_seed	LFSR seed value. This field specifies the initial seed value of the LFSR generator to this byte lane.

[7:4]	RW	cke_cmp_mask	CKE loopback compare mask. This field controls whether the comparison of the loopback data on CKE bits is disabled. 0: not compared 1: compared
[3:0]	RW	odt_cmp_mask	ODT loopback compare mask. This field controls whether the comparison of the loopback data on ODT bits is disabled. 0: not compared 1: compared

ACBISTSTS0

ACBISTSTS0 is BIST test result and status register 0.

NOTE

This register is read-only, and can only be reset by setting bist_op to BIST Reset.

Offset Address	Register Name	Total Reset Value
0x108	ACBISTSTS0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	rst_bist_err, cs_bist_err	ras_bist_err, cas_bist_err	we_bist_err, ba_bist_err	addr_bist_err			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved.
[26]	RO	rst_bist_err	BIST error on RST.
[25:22]	RO	cs_bist_err	BIST error on CS.
[21]	RO	ras_bist_err	BIST error on RAS.
[20]	RO	cas_bist_err	BIST error on CAS.
[19]	RO	we_bist_err	BIST error on write enable.
[18:16]	RO	ba_bist_err	BIST error on bank address.
[15:0]	RO	addr_bist_err	BIST error on address bus.

ACBISTSTS1

ACBISTSTS1 is BIST test result and status register 1.

NOTE

This register is read-only, and can only be reset by setting bist_op to BIST Reset.

Offset Address	Register Name	Total Reset Value
0x10C	ACBISTSTS1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						cke_bist_err	odt_bist_err
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved.
[7:4]	RO	cke_bist_err	BIST error on CKE.
[3:0]	RO	odt_bist_err	BIST error on ODT.

ACCMDBDL0

ACCMDBDL0 is AC command bit delay line configuration register 0.

Offset Address	Register Name	Total Reset Value
0x120	ACCMDBDL0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			odt1_bdl	reserved			odt0_bdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	odt1_bdl	Bit delay line of ODT1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	odt0_bdl	Bit delay line of ODT0.

ACCMDBDL1

ACCMDBDL1 is AC command bit delay line configuration register 1.

Offset Address	Register Name	Total Reset Value
0x124	ACCMDBDL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												odt3_bdl				reserved												odt2_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	odt3_bdl	Bit delay line of ODT3.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	odt2_bdl	Bit delay line of ODT2.

ACCMDBDL2

ACCMDBDL2 is AC command bit delay line configuration register 2.

Offset Address	Register Name	Total Reset Value
0x128	ACCMDBDL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cs1_bdl				reserved												cs0_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cs1_bdl	Bit delay line of CS1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cs0_bdl	Bit delay line of CS0.

ACCMDBDL3

ACCMDBDL3 is AC command bit delay line configuration register 3.

Offset Address	Register Name	Total Reset Value
0x12C	ACCMDBDL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cs3_bdl				reserved												cs2_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cs3_bdl	Bit delay line of CS3.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cs2_bdl	Bit delay line of CS2.

ACCMDBDL4

ACCMDBDL4 is AC command bit delay line configuration register 4.

Offset Address	Register Name	Total Reset Value
0x130	ACCMDBDL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cke1_bdl				reserved												cke0_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cke1_bdl	Bit delay line of CKE1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cke0_bdl	Bit delay line of CKE0.

ACCMDBDL5

ACCMDBDL5 is AC command bit delay line configuration register 5.

Offset Address	Register Name	Total Reset Value
0x134	ACCMDBDL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cke3_bdl				reserved												cke2_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cke3_bdl	Bit delay line of CKE3.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	cke2_bdl	Bit delay line of CKE2.

ACCMDBDL6

ACCMDBDL6 is AC command bit delay line configuration register 6.

Offset Address	Register Name	Total Reset Value
0x138	ACCMDBDL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cas_bdl				reserved												we_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	cas_bdl	Bit delay line of CAS.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	we_bdl	Bit delay line of WE.

ACCMDBDL7

ACCMDBDL7 is AC command bit delay line configuration register 7.

Offset Address	Register Name	Total Reset Value
0x13C	ACCMDBDL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												resetn_bdl				reserved												ras_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	resetn_bdl	Bit delay line of RESETN.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	ras_bdl	Bit delay line of RAS.

ACADDRBDL0

ACADDRBDL0 is AC address bit delay line configuration register 0.

Offset Address	Register Name	Total Reset Value
0x140	ACADDRBDL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr1_bdl				reserved												addr0_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr1_bdl	Bit delay line of ADDR1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr0_bdl	Bit delay line of ADDR0.

ACADDRBDL1

ACADDRBDL1 is AC address bit delay line configuration register 1.

Offset Address	Register Name	Total Reset Value
0x144	ACADDRBDL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr3_bdl				reserved												addr2_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr3_bdl	Bit delay line of ADDR3.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr2_bdl	Bit delay line of ADDR2.

ACADDRBDL2

ACADDRBDL2 is AC address bit delay line configuration register 2.

Offset Address	Register Name	Total Reset Value
0x148	ACADDRBDL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr5_bdl				reserved												addr4_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr5_bdl	Bit delay line of ADDR5.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr4_bdl	Bit delay line of ADDR4.

ACADDRBDL3

ACADDRBDL3 is AC address bit delay line configuration register 3.

Offset Address	Register Name	Total Reset Value
0x14C	ACADDRBDL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr7_bdl				reserved												addr6_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr7_bdl	Bit delay line of ADDR7.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr6_bdl	Bit delay line of ADDR6.

ACADDRBDL4

ACADDRBDL4 is AC address bit delay line configuration register 4.

Offset Address	Register Name	Total Reset Value
0x150	ACADDRBDL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr9_bdl				reserved												addr8_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr9_bdl	Bit delay line of ADDR9.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr8_bdl	Bit delay line of ADDR8.

ACADDRBDL5

ACADDRBDL5 is AC address bit delay line configuration register 5.

Offset Address	Register Name	Total Reset Value
0x154	ACADDRBDL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr11_bdl				reserved												addr10_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr11_bdl	Bit delay line of ADDR11.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr10_bdl	Bit delay line of ADDR10.

ACADDRBDL6

ACADDRBDL6 is AC address bit delay line configuration register 6.

Offset Address	Register Name	Total Reset Value
0x158	ACADDRBDL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr13_bdl				reserved												addr12_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr13_bdl	Bit delay line of ADDR13.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr12_bdl	Bit delay line of ADDR12.

ACADDRBDL7

ACADDRBDL7 is AC address bit delay line configuration register 7.

Offset Address	Register Name	Total Reset Value
0x15C	ACADDRBDL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												addr15_bdl				reserved												addr14_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	addr15_bdl	Bit delay line of ADDR15.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	addr14_bdl	Bit delay line of ADDR14.

ACADDRBDL8

ACADDRBDL8 is AC address bit delay line configuration register 8.

Offset Address	Register Name	Total Reset Value
0x160	ACADDRBDL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												ba1_bdl				reserved												ba0_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved.
[20:16]	RW	ba1_bdl	Bit delay line of BA1.
[15:5]	RO	reserved	Reserved.
[4:0]	RW	ba0_bdl	Bit delay line of BA0.

ACADDRBDL9

ACADDRBDL9 is AC address bit delay line configuration register 9.

Offset Address	Register Name	Total Reset Value
0x164	ACADDRBDL9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ba2_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved.
[4:0]	RW	ba2_bdl	Bit delay line of BA2.

ACCLKBDL

ACCLKBDL is an AC clock bit delay line configuration register.

Offset Address	Register Name	Total Reset Value
0x168	ACCLKBDL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fbclk_bdl				reserved				refclk_bdl				reserved				dramclk1_bdl				reserved				dramclk0_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:24]	RW	fbclk_bdl	Bit delay line of FBCLK.
[23:21]	RO	reserved	Reserved.
[20:16]	RW	refclk_bdl	Bit delay line of REFCLK.
[15:13]	RO	reserved	Reserved.
[12:8]	RW	dramclk1_bdl	Set this field to default value.
[7:5]	RO	reserved	Reserved.
[4:0]	RW	dramclk0_bdl	Set this field to default value.

ACPHYCTL0

ACPHYCTL0 is AC block PHY control register 0. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x170	ACPHYCTL0	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									bufphyclk_div2	lvdqclkdiv2	dramclk_l	dramclk_h	margin_a1	margin_a0	enshift_a0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved.
[6]	RW	bufphyclk_div2	PHY control.
[5]	RW	lvdqclkdiv2	PHY control.
[4]	RW	dramclk_l	PHY control.
[3]	RW	dramclk_h	PHY control.
[2]	RW	margin_a1	PHY control.
[1]	RW	margin_a0	PHY control.
[0]	RW	enshift_a0	PHY control.

ACPHYCTL1

ACPHYCTL1 is AC block PHY control register 1. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x174	ACPHYCTL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dram1sel_addr																reserved				dram1sel_ba				reserved	dram1sel_we	dram1sel_cas	dram1sel_ras	dram1sel_odt	dram1sel_cke	dram1sel_cs	dram1sel_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	dram1sel_addr	PHY control.
[15:11]	RO	Reserved.	Reserved.
[10:8]	RW	dram1sel_ba	PHY control.
[7]	RO	Reserved.	Reserved.
[6]	RW	dram1sel_we	PHY control.
[5]	RW	dram1sel_cas	PHY control.
[4]	RW	dram1sel_ras	PHY control.
[3]	RW	dram1sel_odt	PHY control.
[2]	RW	dram1sel_cke	PHY control.
[1]	RW	dram1sel_cs	PHY control.
[0]	RW	dram1sel_reset	PHY control.

ACPHYCTL2

ACPHYCTL2 is AC block PHY control register 2. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x178	ACPHYCTL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sdrsel_addr																Reserved.				sdrsel_ba				Reserved.	sdrsel_we	sdrsel_cas	sdrsel_ras	sdrsel_odt	sdrsel_cke	sdrsel_cs	sdrsel_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	sdrsel_addr	PHY control.
[15:11]	RO	Reserved.	Reserved.
[10:8]	RW	sdrsel_ba	PHY control.
[7]	RO	Reserved.	Reserved.
[6]	RW	sdrsel_we	PHY control.
[5]	RW	sdrsel_cas	PHY control.
[4]	RW	sdrsel_ras	PHY control.
[3]	RW	sdrsel_odt	PHY control.
[2]	RW	sdrsel_cke	PHY control.
[1]	RW	sdrsel_cs	PHY control.
[0]	RW	sdrsel_reset	PHY control.

ACPHYCTL3

ACPHYCTL3 is AC block PHY control register 3. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x17C	ACPHYCTL3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	posedge_addr																Reserved.						posedge_ba		Reserved.	posedge_we	posedge_cas	posedge_ras	posedge_odt	posedge_cke	posedge_cs	posedge_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	posedge_addr	PHY control.
[15:11]	RO	Reserved.	Reserved.
[10:8]	RW	posedge_ba	PHY control.
[7]	RO	Reserved.	Reserved.
[6]	RW	posedge_we	PHY control.
[5]	RW	posedge_cas	PHY control.
[4]	RW	posedge_ras	PHY control.
[3]	RW	posedge_odt	PHY control.
[2]	RW	posedge_cke	PHY control.
[1]	RW	posedge_cs	PHY control.
[0]	RW	posedge_reset	PHY control.

ACPHYCTL4

ACPHYCTL4 is AC block PHY control register 4. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x180	ACPHYCTL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timing2T_addr																Reserved.				timing2T_ba				Reserved.	timing2T_we	timing2T_cas	timing2T_ras	timing2T_odt	timing2T_cke	timing2T_cs	timing2T_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	timing2T_addr	PHY control.
[15:11]	RO	Reserved.	Reserved.
[10:8]	RW	timing2T_ba	PHY control.
[7]	RO	Reserved.	Reserved.
[6]	RW	timing2T_we	PHY control.
[5]	RW	timing2T_cas	PHY control.
[4]	RW	timing2T_ras	PHY control.
[3]	RW	timing2T_odt	PHY control.
[2]	RW	timing2T_cke	PHY control.
[1]	RW	timing2T_cs	PHY control.
[0]	RW	timing2T_reset	PHY control.

ACPHYCTL5

ACPHYCTL5 is AC block PHY control register 5. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x184	ACPHYCTL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				clk1x_cmd2t_ctl2				clk1x_mclk				clk1x_cmd1t				clk1x_cmd2t				clk1x_cmd2t_ctl				clk1x_dramclk1				clk1x_dramclk0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	Reserved.	Reserved.
[27:24]	RW	clk1x_cmd2t_ctl2	PHY control.

[23:20]	RW	clk1x_mclk	PHY control.
[19:16]	RW	clk1x_cmd1t	PHY control.
[15:12]	RW	clk1x_cmd2t	PHY control.
[11:8]	RW	clk1x_cmd2t_ctl	PHY control.
[7:4]	RW	clk1x_dramclk1	PHY control.
[3:0]	RW	clk1x_dramclk0	PHY control.

ACPHYCTL6

ACPHYCTL6 is AC block PHY control register 6. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x188	ACPHYCTL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				clk2x_cmd2t_ctl2				clk2x_mclk				clk2x_cmd1t				clk2x_cmd2t				clk2x_cmd2t_ctl				clk2x_dramclk1				clk2x_dramclk0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	Reserved.	Reserved.
[27:24]	RW	clk2x_cmd2t_ctl2	PHY control.
[23:20]	RW	clk2x_mclk	PHY control.
[19:16]	RW	clk2x_cmd1t	PHY control.
[15:12]	RW	clk2x_cmd2t	PHY control.
[11:8]	RW	clk2x_cmd2t_ctl	PHY control.
[7:4]	RW	clk2x_dramclk1	PHY control.
[3:0]	RW	clk2x_dramclk0	PHY control.

ACPHYCTL7

ACPHYCTL7 is AC block PHY control register 7. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x018C	ACPHYCTL7	0x0080_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.					halft_cmd2tctl2	halft_dramclk0	halft_dramclk1	halft_cmd1t	Reserved.	halft_cmd2tctl	ck5p_cmd2tc				Reserved.				ck3p_cmd1t			ck2p_dclk1				ck1p_dclk0				ck0p_mclk				ckd2_mclk			
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	Reserved.	Reserved.
[26]	RW	halft_cmd2tctl2	Set this field to default value.
[25]	RW	halft_dramclk0	Set this field to default value.
[24]	RW	halft_dramclk1	Set this field to default value.
[23]	RW	halft_cmd1t	Set this field to default value.
[22]	RO	Reserved.	Reserved.
[21]	RW	halft_cmd2tctl	Set this field to default value.
[20:18]	RW	ck5p_cmd2tc	Set this field to default value.
[17:15]	RO	Reserved.	Reserved.
[14:12]	RW	ck3p_cmd1t	Set this field to default value.
[11:9]	RW	ck2p_dclk1	Configure DRAM CK1 clock phase from PLL1 tap: 1/16 T
[8:6]	RW	ck1p_dclk0	Configure DRAM CK0 clock phase from PLL1 tap: 1/16 T
[5:3]	RW	ck0p_mclk	Set this field to default value.
[2:0]	RW	ckd2_mclk	Set this field to default value.

ACDEBUG

ACDEBUG is a PHY debugging register.

Offset Address	Register Name	Total Reset Value
0x0190	ACDEBUG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												acdbg_config				Reserved.							DESKEW_regread	Reserved.							ac_rdcnt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	Reserved.	Reserved.
[19:16]	RW	acdbg_config	Set this field to default value.
[15:9]	RO	Reserved.	Reserved.
[8]	RO	DESKEW_regread	Set this field to default value.
[7:3]	RO	Reserved.	Reserved.
[2:0]	RO	ac_rdcnt	Set this field to default value.

ACPHYRSVDC

ACPHYRSVDC is AC block PHY reserved control pin register 1. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x0194	ACPHYRSVDC	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ac_rsv_control																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	ac_rsv_control	Reserved.

ACPHYRSVDS

ACPHYRSVDS is AC block PHY reserved control pin register 2. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x0198	ACPHYRSVDS	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ac_rsv_status																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ac_rsv_status	Reserved.

ACPHYCTL8

ACPHYCTL8 is AC block PHY control register 8. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x019C	ACPHYCTL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												ac_ck12p_reserve				ac_ck11p_reserve				ac_ck10p_reserve				ac_ck9p_reserve				ac_ck8p_reserve				ac_ck7p_reserve				ac_ck6p_reserve			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	Reserved.	Reserved.
[20:18]	RW	ac_ck12p_reserve	Set this field to default value.
[17:15]	RW	ac_ck11p_reserve	Set this field to default value.
[14:12]	RW	ac_ck10p_reserve	Set this field to default value.
[11:9]	RW	ac_ck9p_reserve	Set this field to default value.
[8:6]	RW	ac_ck8p_reserve	Set this field to default value.
[5:3]	RW	ac_ck7p_reserve	Set this field to default value.
[2:0]	RW	ac_ck6p_reserve	Set this field to default value.

ACCMDBDL8

ACCMDBDL8 is AC command bit delay line configuration register 8.

Offset Address	Register Name	Total Reset Value
0x1A0	ACCMDBDL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												odt1_bdl1				Reserved.												odt1_bdl0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	Reserved.	Reserved.
[20:16]	RW	odt1_bdl1	Set this field to default value.
[15:5]	RO	Reserved.	Reserved.
[4:0]	RW	odt1_bdl0	Set this field to default value.

ACCMDBDL9

ACCMDBDL9 is AC command bit delay line configuration register 9.

Offset Address	Register Name	Total Reset Value
0x1A4	ACCMDBDL9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												odt1_bdl3				Reserved.												odt1_bdl2			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	Reserved.	Reserved.
[20:16]	RW	odt1_bdl3	Set this field to default value.
[15:5]	RO	Reserved.	Reserved.
[4:0]	RW	odt1_bdl2	Set this field to default value.

ACCMDBDL10

ACCMDBDL10 is AC command bit delay line configuration register 10.

Offset Address	Register Name	Total Reset Value
0x1A8	ACCMDBDL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												cs1_bdl1				Reserved.												cs1_bdl0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	Reserved.	Reserved.
[20:16]	RW	cs1_bdl1	Set this field to default value.
[15:5]	RO	Reserved.	Reserved.
[4:0]	RW	cs1_bdl0	Set this field to default value.

ACCMDBDL11

ACCMDBDL11 is AC command bit delay line configuration register 11.

Offset Address	Register Name	Total Reset Value
0x1AC	ACCMDBDL11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												cs1_bdl3				Reserved.												cs1_bdl2			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	Reserved.	Reserved.
[20:16]	RW	cs1_bdl3	Set this field to default value.
[15:5]	RO	Reserved.	Reserved.
[4:0]	RW	cs1_bdl2	Set this field to default value.

ACPHYDCC

ACPHYDCC is an AC block PHY DCC control register. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x01B0	ACPHYDCC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												acdcc_mclk				Reserved.	acdcc_dqs0			Reserved.	acdcc_dqs1			Reserved.	acdcc_dq0			Reserved.	acdcc_dq1		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	Reserved.	Reserved.
[18:16]	RW	acdcc_mclk	Set this field to default value.
[15]	RO	Reserved.	Reserved.
[14:12]	RW	acdcc_dqs0	Set this field to default value.
[11]	RO	Reserved.	Reserved.
[10:8]	RW	acdcc_dqs1	Set this field to default value.
[7]	RO	Reserved.	Reserved.
[6:4]	RW	acdcc_dq0	Set this field to default value.
[3]	RO	Reserved.	Reserved.
[2:0]	RW	acdcc_dq1	Set this field to default value.

ACPHYCTL9

ACPHYCTL9 is AC block PHY control register 9. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x01B4	ACPHYCTL9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																				actiming2t_odt1	actiming2t_cke1	actiming2t_cs1	acdram1sel_odt1	acdram1sel_cke1	acdram1sel_cs1	acposedge_odt1	acposedge_cke1	acposedge_cs1	acsdrsel_odt1	acsdrsel_cke1	acsdrsel_cs1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	Reserved.	Reserved.

[11]	RW	actiming2t_odt1	Set this field to default value.
[10]	RW	actiming2t_cke1	Set this field to default value.
[9]	RW	actiming2t_cs1	Set this field to default value.
[8]	RW	acdram1sel_odt1	Set this field to default value.
[7]	RW	acdram1sel_cke1	Set this field to default value.
[6]	RW	acdram1sel_cs1	Set this field to default value.
[5]	RW	acposedge_odt1	Set this field to default value.
[4]	RW	acposedge_cke1	Set this field to default value.
[3]	RW	acposedge_cs1	Set this field to default value.
[2]	RW	acsdrsel_odt1	Set this field to default value.
[1]	RW	acsdrsel_cke1	Set this field to default value.
[0]	RW	acsdrsel_cs1	Set this field to default value.

CATTIMER0

CATTIMER0 is a CA training timer 0 register.

Offset Address	Register Name	Total Reset Value
0x01C0	CATTIMER0	0x0B17_0B0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				tcackeh				Reserved.				tcacd				Reserved.				tcaent				Reserved.				tcackel			
Reset	0	0	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:30]	RO	Reserved.	Reserved.
[29:24]	RW	tcackeh	tCACKEH (dficlk cycle).
[23:22]	RO	Reserved.	Reserved.
[21:16]	RW	tcacd	tCACD (dficlk cycle).
[15:14]	RO	Reserved.	Reserved.
[13:8]	RW	tcaent	tCAENT (dficlk cycle).
[7:6]	RO	Reserved.	Reserved.
[5:0]	RW	tcackel	tCACKEL (dficlk cycle).

CATTIMER1

CATTIMER1 is CA training timer 1 register.

Offset Address	Register Name	Total Reset Value
0x01C4	CATTIMER1	0x0000_040B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																				tmrz				Reserved.				tcaext			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:14]	RO	Reserved.	Reserved.
[13:8]	RW	tmrz	tMRZ (dficlk cycle).
[7:6]	RO	Reserved.	Reserved.
[5:0]	RW	tcaext	tCAEXT (dficlk cycle).

CATCONFIG

CATCONFIG is a CA training configuration register.

Offset Address	Register Name	Total Reset Value
0x01C8	CATCONFIG	0x0008_2606

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_cat_en	sw_cat_dqvalid	sw_cat_cke_low	sw_cat_cke_high	sw_cat_strobe	sw_cat_mrw41	sw_cat_mrw48	sw_cat_mrw42	Reserved.			cat_openeye_en	cat_restore_en	cat_cat_phydq_sel	Reserved.		cat_rb_backtap				ca_samp_num_ph				Reserved.				ca_samp_num_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31]	RW	sw_cat_en	SW CA training enable. When this field is asserted, PACK will enter the SW CA training state. After the SW CA training is complete, this bit should be deasserted by firmware. 0: disabled (default) 1: enabled

[30]	RW	sw_cat_dqvalid	SW CA training. This field indicates whether the CA result is ready. This bit is cleared when sw_cat_strobe is asserted. Then after the timing tCACD, this bit is asserted. 0: not valid 1: valid
[29]	RW	sw_cat_cke_low	SW CA training. This field is used to request the CKE to be low and it cleared by HW.
[28]	RW	sw_cat_cke_high	SW CA training. This field is used to request the CKE to be high and is cleared by HW.
[27]	RW	sw_cat_strobe	SW CA training. This field is used to issue the predefined SW CA pattern and is cleared by HW.
[26]	RW	sw_cat_mrw41	SW CA training. This field is used to issue the MRW41 command and is cleared by HW.
[25]	RW	sw_cat_mrw48	SW CA training. This field is used to issue the MRW48 command and is cleared by HW.
[24]	RW	sw_cat_mrw42	SW CA training. This field is used to issue the MRW42 command and is cleared by HW.
[23:21]	RO	Reserved.	Reserved.
[20]	RW	cat_openeye_en	HW CA training open eye enable. 0: disabled (default) 1: enabled
[19]	RW	cat_restore_en	HW CA training restore enable. If this field is set to high, the CA training will restore the CA phase before the second CA training (mapping stage) starts. This field is recommended to set to high. 0: disabled 1: enabled (default)
[18]	RW	cat_cat_phydq_sel	HW CA training PHY DQ CA result select. 0: LSB (default) 1: MSB
[17:16]	RO	Reserved.	Reserved.
[15:12]	RW	cat_rb_backtap	HW CA training right boundary back tap. This field is used to offset the addrph_a before the right boundary search is started to overcome meta-sable zone.
[11:8]	RW	ca_samp_num_ph	HW CA training sample count for CA phase. Value range: 1−15
[7:4]	RO	Reserved.	Reserved.
[3:0]	RW	ca_samp_num_bdl	HW CA training sample count for CA BDL. Value range: 1−15

CATRESULT

CATRESULT is a CA training result register (for debugging).

Offset Address	Register Name	Total Reset Value
0x01CC	CATRESULT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																						cat_reault									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	Reserved.	Reserved.
[9:0]	RO	cat_reault	CA training. HW CA training result for each address bit during each HW CA training state. This field is meaningful only after the HW CA training is complete and is only for debugging. 0: Failed 1: OK

PHYDQRESULT

PHYDQRESULT is a SW CA training DQ result (from PHY) register.

Offset Address	Register Name	Total Reset Value
0x01D0	PHYDQRESULT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy_dq_result																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	phy_dq_result	SW CA training. SW CA training latched results from the DRAM device. For the LPDDR3 CA training, the meaningful bits are [15:0] (mapped to DQ[15:0]). PACK and PHY will not latch these bits, so these bits are those you obtained on DQ of the DRAM device.

ADDRPHBOUND

ADDRPHBOUND is a CA training address phase boundary register.

Offset Address	Register Name	Total Reset Value
0x01D4	ADDRPHBOUND	0x0008_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				addrph_a_ori				Reserved.				addrph_a				Reserved.				addrph_a_left				Reserved.				addrph_a_right			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	Reserved.	Reserved.
[28:24]	RO	addrph_a_ori	HW CA training. This field records the address phase before the HW CA training (for debugging).
[23:21]	RO	Reserved.	Reserved.
[20:16]	RW	addrph_a	HW CA training. This field records the left boundary of the address phase after the HW CA training (for debugging).
[15:13]	RO	Reserved.	Reserved.
[12:8]	RO	addrph_a_left	HW CA training. This field records the left boundary of the address phase after the HW CA training (for debugging).
[7:5]	RO	Reserved.	Reserved.
[4:0]	RO	addrph_a_right	HW CA training. This field records the right boundary of the address phase after the HW CA training (for debugging).

SWCATPATTERN_P

SWCATPATTERN_P is an SW CA training pattern register for the positive CK edge.

Offset Address	Register Name	Total Reset Value
0x01D8	SWCATPATTERN_P	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																								sw_cat_pat_p							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	Reserved.	Reserved.
[9:0]	RW	sw_cat_pat_p	SW CA training pattern for the positive CK edge. You can fill any pattern.

SWCATPATTERN_N

SWCATPATTERN_N is an SW CA training pattern register for the negative CK edge.

Offset Address	Register Name	Total Reset Value
0x01DC	SWCATPATTERN_N	0x0000_03FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																						sw_cat_pat_n									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:10]	RO	Reserved.	Reserved.
[9:0]	RW	sw_cat_pat_n	SW CA training pattern for the negative CK edge. You can fill any pattern.

LPCTRL

LPCTRL is a low-power control register.

Offset Address	Register Name	Total Reset Value
0x01E4	LPCTRL	0xFE80_8688

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcken_auto_en	gcken_dfi_main	gcken_dinit	gcken_dtrain	gcken_retrain	gcken_acbist	gcken_dxbist	t_wakeup_thrd_lv2				lp_cmdoen_disable	lp_ac_phy_clkgated_disable	lp_dx_phy_clkgated_disable	lp_dx_phy_phgated_disable	lp_pll_powerdown_disable	t_resp				t_wakeup_thrd_lv3				t_dram_clk_disable				t_dram_clk_enable			
Reset	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31]	RW	gcken_auto_en	Auto gated clock control enable. If this field is set to high, HW automatically/dynamically controls the PACK high-level clock gating. 0: off 1: on (default)

[30]	RW	gcken_dfi_main	Manual gating control, main DFI clock gating switch. 0: clock off 1: clock on (default) When this field is set to low (clock off), some control registers that use the dfi_main clock are affected.
[29]	RW	gcken_dinit	Manual gating control, DRAM initialization clock gating. 0: clock off 1: clock on (default)
[28]	RW	gcken_dtrain	Manual gating control, data training clock gating. 0: clock off 1: clock on (default)
[27]	RW	gcken_retrain	Manual gating control, retraining clock gating. 0: clock off 1: clock on (default)
[26]	RW	gcken_acbist	Manual gating control, AC BIST clock gating. 0: clock off 1: clock on (default)
[25]	RW	gcken_dxbist	Manual gating control, data BIST clock gating. 0: clock off 1: clock on (default)
[24:21]	RW	t_wakeup_thrd_lv2	DFI low-power control interface timing threshold. ≥ wakeup_thrd_lv2: PHY clock gating, disable AC output enable ≥ wakeup_thrd_lv3: PHY clock gating, disable AC output enable, PHY PLL disable **NOTE** wakeup_thrd_lv3 should ≥ wakeup_thrd_lv2
[20]	RW	lp_cmdoen_disable	LP CMDOEN function disable when low-power assert. If this function is enabled, the I/O output of CA is floating to reduce I/O power. 0: LP-related function enabled (default) 1: LP-related function disabled
[19]	RW	lp_ac_phy_clkgated_disable	LP AC PHY clock gating disable when low-power assert. 0: LP-related function enabled (default) 1: LP-related function disabled
[18]	RW	lp_dx_phy_clkgated_disable	LP DX PHY clock gating disable when low-power assert. 0: LP-related function enabled (default) 1: LP-related function disabled

[17]	RW	lp_dx_phy_phgated_disable	DX PHY clock phase gating disable when low-power assert. 0: LP-related function enabled (default) 1: LP-related function disabled
[16]	RW	lp_pll_powerdown_disable	LP PLL disable function disable when low-power assert. 0: LP-related function enabled (default) 1: LP-related function disabled
[15:12]	RW	t_resp	DFI low-power control interface timing parameter. The field value must be smaller than DFI tlp_resp.
[11:8]	RW	t_wakeup_thrd_lv3	DFI low-power control interface timing threshold. ≥ wakeup_thrd_lv2: PHY clock gating, disable AC output enable ≥ wakeup_thrd_lv3: PHY clock gating, disable AC output enable, PHY PLL power down Note: wakeup_thrd_lv3 should ≥ wakeup_thrd_lv2
[7:4]	RW	t_dram_clk_disable	DFI DRAM clock disable timing parameter. This field is used to count down before DRAM CK is disabled.
[3:0]	RW	t_dram_clk_enable	DFI DRAM clock enable timing parameter. This field is used to count down before DRAM CK is enabled.

DXNBISTCTRL

DXNBISTCTRL is a loopback data comparison control register during BIST of data blocks.

Offset Address	Register Name	Total Reset Value
0x200 + *n* x 0x80 (*n* = 0–3)	DXNBISTCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lfsr_seed								Reserved.							dqm_cmp_mask	dq_cmp_mask								Reserved.							bist_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	lfsr_seed	LFSR seed value. This field specifies the initial seed value of the LFSR generator to this byte lane.
[23:17]	RO	Reserved.	Reserved.

[16]	RW	dqm_cmp_mask	DQM loopback compare mask. This field controls whether the comparison of the loopback data on DQM bits is disabled. 0: not compared 1: compared
[15:8]	RW	dq_cmp_mask	DQ loopback compare mask. This field controls whether the comparison of the loopback data on DQ bits is disabled. 0: not compared 1: compared
[7:1]	RO	Reserved.	Reserved.
[0]	RW	bist_en	BIST enable. This field specifies whether the data block is included for the loopback test while bist_op is set to BIST Enable.

DXNBISTSTS

DXNBISTSTS is a BIST test result and status register. Note that this register is read-only, and can be reset only by setting bist_op to BIST Reset.

Offset Address	Register Name	Total Reset Value
0x204 + *n* x 0x80 (*n* = 0–3)	DXNBISTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.															dqm_cmp_err	dq_cmp_ferr								dq_cmp_rerr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	Reserved.	Reserved.
[16]	RO	dqm_cmp_err	BIST error on DQM.
[15:8]	RO	dq_cmp_ferr	BIST error on DQ at the falling edge of DQS.
[7:0]	RO	dq_cmp_rerr	BIST error on DQ at the rising edge of DQS

DXNCTRL

DXNCTRL is a data block control register.

Offset Address	Register Name	Total Reset Value
0x208 + *n* x 0x80 (*n* = 0–3)	DXNCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																														dm_dis	bl_dis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	Reserved.	Reserved.
[1]	RW	dm_dis	Data mask disable. This field specifies whether the corresponding write data mask (DM) is enabled. When this field is set to 1, the corresponding DM is not used and calibrated during training.
[0]	RW	bl_dis	Byte lane disable. This field specifies whether the corresponding byte lane is in use. If the corresponding byte lane is not used, the PLL/DDL is powered down, and the output driver is turned off.

DXNWDQNBDL0

DXNWDQNBDL0 is data block bit delay configuration register 0.

Offset Address	Register Name	Total Reset Value
0x210 + *n* x 0x80 (*n* = 0–3)	DXNWDQNBDL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				wdq3bdl				Reserved.				wdq2bdl				Reserved.				wdq1bdl				Reserved.				wdq0bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	Reserved.	Reserved.
[28:24]	RW	wdq3bdl	Delay select of WDQ3. This field specifies the delay value of the bit delay line on the write path of DQ3.

[23:21]	RO	Reserved.	Reserved.
[20:16]	RW	wdq2bdl	Delay select of WDQ2. This field specifies the delay value of the bit delay line on the write path of DQ2.
[15:13]	RO	Reserved.	Reserved.
[12:8]	RW	wdq1bdl	Delay select of WDQ1. This field specifies the delay value of the bit delay line on the write path of DQ1.
[7:5]	RO	Reserved.	Reserved.
[4:0]	RW	wdq0bdl	Delay select of WDQ0. This field specifies the delay value of the bit delay line on the write path of DQ0.

DXNWDQNBDL1

DXNWDQNBDL1 is data block bit delay configuration register 1.

Offset Address	Register Name	Total Reset Value
0x214 + *n* x 0x80 (*n* = 0–3)	DXNWDQNBDL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				wdq7bdl				Reserved.				wdq6bdl				Reserved.				wdq5bdl				Reserved.				wdq4bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	Reserved.	Reserved.
[28:24]	RW	wdq7bdl	Delay select of WDQ7. This field specifies the delay value of the bit delay line on the write path of DQ3.
[23:21]	RO	Reserved.	Reserved.
[20:16]	RW	wdq6bdl	Delay select of WDQ6. This field specifies the delay value of the bit delay line on the write path of DQ2.
[15:13]	RO	Reserved.	Reserved.
[12:8]	RW	wdq5bdl	Delay select of WDQ5. This field specifies the delay value of the bit delay line on the write path of DQ1.

[7:5]	RO	Reserved.	Reserved.
[4:0]	RW	wdq4bdl	Delay select of WDQ4. This field specifies the delay value of the bit delay line on the write path of DQ0.

DXNWDQNBDL2

DXNWDQNBDL2 is data block bit delay configuration register 2.

Offset Address	Register Name	Total Reset Value
0x218 + *n* x 0x80 (*n* = 0–3)	DXNWDQNBDL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																												wdmbdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	Reserved.	Reserved.
[4:0]	RW	wdmbdl	Delay select of WDQM. This field specifies the delay value of the bit delay line on DQM.

DXNRDQNBDL0

DXNRDQNBDL0 is data block bit delay configuration register 4.

Offset Address	Register Name	Total Reset Value
0x21C + *n* x 0x80 (*n* = 0–3)	DXNRDQNBDL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				rdq3bdl				Reserved.				rdq2bdl				Reserved.				rdq1bdl				Reserved.				rdq0bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	Reserved.	Reserved.
[28:24]	RW	rdq3bdl	Delay select of RDQ3. This field specifies the delay value of the bit delay line on the write path of DQ3.

[23:21]	RO	Reserved.	Reserved.
[20:16]	RW	rdq2bdl	Delay select of RDQ2. This field specifies the delay value of the bit delay line on the write path of DQ2.
[15:13]	RO	Reserved.	Reserved.
[12:8]	RW	rdq1bdl	Delay select of RDQ1. This field specifies the delay value of the bit delay line on the write path of DQ1.
[7:5]	RO	Reserved.	Reserved.
[4:0]	RW	rdq0bdl	Delay select of RDQ0. This field specifies the delay value of the bit delay line on the write path of DQ0.

DXNRDQNBDL1

DXNRDQNBDL1 is data block bit delay configuration register 5.

Offset Address	Register Name	Total Reset Value
0x220 + *n* x 0x80 (*n* = 0–3)	DXNRDQNBDL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				rdq7bdl				Reserved.				rdq6bdl				Reserved.				rdq5bdl				Reserved.				rdq4bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	Reserved.	Reserved.
[28:24]	RW	rdq7bdl	Delay select of RDQ7. This field specifies the delay value of the bit delay line on the write path of DQ3.
[23:21]	RO	Reserved.	Reserved.
[20:16]	RW	rdq6bdl	Delay select of RDQ6. This field specifies the delay value of the bit delay line on the write path of DQ2.
[15:13]	RO	Reserved.	Reserved.
[12:8]	RW	rdq5bdl	Delay select of RDQ5. This field specifies the delay value of the bit delay line on the write path of DQ1.

[7:5]	RO	Reserved.	Reserved.
[4:0]	RW	rdq4bdl	Delay select of RDQ4. This field specifies the delay value of the bit delay line on the write path of DQ0.

DXNRDQNBDL2

DXNRDQNBDL2 is data block bit delay configuration register 6.

Offset Address	Register Name	Total Reset Value
0x224 + *n* x 0x80 (*n* = 0–3)	DXNRDQNBDL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																												rdmbdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	Reserved.	Reserved.
[4:0]	RW	rdmbdl	Delay select of RDQM. This field specifies the delay value of the bit delay line on loopback read path of DQM.

DXNRDQSDLY

DXNRDQSDLY is a local delay line control register.

Offset Address	Register Name	Total Reset Value
0x22C + *n* x 0x80 (*n* = 0–3)	DXNRDQSDLY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.								rdqscyc								Reserved.								rdqsbdl							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	Reserved.	Reserved.
[22:16]	RW	rdqscyc	Read DQS clock phase select. This field specifies the number of taps in one clock cycle for the 1-T delay measurement type or the number of taps in half of clock cycle for the half-T delay measurement type. This field is used to create 90 degree delays for RDQS.

[15:7]	RO	Reserved.	Reserved.
[6:0]	RW	rdqsbdl	Read DQS delay select. This field specifies the phase shift of the read DQS to create 90 degree delays.

DXNWDQSDLY

DXNWDQSDLY is a write leveling DQS delay control register.

Offset Address: 0x230 + *n* x 0x80 (*n* = 0–3)
Register Name: DXNWDQSDLY
Total Reset Value: 0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Reserved.					wdqsphase	Reserved.	wdqsbdl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	RO	Reserved.	Reserved.
[11:8]	RW	wdqsphase	Write DQS clock phase select.
[7:5]	RO	Reserved.	Reserved.
[4:0]	RW	wdqsbdl	Write leveling DQS delay select. This field specifies the delay value of delay applied on WDQS for write leveling.

DXNWDQDLY

DXNWDQDLY is a write leveling delay line control register.

Offset Address: 0x234 + *n* x 0x80 (*n* = 0–3)
Register Name: DXNWDQDLY
Total Reset Value: 0x0000_0C00

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Reserved.					wdqphase	Reserved.	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	Reserved.	Reserved.

[12:8]	RW	wdqphase	Write data eye clock phase select.
[7:0]	RO	Reserved.	Reserved.

DXNWLSL

DXNWLSL is an extra system latency addition control register.

Offset Address	Register Name	Total Reset Value
0x238 + *n* x 0x80 (*n* = 0–3)	DXNWLSL	0x0001_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.														wlsl		Reserved.															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	Reserved.	Reserved.
[17:16]	RW	wlsl	Write leveling system latency. This field is used to adjust the write latency after write leveling.
[15:0]	RO	Reserved.	Reserved.

DXNRDQSGDLY

DXNRDQSGDLY is a local delay line control register.

Offset Address	Register Name	Total Reset Value
0x23C + *n* x 0x80 + *m* x 0x400 (*n* = 0–3) (*m* = 0–1)	DXNRDQSGDLY	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.			org_rdqsgph					Reserved.			rdqsgtxbdl					Reserved.			rdqsgphase				Reserved.			rdqsgbdl				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	Reserved.	Reserved.

[29:24]	RO	org_rdqsgph	Original read DQS gate phase before HW gate training post-update stage (for debugging).
[23:21]	RO	Reserved.	Reserved.
[20:16]	RW	rdqsgtxbdl	Read DQS gate delay select. This field specifies the delay value of the read gating delay before DQS dummy PAD.
[15:14]	RO	Reserved.	Reserved.
[13:8]	RW	rdqsgphase	Read DQS gating clock phase select.
[7:6]	RO	Reserved.	Reserved.
[5:0]	RW	rdqsgbdl	Read DQS gating delay select. This field specifies the delay value of the read gating delay after DQS dummy PAD.

DXPHYCTRL

DXPHYCTRL is a DX PHY control register.

Offset Address	Register Name	Total Reset Value
0x240 + *n* x 0x80 (*n* = 0–3)	DXPHYCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																dx_pll_cal		dx_pll_calm		dx_pll_calt		dx_pll_lt		dx_pll_sp		dx_pll_cpi		dx_pll_init		dx_pll_testen		dx_pll_testpem		dx_pll_thrm	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	Reserved.	Reserved.
[14]	RW	dx_pll_cal	The value 0x0 is recommended.
[13]	RW	dx_pll_calm	The value 0x0 is recommended.
[12]	RW	dx_pll_calt	The value 0x0 is recommended.
[11:10]	RW	dx_pll_lt	The value 0x0 is recommended.
[9:7]	RW	dx_pll_sp	The value 0x2 is recommended.
[6:4]	RW	dx_pll_cpi	The value 0x4 is recommended.

[3]	RW	dx_pll_init	The value 0x0 is recommended.
[2]	RW	dx_pll_testen	The value 0x0 is recommended.
[1]	RW	dx_pll_testpem	The value 0x0 is recommended.
[0]	RW	dx_pll_thrm	The value 0x0 is recommended.

DXNGDS

DXNGDS is a latch enable register. It is used to control the latch enable within the PHY to obtain stable data.

Offset Address	Register Name	Total Reset Value
0x248 + *n* x 0x80 (*n* = 0–3)	DXNGDS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																														gds	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	Reserved.	Reserved.
[2:0]	RW	gds	Rank 0 read data latch delay. This field is used as a reference stable region for the PHY to latch the read data.

DXNCLKBDL

DXNCLKBDL is a data block clock bit delay line configuration register.

Offset Address	Register Name	Total Reset Value
0x24C + *n* x 0x80 (*n* = 0–3)	DXNCLKBDL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												dx_refclk_bdl				Reserved.												dx_fbclk_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	Reserved.	Reserved.
[20:16]	RW	dx_refclk_bdl	Bit delay line of REFCLK.
[15:5]	RO	Reserved.	Reserved.

[4:0]	RW	dx_fbclk_bdl	Bit delay line of FBCLK.

DXNRDBOUND

DXNRDBOUND is a read data eye boundary register. This register indicates the left and right boundaries of RDQSQDL of the data eye.

Offset Address	Register Name	Total Reset Value
0x250 + *n* x 0x80 (*n* = 0–3)	DXNRDBOUND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												rdqsbdl_left				Reserved.												rdqsbdl_right			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	Reserved.	Reserved.
[22:16]	RO	rdqsbdl_left	Left boundary of read data eye.
[15:7]	RO	Reserved.	Reserved.
[6:0]	RO	rdqsbdl_right	Right boundary of read data eye.

DXNWRBOUND

DXNWRBOUND is a write data eye boundary register. This register indicates the left and right boundaries of WDQSQDL of the data eye.

Offset Address	Register Name	Total Reset Value
0x254 + *n* x 0x80 (*n* = 0–3)	DXNWRBOUND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												wdqphase_left				Reserved.												wdqphase_right			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	Reserved.	Reserved.
[20:16]	RO	wdqphase_left	Left boundary of the write data eye.
[15:5]	RO	Reserved.	Reserved.
[4:0]	RO	wdqphase_right	Right boundary of the write data eye.

DXNOEBDL

DXNOEBDL is an output enable delay line control register. This register specifies the delay line value of the output enable delay line within the PHY data block.

Offset Address	Register Name	Total Reset Value
0x258 + *n* x 0x80 (*n* = 0–3)	DXNOEBDL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.												wdqsoe_bdl				Reserved.												oen_bdl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	Reserved.	Reserved.
[20:16]	RW	wdqsoe_bdl	Write DQS output enable delay control.
[15:5]	RO	Reserved.	Reserved.
[4:0]	RW	oen_bdl	DQ output enable delay control.

DXNMISCCTRL0

DXNMISCCTRL0 is data block PHY miscellaneous control register 0. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x260 + *n* x 0x80 (*n* = 0–3)	DXNMISCCTRL0	0x0002_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.				ptrgated_en	enshift_a0	margin_a0	bufphyclkdiv2	lvdqclkdiv2	dqsgatedla	dx_rxp_2nd_dm	dx_rxn_2nd_dm	dx_dqs_h	dx_dqs_l	dx_margin_a1	rxp_2nd_dq					rxn_2nd_dq												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	Reserved.	Reserved.
[26]	RW	ptrgated_en	Set this field to default value.
[25]	RW	enshift_a0	Set this field to default value.

[24]	RW	margin_a0	After this field is modified, "phyconn_rst" is required to update the latest setting. If the dly_track_type=1 tracking type is required, this field should be set to 0x1 before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[23]	RW	bufphyclkdiv2	Set this field to default value.
[22]	RW	lvdqclkdiv2	Set this field to default value.
[21]	RW	dqsgatedla	Set this field to default value.
[20]	RW	dx_rxp_2nd_dm	After this field is modified, "phyconn_rst" is required to update the latest setting. If the dly_track_type=1 tracking type is required, this field should be set to 0x1 before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[19]	RW	dx_rxn_2nd_dm	After this field is modified, "phyconn_rst" is required to update the latest setting. If the dly_track_type=1 tracking type is required, this field should be set to 0x1 before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[18]	RW	dx_dqs_h	Set this field to default value.
[17]	RW	dx_dqs_l	Set this field to default value.
[16]	RW	dx_margin_a1	After this field is modified, "phyconn_rst" is required to update the latest setting. If the dly_track_type=1 tracking type is required, this field should be set to 0x1 before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[15:8]	RW	rxp_2nd_dq	After this field is modified, "phyconn_rst" is required to update the latest setting. When the dly_track_type=1 tracking type is required, this field should be set to 0xFF before initial trainings and dly_track_type should be set to 0x1 after initial trainings.
[7:0]	RW	rxn_2nd_dq	After this field is modified, "phyconn_rst" is required to update the latest setting. When the dly_track_type=1 tracking type is required, this field should be set to 0xFF before initial trainings and dly_track_type should be set to 0x1 after initial trainings.

DXNMISCCTRL1

DXNMISCCTRL1 is data block PHY miscellaneous control register 1. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x264 + *n* x 0x80 (*n* = 0–3)	DXNMISCCTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dqclk1x				dqclk2x				dqsgclk1x				dqsgclk2x				dqsclk1x				dqsclk2x				mclk1x				mclk2x			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	dqclk1x	Set this field to default value.
[27:24]	RW	dqclk2x	Set this field to default value.
[23:20]	RW	dqsgclk1x	Set this field to default value.
[19:16]	RW	dqsgclk2x	Set this field to default value.
[15:12]	RW	dqsclk1x	Set this field to default value.
[11:8]	RW	dqsclk2x	Set this field to default value.
[7:4]	RW	mclk1x	Set this field to default value.
[3:0]	RW	mclk2x	Set this field to default value.

DXDEBUG0

DXDEBUG0 is data block PHY debug signal register 0.

Offset Address	Register Name	Total Reset Value
0x268 + *n* x 0x80 (*n* = 0–3)	DXDEBUG0	0x0000_5415

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																s0a	s0b	s1a	s1b	s2a	s2b	dqs_rdcnt				dqs_ca				dqs_cb			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1	0	1

Bits	Access	Name	Description
[31:15]	RO	Reserved.	Debug signal.
[14]	RO	s0a	Set this field to default value.
[13]	RO	s0b	Set this field to default value.
[12]	RO	s1a	Set this field to default value.
[11]	RO	s1b	Reserved.
[10]	RO	s2a	Reserved.

[9]	RO	s2b	Reserved.
[8:6]	RO	dqs_rdcnt	Reserved.
[5:3]	RO	dqs_ca	Reserved.
[2:0]	RO	dqs_cb	Reserved.

DXDEBUG1

DXDEBUG1 is data block PHY debug signal register 1.

Offset Address	Register Name	Total Reset Value
0x26C + *n* x 0x80 (*n* = 0–3)	DXDEBUG1	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.								dqs0								dqs0b								dqs0_gold							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:24]	RO	Reserved.	Debug signal. Note that the field may have unknown values in the simulation.
[23:0]	RO	dqs0	Reserved.
[15:8]	RO	dqs0b	Reserved.
[7:0]	RO	dqs0_gold	Reserved.

DXPHYRSVD

DXPHYRSVD is a data block PHY reserved control pin register. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x270 + *n* x 0x80 (*n* = 0–3)	DXPHYRSVD	0x0000_FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dx_rsv_status																dx_rsv_control															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dx_rsv_status	Reserved.

[15:0]	RW	dx_rsv_control	Reserved. The followings are for (n = 0, 2): Bit 1 (reg_DQSG_extend_2T): 0/1: extend DQSG 1T/2T dfi_clk, when reg_DQSG_extend_en is 1 Bit 0 (reg_DQSG_extend_en): 0/1: disable/enable the DQSG extend function

DXNMISCCTRL2

DXNMISCCTRL2 is data block PHY miscellaneous control register 2. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x274 + *n* x 0x80 (*n* = 0–3)	DXNMISCCTRL2	0x0000_026F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																					reg_OE_extend1T_en	reg_dqsg_TX_2path	reg_squeach_en	reg_dqsglat1T_en	reg_sel_halfT_gated_16b	reg_dynamic_PUPDEN_16b	reg_dummypad_use	reg_ODTEN_gated	reg_GDS_r1T_sel_16b	BUFRESETCONTN_gated_TDC	BUFRESETCONTN_gated_DQSGERROR
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	1	1

Bits	Access	Name	Description
[31:11]	RO	Reserved.	Reserved.
[10]	RW	reg_OE_extend1T_en	Set this field to default value.
[9]	RW	reg_dqsg_TX_2path	Set this field to default value.
[8]	RW	reg_squeach_en	Set this field to default value.
[7]	RW	reg_dqsglat1T_en	Set this field to default value.
[6]	RW	reg_sel_halfT_gated_16b	Set this field to default value.

[5]	RW	reg_dynamic_PUPDEN_16b	Set this field to default value.
[4]	RW	reg_dummypad_use	Set this field to default value.
[3]	RW	reg_ODTEN_gated	Set this field to default value.
[2]	RW	reg_GDS_r1T_sel_16b	Set this field to default value.
[1]	RW	BUFRESETCONTN_gated_TDC	Set this field to default value.
[0]	RW	BUFRESETCONTN_gated_DQSGERROR	Set this field to default value.

DXDEBUGCONFIG

DXDEBUGCONFIG is a data block PHY debugging control register. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x278 + *n* x 0x80 (*n* = 0–3)	DXDEBUGCONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																											DESKEW_regread	reg_dbg_prepost_sel	reg_dbg_pllclk_sel	reg_dbg_REFFB_predly	reg_dbg_REFFB_postdly
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	Reserved.	Reserved.
[4]	RO	DESKEW_regread	Reserved. registers for the future.
[3]	RW	reg_dbg_prepost_sel	Set this field to default value.
[2]	RW	reg_dbg_pllclk_sel	Set this field to default value.
[1]	RW	reg_dbg_REFFB_predly	Set this field to default value.

[0]	RW	reg_dbg_REFFB_postdly	Set this field to default value.

DXNDCC

DXNDCC is a data block PHY DCC control register. This register is used to control the PHY and should not be modified.

Offset Address	Register Name	Total Reset Value
0x27C + *n* x 0x80 (*n* = 0–3)	DXNDCC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved.																				dxctl_mclk_dcc				dxctl_dqs_dcc				dxctl_dqsg_dcc				dxctl_dq_dcc			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	Reserved.	Reserved.
[11:9]	RW	dxctl_mclk_dcc	bit[11]: dly_sel_xxx_DCC_16b bit[10]: ctrlC_xxx_DCC_16b bit[9]: ctrl2_xxx_DCC_16b
[8:6]	RW	dxctl_dqs_dcc	bit[8]: dly_sel_xxx_DCC_16b bit[7]: ctrlC_xxx_DCC_16b bit[6]: ctrl2_xxx_DCC_16b
[5:3]	RW	dxctl_dqsg_dcc	bit[5]: dly_sel_xxx_DCC_16b bit[4]: ctrlC_xxx_DCC_16b bit[3]: ctrl2_xxx_DCC_16b
[2:0]	RW	dxctl_dq_dcc	bit[2]: dly_sel_xxx_DCC_16b bit[1]: ctrlC_xxx_DCC_16b bit[0]: ctrl2_xxx_DCC_16b

4.2 Flash Memory Controller

4.2.1 Overview

The flash memory controller (FMC) provides memory controller interfaces for connecting to external SPI NAND flash or SPI NOR flash to access data.

4.2.2 Features

The FMC has the following features:

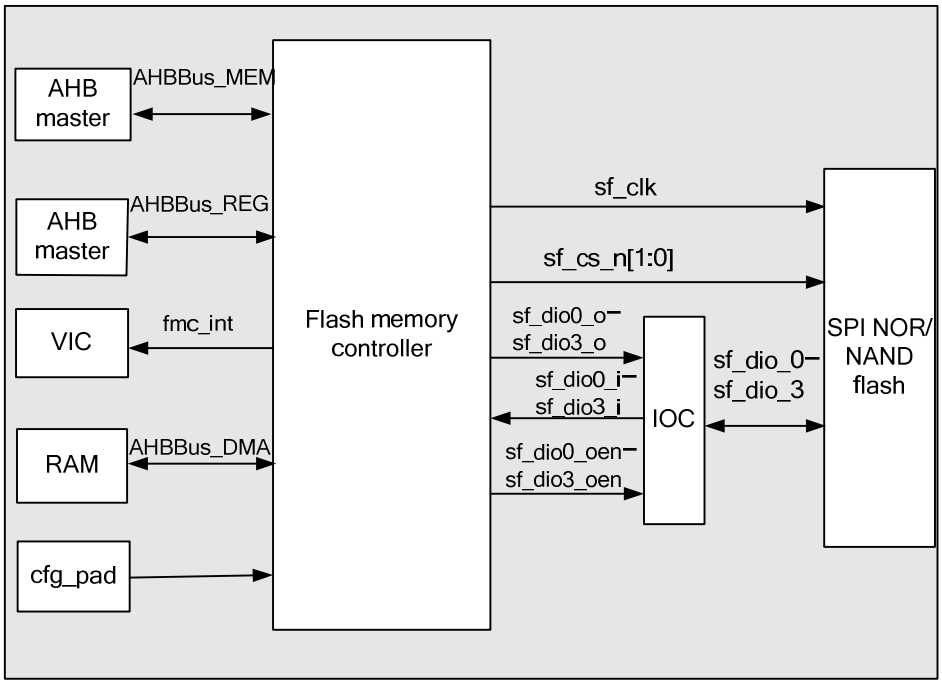
- Provides 4 KB+256 bytes on-chip buffer for improving the read speed.
- Supports two CSs that can be connected to two SPI NOR flash memories, two SPI NAND flash memories, or one SPI NAND flash memory and one SPI NOR flash memory.
- Supports the SPI NOR flash with 3-byte or 4-byte address.
- Support the SPI NAND flash with 2 KB or 4 KB page size.
- Supports five types of SPIs, including the standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, and quad I/O SPI.
- Boots directly from the SPI NOR flash or SPI NAND flash and supports at most 1 MB boot space when booting from CS0.
- Supports the function of skipping bad blocks during booting from the SPI NAND flash. The FMC automatically searches for good blocks for booting.
- Supports 1-wire and 4-wire boot modes for the SPI NAND flash and only 1-wire boot mode for the SPI NOR flash
- Supports the adaptive boot mode for the SPI NAND flash. The configurations of ecc_type and the page size are automatically configured by logic.
- Supports 8 bits/1 KB, 16 bits/1 KB, 24 bits/1 KB, and 28 bits/1 KB BCH code error correcting code (ECC) check and error correction for the NAND flash with the page size of 2 KB or 4 KB. Only the 8-bit or 24-bit ECC is supported during the boot process.
- Supports the query mode and interrupt report mode and reports the read/write interrupt, erase interrupt, programming completion interrupt, DMA programming timeout failure interrupt, and ECC check error interrupt.
- Supports the read and write operations in internal DMA mode for the SPI NAND flash. You can write only the entire page and read the entire page or the control information (read only the OOB).
- Supports data transfer in internal DMA mode for the SPI NOR flash. The length of the data transferred each time is configurable.
- Supports the read and write operations in transparent transfer (ECC0) mode. That is, data is directly transferred with unprocessed data storage structure.
- Supports the low-power mode. The unused modules can be disabled.

4.2.3 Function Description

4.2.3.1 Interface Block Diagram

The Hi3521A provides two CSs that can connect to the SPI NOR flash or SPI NAND flash. Figure 4-3 shows the block diagram of FMC interfaces.

Figure 4-3 Block diagram of FMC interfaces



In Figure 4-3, the pin names such as sf_clk indicate the names of pins in the FMC. Table 4-13 describes the mapping between the names of FMC pins and the names of external pins. In the following sections, the pin names related to interface description indicate the names of FMC pins.

Table 4-13 Mapping between the names of FMC pins and the names of chip pins

FMC Pin Name	Chip Pin Name
sf_clk	SFC_CLK
sf_dio_0	SFC_DIO
sf_dio_1	SFC_DOI
sf_dio_2	SFC_WP_IO2
sf_dio_3	SFC_HOLD_IO3
sf_cs_n[0]	SFC_CS0N
sf_cs_n[1]	SFC_CS1N

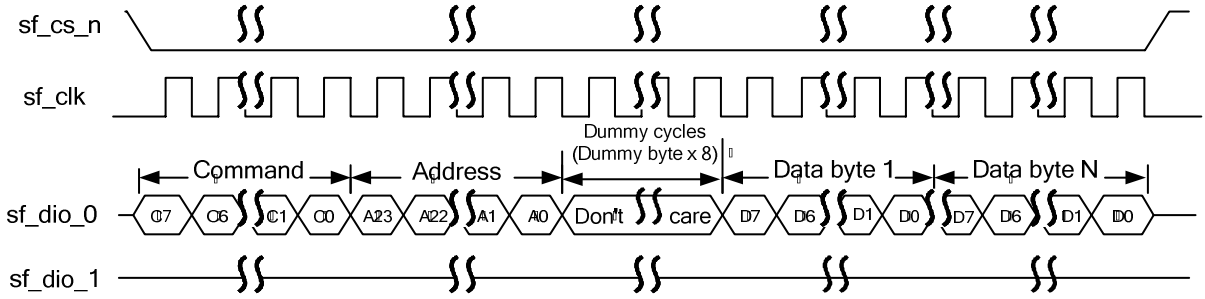
4.2.3.2 Interfaces

The FMC supports five types of SPIs, including the standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, and quad I/O SPI.

Standard SPI Mode

The standard SPI is connected to a 1-bit data input line and a 1-bit data output line. Figure 4-4 shows the write timing of the standard SPI.

Figure 4-4 Write timing of the standard SPI

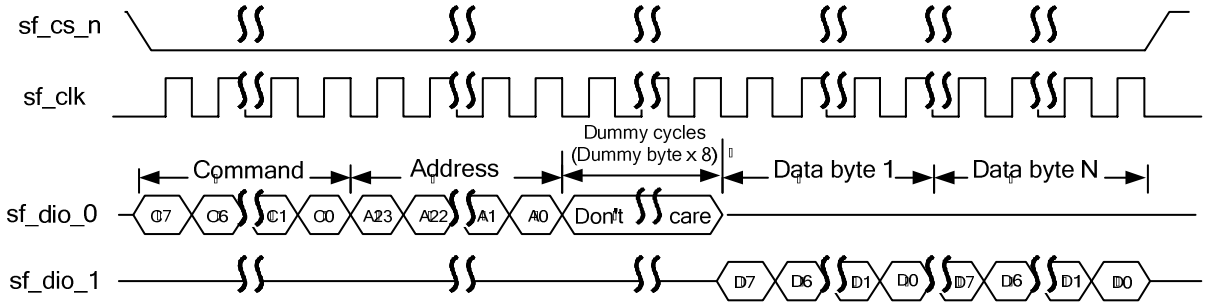


Note the following:

- The command cycles, address cycles, and dummy cycles are output in the unit of a single bit in serial mode through the sf_dio_0 line.
- The data bytes are output in the unit of a single bit in serial mode through the sf_dio_0 line.

Figure 4-5 shows the read timing of the standard SPI.

Figure 4-5 Read timing of the standard SPI



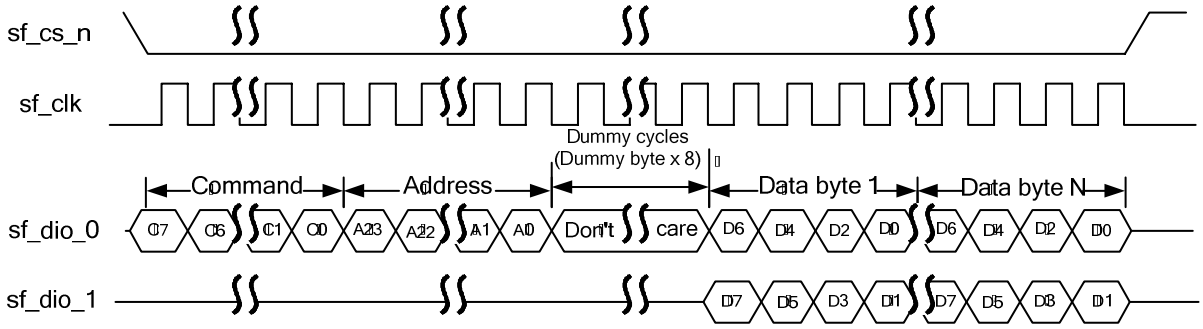
Note the following:

- The command cycles, address cycles, and dummy cycles are output in the unit of a single bit in serial mode through the sf_dio_0 line.
- The data bytes are input in the unit of a single bit in serial mode through the sf_dio_1 line.

Dual-Output/Dual-Input SPI

Figure 4-6 shows the timing of the dual-output/dual-input SPI.

Figure 4-6 Timing of the dual-output/dual-input SPI



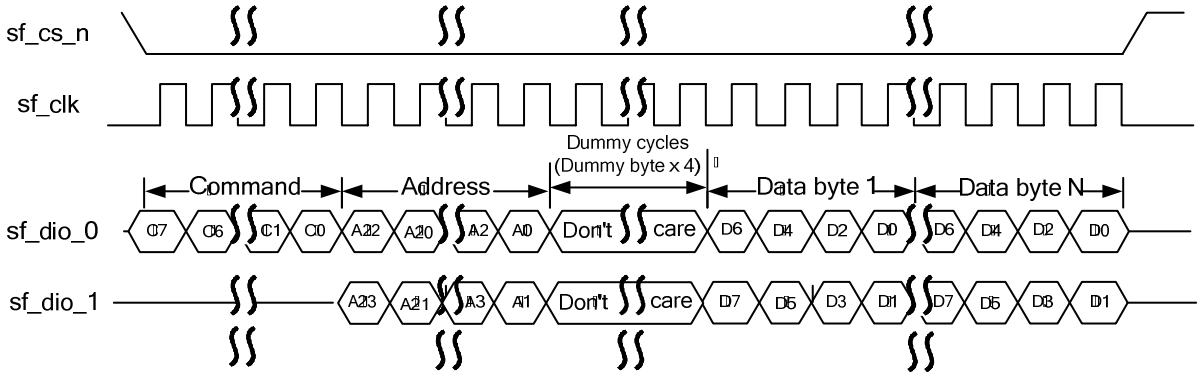
Note the following:

- The command cycles, address cycles, and dummy cycles are output in the unit of a single bit in serial mode through the sf_dio_0 line.
- The data bytes are output (written) or input (read) in the unit of two bits through the sf_dio_0 or sf_dio_1 line.

Dual I/O SPI

Figure 4-7 shows the timing of the dual I/O SPI.

Figure 4-7 Timing of the dual I/O SPI



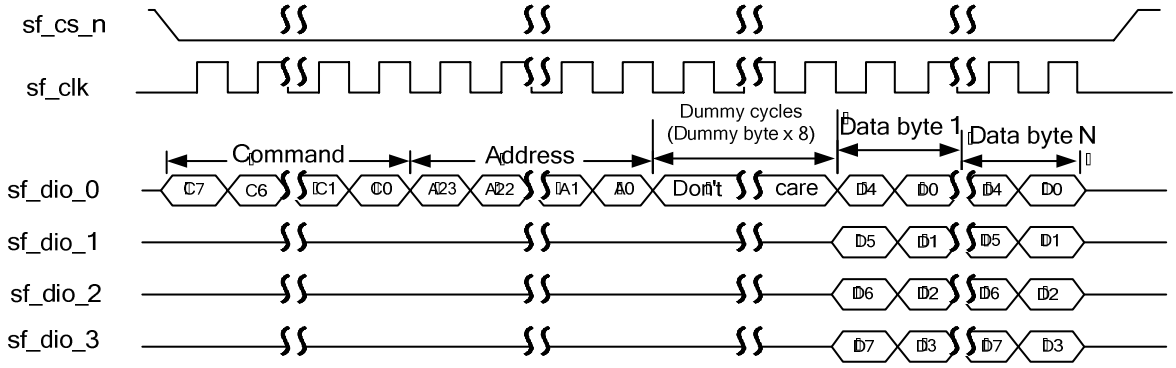
Note the following:

- The command cycles are output in the unit of a single bit in serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in the unit of two bits in serial mode through the sf_dio_0 or sf_dio_1 line.
- The data bytes are output (written) or input (read) in the unit of two bits through the sf_dio_0 or sf_dio_1 line.

Quad-Output/Quad-Input SPI

Figure 4-8 shows the timing of the quad-output/quad-input SPI.

Figure 4-8 Timing of the quad-output/quad-input SPI



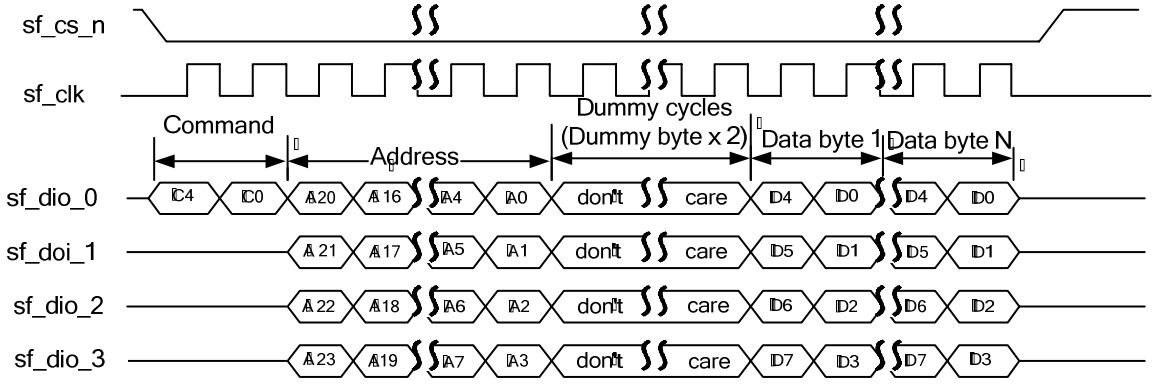
Note the following:

- The command cycles, address cycles, and dummy cycles are output in the unit of a single bit in serial mode through the sf_dio_0 line.
- The data bytes are output (written) or input (read) in the unit of four bits through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.

Quad I/O SPI

Figure 4-9 shows the timing of the quad I/O SPI.

Figure 4-9 Timing of the quad I/O SPI



Note the following:

- The command cycles are output in the unit of a single bit in serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in the unit of four bits in serial mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.
- The data bytes are output (written) or input (read) in the unit of four bits through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.

4.2.3.3 Boot Function

The FMC is in boot mode by default. The chip can boot by reading data directly from the flash memory. The CPU can directly read the data stored in the address ranging from 0x00_0000 to 0x0F_FFFF. The size of the entire address space is 1 MB.

For the SPI NAND flash, physical block 0 must be a good block. For other physical blocks, the bad blocks are skipped and the good blocks are read during the boot process. If there are five consecutive bad blocks, the boot fails. In other cases, the boot is successful even if there are bad blocks.

The chip boots and automatically adapts to the page size and required ECC of the SPI NAND flash based on ECC_TYPE and PAGE_SIZE.

4.2.3.4 Operations in Register Mode

The registers related to the operation command and address are configured by using software. Then the corresponding command is issued by configuring the FMC_OP register. The FMC issues a command to the flash memory according to the value configured by software. If data needs to be transferred to the flash memory, the internal buffer is used.

Operations such as reading ID, setting feature, and erasing are performed in this mode.

In register mode, all the operations related to the flash memory can be combined, and commands related to the address and data transfer can be issued separately.

4.2.3.5 Operations in Internal DMA Mode

The FMC can perform read and write operations in internal DMA mode for improving the access speed. In internal DMA mode, the FMC can directly access the DDR through the bus.

- DMA write operation: For the SPI NOR flash, data with any length can be transferred from any address of the DDR and written to any address of the flash memory. For the SPI NAND flash, the write operation is performed only by page.
- DMA read operation: For the SPI NOR flash, data with any length can be transferred from any address of the flash memory and written to any address of the DDR. For the SPI NAND flash, the entire page is read or only the OOB is read.
- Only-OOB read operation: When the software requires only software management information such as the bad block flag and empty block flag, only the control information needs to be read. In this case, only the OOB is read in DMA mode.

4.2.3.6 ECC Check

The FMC supports ECC check and error correction for the SPI NAND flash. Four types of ECCs are supported, including 8 bits/1 KB ECC, 16 bits/1 KB ECC, 24 bits/1 KB ECC, and 28 bits/1 KB ECC. The 8 bits/1 KB ECC indicates that errors occur in at most eight bits of the checked 1 KB data can be corrected.

The OOB information is added to the data with ECC protection, and then the ECC is added. The error correction algorithm runs by the error correction unit (1 KB). For example, the ECC is calculated for (DATA+OOB). If the page size is 2 KB, data in each error correction unit is (DATA+OOB)/2; if the page size is 4 KB, data in each error correction unit is (DATA+OOB)/4.

- The OOB is part of the software management information. For details, see the (BB+CTRL) part in the data structure.

- DATA indicates the real data. DATA indicates 2048-byte data when the page size is 2 KB and 4096-byte data when the page size is 4 KB.

During the boot process, only the 8-bit or 24-bit ECC is supported, while the flash memory requires 4 bits/512 bytes or 8 bits/512 bytes ECC (the error correction unit is 512 bytes in the memory manual). In normal mode, 8-/16-/24-/28-bit ECC is supported. The 16-bit and 28-bit ECCs are enhanced versions of the 8-bit and 24-bit ECCs. If the spare area of the flash is sufficient for storing the ECC, the 16 bits/1 KB error correction algorithm can be used for the flash that requires 4 bits/512 bytes ECC for improving reliability.

When the maximum error correction capability is exceeded, the uncorrectable error interrupt is reported. The FMC supports the alarm interrupt. When the number of error bits during one error correction operation is greater than or equal to the configured error threshold (FMC_ERR_THD), an error alarm interrupt is reported. If error bits occur in one or more error correction units and the number of error bits in each error correction unit is less than the error threshold and uncorrectable error value, the correctable error interrupt flag FMC_INT[err_val_int] is changed to 1.

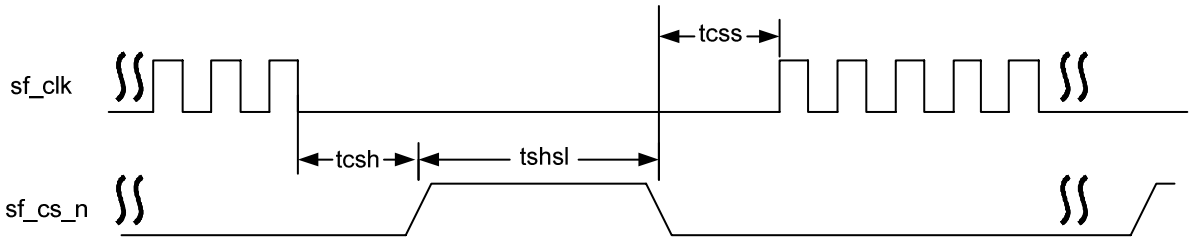
When the data on a page is read, if uncorrectable errors occur in one error correction unit, the uncorrectable error interrupt is reported. If an error alarm interrupt is reported for an error correction unit, the error correction alarm status is reported. If the number of error correction bits is less than the error threshold, the correctable error interrupt status is reported.

The FMC does not support ECC check for the SPI NOR flash. If FMC_CFG[ecc_type] is 0, the SPI NAND flash works in non-ECC check mode and the FMC transfers data directly from the flash without data structure processing.

4.2.3.7 SPI Timings

Figure 4-10 shows the SPI timings and related parameters.

Figure 4-10 SPI output timing



NOTE

- The timings are configured in the TIMING_SPI_CFG register.
- tcsh indicates the CS hold time.
- tcss indicates the CS setup time.
- tshsl indicates the CS deselect time.

4.2.3.8 SPI NAND Flash Address

Table 4-14 describes the address allocation of the SPI NAND flash. The first and second bytes indicate the column address, whereas the third, fourth, and fifth bytes indicate the row address.

Table 4-14 Address allocation of the SPI NAND flash

Byte	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1st byte	A0	A1	A2	A3	A4	A5	A6	A7
2nd byte	A8	A9	A10	A11	A12*	A13*	0	0
3rd byte	A12	A13	A14	A15	A16	A17	A18	A19
4th byte	A20	A21	A22	A23	A24	A25	A26	A27
5th byte*	A28*	A29*	0	0	0	0	0	0

NOTE

- Bits A0−A11 are configured as the valid column address when the page size is 2 KB. Bits A0−A12 are configured as the valid column address when the page size is 4 KB.
- Bit A12 (2 KB page size) and bit A13 (4 KB page size) indicate the plane address only for Micron flash memories. Other vendors do not have the concept of plane address.
- Whether bits A28 and A29 are required depends on the flash memory. If the two bits are not used, the outputs are 0.

When the read and write commands of the SPI NAND flash are issued, the column and row addresses are configured based on the following operations:

- For the write operation, the column address is configured during the loading process and the row address is configured during the programming process.
- For the read operation, the row address is configured when the page is read to cache and the column address is configured during the read operation.

In internal DMA mode, the address command is issued by the FMC. FMC_ADDRL and FMC_ADDRH are configured by software based on the operation address. The configuration values of FMC_ADDRL and FMC_ADDRH are 1st byte−4th byte and 5th byte respectively.

NOTE

- If the page size is 2 KB, bit A12 indicates the plane address. Other meanings of bit A12 are not supported; otherwise, the results of the read and write operations will be affected.
- If the page size is 4 KB, bit A13 indicates the plane address. Other meanings of bit A13 are not supported; otherwise, the results of the read and write operations will be affected.

4.2.4 Working Process

4.2.4.1 Initialization

The initialization process is as follows:

Step 1 Configure the TIMING_SPI_CFG register according to the flash memory if the timing parameters need to be configured.

Step 2 Configure the interface type, ecc_type and page size of the flash memory in the FMC configuration register (FMC_CFG) according to the manual of the connected flash.

Step 3 Switch the address mode of the SPI NOR flash to the 4-byte address mode if the default address mode is 3-byte address mode. For details, see section 4.2.4.4 "Process of Changing the Address Mode of the SPI NOR Flash."

----End

4.2.4.2 Process of Reading or Configuring Component Registers

To read the IDs of the component registers or configure component registers by configuring FMC_OP, perform the following steps:

Step 1 Set ecc_type of the FMC_CFG register to 0.

Step 2 Write the expected operation data from the memory access start address for a register write operation (for example, configure the flash memory configuration register).

Step 3 Configure the operation command, operation address, and number of data segments to be read or written as required in FMC_CMD, FMC_ADDRL, and FMC_DATA_NUM respectively.

Step 4 Configure FMC_OP_CFG based on the component commands that are issued by configuring FMC_OP.

Step 5 Configure FMC_OP to issue commands. For details about the configuration value, see the description of FMC_OP.

Step 6 Check whether the operation is complete by querying of FMC_OP bit[0] in query mode and FMC_INT[op_done_init] in interrupt mode. If FMC_OP bit[0] or FMC_INT[op_done_init] is 1, the operation is complete.

Step 7 Read the value of the component register from the buffer that stores the read results in step 6.

----End

4.2.4.3 Process of Reading the Component Status

To read the component status, perform the following steps:

Step 1 Set FMC_OP[read_status_en] and FMC_OP[reg_op_start] to 1 to issue the component status read command.

Step 2 Store the read result in FMC_STATUS.

----End

4.2.4.4 Process of Changing the Address Mode of the SPI NOR Flash

The SPI NOR flash supports the 3-byte and 4-byte address modes. You can specify the default address mode by pulling up or pulling down the corresponding pin, and dynamically change the address mode by configuring registers after the chip boots.

If the default address mode is the 3-byte address mode and the address mode of the flash memory is 4-byte address mode, perform the following steps to change the address mode after the chip boots:

Step 1 Ensure that the operations on the SPI NOR flash are complete.

Step 2 Configure the related registers to issue the command for changing the address mode of the flash memory to 4-byte address mode in register mode according to the flash memory requirements.

Step 3 Set FMC_CFG [spi_nor_addr_mode] to 1 to change the address mode of the SPI NOR flash from the 3-byte address mode to 4-byte address mode.

----End

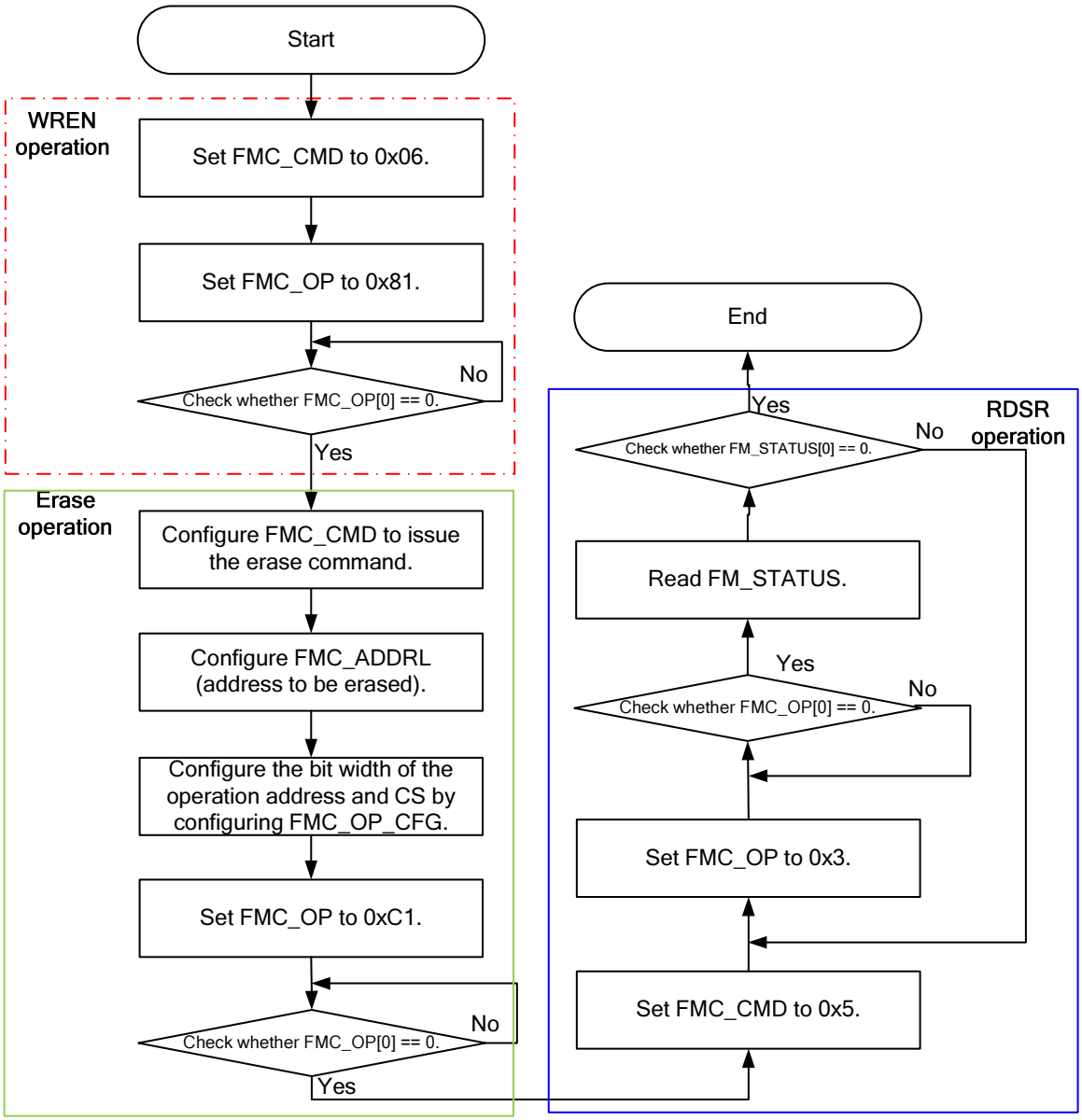
NOTE

For details about the command for changing the address mode of the SPI NOR flash, see the related flash manual.

4.2.4.5 Erase Operation Process

The data in the flash memory must be erased before the program operation is performed. Note that the write enable (WREN) operation must be performed before the erase operation. Figure 4-11 shows an example of erase operation process in query mode.

Figure 4-11 Example of erase operation process



NOTE

- Figure 4-11 shows the erase operation process in query mode. If the interrupt mode is used, check whether FMC_INT[op_done_init] is 1; if yes, the operation is complete.
- During the erase operation, configure the erase instruction and operation address according to the manual of the corresponding flash.

4.2.4.6 Process of Reading Data in Internal DMA Mode

To read data in internal DMA mode, perform the following steps:

Step 1 Start a DMA read operation if FMC_OP_CTRL bit[0] is 0 and the DMA read operation is required.

Step 2 Configure the operation address of the flash memory by configuring FMC_ADDRL and FMC_ADDRH. For the SPI NOR flash, only FMC_ADDRL needs to be configured.

Step 3 Configure the start address for storing data in the DDR by configuring FMC_DMA_SADDR_D0 and FMC_DMA_SADDR_OOB.

- For the SPI NOR flash, FMC_DMA_SADDR_OOB does not need to be configured.
- For the SPI NAND flash, if only the OOB is read, only FMC_DMA_SADDR_OOB needs to be configured.

Step 4 Configure the length of data to be read for the SPI NOR flash and the length of the spare area data to be transferred for the SPI NAND flash in ECC0 mode by configuring FMC_DMA_LEN. Skip this step for other operations on the SPI NAND flash.

Step 5 Configure FMC_OP_CFG based on the requirements of the issued read command.

- Configure FMC_OP_CFG[dummy_num] based on the number of dummy cycles in the read timing.
- Configure FMC_OP_CFG[mem_if_type] based on the SPI required for the read operation.
- Configure FMC_OP_CFG[fm_cs] to select the CS to be operated.

Step 6 Set bit[0] of FMC_OP_CTRL to 1 to issue the flash read command.

- Set FMC_OP_CTRL[rw_op] to 0 to select the DMA read operation.
- For the SPI NAND flash, if only the OOB is read, FMC_OP_CTRL[rd_op_sel] needs to be configured.
- Configure FMC_OP_CTRL[rd_opcode] based on the instruction of the flash read operation.

Step 7 Check whether the read operation is complete by querying FMC_OP_CTRL bit[0] in query mode and FMC_INT[op_done_int] in interrupt mode. If FMC_OP_CTRL bit[0] or FMC_INT[op_done_int] is 1, the read operation is complete, and data is written to the DDR.

----End

NOTE

- For the SPI NAND flash in ECC0 mode, the length configured in FMC_DMA_LEN must be 4-byte-aligned.
- For the SPI NAND flash, the start address for storing data in the DDR must be 4-byte-aligned.

4.2.4.7 Process of Writing Data in Internal DMA Mode

To write data in internal DMA mode, perform the following steps:

Step 1 Start a DMA write operation if FMC_OP_CTRL bit[0] is 0 and the DMA write operation is required.

Step 2 Configure the operation address of the flash memory by configuring FMC_ADDRL and FMC_ADDRH. For the SPI NOR flash, only FMC_ADDRL needs to be configured.

Step 3 Configure the start address for transferring data from the DDR by configuring FMC_DMA_SADDR_D0 and FMC_DMA_SADDR_OOB. For the SPI NOR flash, FMC_DMA_SADDR_OOB does not need to be configured.

Step 4 Configure the length of data to be transferred for the SPI NOR flash and the length of the spare area data to be transferred for the SPI NAND flash in ECC0 mode by configuring FMC_DMA_LEN. Skip this step for other operations on the SPI NAND flash.

Step 5 Configure FMC_OP_CFG based on the requirements of the issued write command.

- Configure FMC_OP_CFG[mem_if_type] based on the SPI required for the write operation.
- Configure FMC_OP_CFG[fm_cs] to select the CS to be operated.

Step 6 Configure FMC_OP_CTRL to issue corresponding commands.

- Set FMC_OP_CTRL[rw_op] to 1 to select the DMA write operation.
- Configure FMC_OP_CTRL[wr_opcode] based on the instruction of the flash program operation.

Step 7 Check whether the write operation is complete by querying FMC_OP_CTRL bit[0] in query mode and FMC_INT[op_done_int] in interrupt mode. If FMC_OP_CTRL bit[0] is 0 or FMC_INT[op_done_int] is 1, the write operation is complete, and data is written to the flash memory.

----End

NOTE

- For the SPI NAND flash in ECC0 mode, the length configured in FMC_DMA_LEN must be 4-byte-aligned.
- For the SPI NAND flash, the start address for storing data in the DDR must be 4-byte-aligned.

4.2.4.8 Notes

Note the following:

- You must reset the SPI NAND flash before use or after exceptions occur.
- You are advised not to configure registers when FMC_OP_CTRL [dma_op_ready] or FMC_OP [reg_op_start] is 1, indicating that the controller is performing an operation. Otherwise, the operation may become abnormal.

4.2.5 Data Storage Structure

The data storage structure of the SPI NAND flash is different from that of the driver software because the ECC needs to be inserted and the bad block flag must be in the default position specified by the vendor. The following describes the format of data prepared by software and the data storage structure in the components.

Non-ECC Mode

When the FMC does not need to perform the ECC:

- During write operations, the FMC transparently writes the data in buffers to the SPI NAND flash without processing.
- During read operations, the FMC writes data read from the SPI NAND flash to the internal buffers without processing.
- The number of bytes of the read and written data is set by the **FMC**_DATA_NUM register.
- The non-ECC mode is used when the ID is read or features are configured and obtained.

4.2.5.2 Data Storage Structure of the Driver Software

2 KB Page Size

Figure 4-12 shows the data structure of the driver (2 KB page size).

Figure 4-12 Data structure of the driver (2 KB page size)

BB: bad block, 2 bytes
CTRL: control area for software, 6 bytes for the 16-bit ECC and 30 bytes for other ECCs

4 KB Page Size

Figure 4-13 shows the data structure of the driver (4 KB page size).

Figure 4-13 Data structure of the driver (4 KB page size)

BB: bad block, 2 bytes
CTRL: control area for software, 14 bytes for the 16-bit ECC and 30 bytes for other ECCs

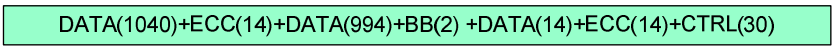
4.2.5.3 8-Bit ECC Mode

2 KB Page Size

Figure 4-14 shows the data structure of the SPI NAND flash in 8-bit ECC mode (2 KB page size). The software valid data is divided into two 1040-byte data segments, and the ECC is calculated for each data segment. When being written to the SPI NAND flash, the data is

automatically stored in two groups in the alternate form of 1040-byte data+14-byte ECC. The bad block information is stored in the first two bytes of the SPI NAND flash spare area.

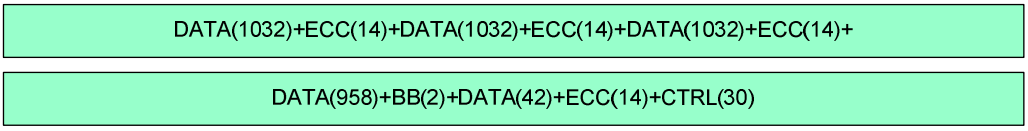
Figure 4-14 Data structure of the SPI NAND flash in 8-bit ECC mode (2 KB page size)



4 KB Page Size

Figure 4-15 shows the data structure of the SPI NAND flash in 8-bit ECC mode (4 KB page size). The software valid data is divided into four 1032-byte data segments, and the ECC is calculated for each data segment. Data written to the SPI NAND flash is automatically stored in three groups in the alternate form of 1032-byte data+14-byte ECC. For the last group (1032-byte data+14-byte ECC), the bad block flag is inserted in byte 4096 of the SPI NAND flash.

Figure 4-15 Data structure of the SPI NAND flash in 8-bit ECC mode (4 KB page size)

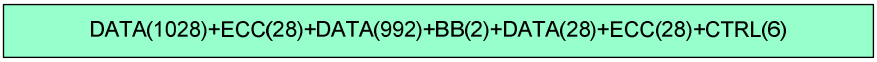


4.2.5.4 16-Bit ECC Mode

2 KB Page Size

Figure 4-16 shows the data structure of the SPI NAND flash in 16-bit ECC mode (2 KB page size). The 2056-byte software valid data is divided into two 1028-byte data segments, and the 28-byte ECC is calculated for each data segment. Then the data segments and ECC are written to the SPI NAND flash alternately.

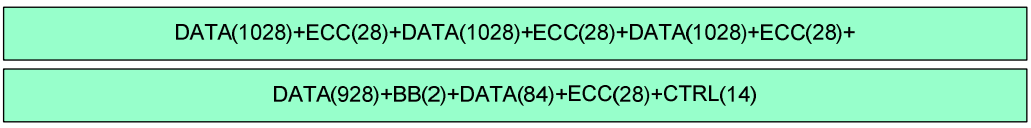
Figure 4-16 Data structure of the SPI NAND flash in 16-bit ECC mode (2 KB page size)



4 KB Page Size

Figure 4-17 shows the data structure of the SPI NAND flash in 16-bit ECC mode (4 KB page size). The software valid data is divided into four 1032-byte data segments, and the ECC is calculated for each data segment. Data written to the SPI NAND flash is automatically stored in three groups in the alternate form of 1032-byte data+28-byte ECC. For the last group (1032-byte data+28-byte ECC), the bad block flag is inserted in byte 4096 of the SPI NAND flash.

Figure 4-17 Data structure of the SPI NAND flash in 16-bit ECC mode (4 KB page size)

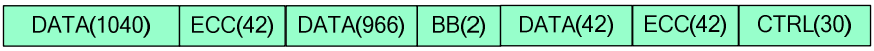


4.2.5.5 24-Bit ECC Mode

2 KB Page Size

Figure 4-18 shows the data structure of the SPI NAND flash in 24-bit ECC mode (2 KB page size). The bad block flag is inserted in byte 2048 of the SPI NAND flash.

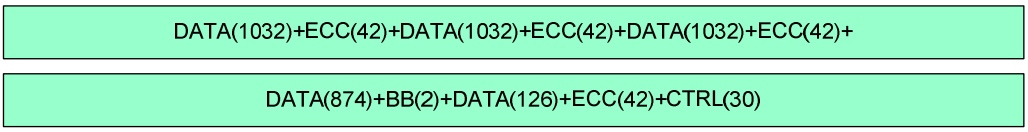
Figure 4-18 Data structure of the SPI NAND flash in 24-bit ECC mode (2 KB page size)



4 KB Page Size

Figure 4-19 shows the data structure of the SPI NAND flash in 24-bit ECC mode (4 KB page size). The data is divided into four 1024 bytes+8 bytes data segments, and a 42-byte ECC is calculated for each data segment. When being written to the SPI NAND flash, data and ECC in the first three data segments are stored in the alternative form. For the last data segment (1024 bytes+8 bytes+42 bytes), the bad block flag is inserted in byte 4096 of the SPI NAND flash.

Figure 4-19 Data structure of the SPI NAND flash in 24-bit ECC mode (4 KB page size)

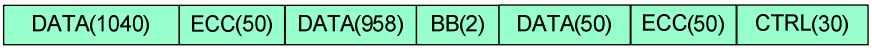


4.2.5.6 28-Bit ECC Mode

2 KB Page Size

Figure 4-20 shows the data structure of the SPI NAND flash in 28-bit ECC mode (2 KB page size). The bad block flag is inserted in byte 2048 of the SPI NAND flash.

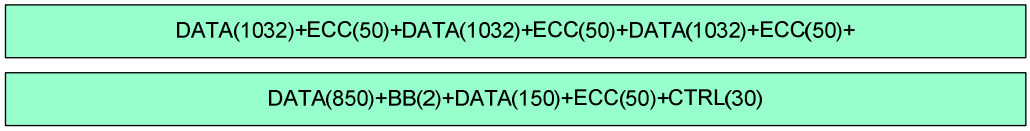
Figure 4-20 Data structure of the SPI NAND flash in 28-bit ECC mode (2 KB page size)



4 KB Page Size

Figure 4-21 shows the data structure of the SPI NAND flash in 28-bit ECC mode (4 KB page size). The data is divided into four 1024 bytes+8 bytes data segments, and a 50-byte ECC is calculated for each data segment. When being written to the SPI NAND flash, data and ECC in the first three data segments are stored in the alternative form. For the last data segment (1024 bytes+8 bytes+50 bytes), the bad block flag is inserted in byte 4096 of the SPI NAND flash.

Figure 4-21 Data structure of the SPI NAND flash in 28-bit ECC mode (4 KB page size)



4.2.6 ECC Mode Selection

The ECC IP used by the controller processes data based on 1 KB data block. Therefore, the ECC performance of the controller is described in the format of *n* bits/1 KB, for example, 8 bits/1 KB or 24 bits/1 KB. To ensure component reliability, the recommended ECC performance of 1 bit/512 bytes, 4 bits/512 bytes, or 8 bits/512 bytes is provided in the component data sheet. The ECC performance of 8 bits/1 KB is equivalent to that of 4 bits/512 bytes. When you select the ECC mode for the controller, note the following:

- The priority of the ECC performance of the controller is higher than or equal to that of the recommended ECC performance.

  For example, if the recommended ECC performance is 1 bit/512 bytes or 4 bits/512 bytes, the controller can select the ECC mode with the performance of 8 bits/1 KB.
- The component page size must be greater than or equal to the required storage size of the ECC mode for the controller.

  For example, if the component page size is (2 KB + 64 bytes), the controller cannot select the ECC mode with the performance of 24 bits/1 KB because the required storage size of this ECC mode is (2 KB + 116 bytes). For details about the required storage size for the ECC mode, see section 4.2.5 "Data Storage Structure."

4.2.7 FMC Registers

4.2.7.1 Register Summary

Table 4-15 describes FMC registers.

Table 4-15 Summary of FMC registers (base address of 0x1000_0000)

Offset Address	Register	Description	Page
0x0000	FMC_CFG	Component configuration register	4-251
0x0004	GLOBAL_CFG	Global configuration register	4-252
0x0008	TIMING_SPI_CFG	SPI timing configuration register	4-252
0x0018	FMC_INT	Interrupt status register	4-253
0x001C	FMC_INT_EN	Interrupt enable register	4-254
0x0020	FMC_INT_CLR	Interrupt clear register	4-256
0x0024	FMC_CMD	Command word configuration register	4-256
0x0028	FMC_ADDRH	Upper-byte component address configuration register	4-257

Offset Address	Register	Description	Page
0x002C	FMC_ADDRL	Lower-byte component address configuration register	4-257
0x0030	FMC_OP_CFG	Operation configuration register	4-257
0x0038	FMC_DATA_NUM	Data length register	4-258
0x003C	FMC_OP	Operation register	4-259
0x0040	FMC_DMA_LEN	DMA operation length register	4-260
0x0048	FMC_DMA_AHB_CTRL	DMA AHB bus control register	4-261
0x004C	FMC_DMA_SADDR_D0	DDR start address register 0 for DMA operations	4-261
0x005C	FMC_DMA_SADDR_OOB	DDR OOB information storage start address register for DMA operations	4-262
0x0068	FMC_OP_CTRL	DMA Operation control register	4-262
0x006C	FMC_TIMEOUT_WR	Write operation timeout register	4-263
0x0070	FMC_OP_PARA	Data segment ID register for reading/writing to the SPI NAND flash in DMA mode	4-263
0x0074	FMC_BOOT_SET	Boot setting register	4-264
0x0078	FMC_LP_CTRL	Low-power control register	4-265
0x00A8	FMC_ERR_THD	ECC alarm threshold register	4-265
0x00AC	FMC_STATUS	Component operating status register	4-266
0x00B4	FMC_MEM_CTRL	SRAM pin configuration register	4-266
0x00BC	VERSION	Version register	4-267
0x00C0	FMC_ERR_NUM0_BUF0	SPI NAND flash error correction information 0 statistics register for the first buffer operation	4-267
0x00D0	FMC_ERR_ALARM_ADDRH	Upper-byte ECC alarm flash address register	4-268
0x00D4	FMC_ERR_ALARM_ADDRL	Lower-byte ECC alarm flash address register	4-268
0x00D8	FMC_ECC_INVALID_ADDRH	Upper-byte ECC uncorrectable address register	4-269
0x00DC	FMC_ECC_INVALID_ADDRL	Lower-byte ECC uncorrectable address register	4-269

4.2.8 Register Description

FMC_CFG

FMC_CFG is a component configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	FMC_CFG	0x0000_1820

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					spi_nor_addr_mode	block_size		ecc_type				page_size		flash_sel	op_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10]	RW	spi_nor_addr_mode	SPI address mode (valid only for the SPI NOR flash) 0: (default): 3-byte address mode 1: 4-byte address mode
[9:8]	RW	block_size	Block size of the SPI NAND flash 00: 64 pages Other values: reserved
[7:5]	RW	ecc_type	ECC type of the controller 000: no ECC 001: 8-bit ECC 010: 16-bit ECC 011: 24-bit ECC 100: 28-bit ECC Other values: reserved
[4:3]	RW	page_size	Page size of the SPI NAND flash 00: 2 KB page size 01: 4 KB page size Other values: reserved

[2:1]	RW	flash_sel	Flash type select 00: SPI NOR flash 01: SPI NAND flash Other values: reserved The reset value is determined by the FMC_FLASH_SEL pin.
[0]	RW	op_mode	FMC operation mode 0: boot mode 1: normal mode

GLOBAL_CFG

GLOBAL_CFG is a global configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	GLOBAL_CFG	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									wp_en				reserved				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	wp_en	Write protection enable for the WP pin. When this bit is enabled, the chip outputs 0 to the WP pin. 0: disabled 1: enabled
[5:0]	RO	reserved	Reserved

TIMING_SPI_CFG

TIMING_SPI_CFG is an SPI timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	TIMING_SPI_CFG	0x0000_066F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				tcsh				tcss				tshsl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	1	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	tcsh	CS hold time 000−111: (*n* + 1) interface clock cycles (*n* = 0, 1, 2, …, 7)
[7:4]	RW	tcss	CS setup time 000−111: (*n* + 1) interface clock cycles (*n* = 0, 1, 2, …, 7)
[3:0]	RW	tshsl	CS deselect time. It is equal to the interval between two flash operations. 0000−1111: (*n* + 1) interface clock cycles (*n* = 0, 1, 2, …, 15)

FMC_INT

FMC_INT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0018	FMC_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ahb_op_int	reserved	dma_err_int	err_alarm_int	err_inval_int	err_val_int	op_fail_int	op_done_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	ahb_op_int	CPU read/write internal buffer interrupt enable when the FMC is reading/writing data from/to the flash memory 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	reserved	Reserved

[5]	RO	dma_err_int	DMA transfer bus error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	err_alarm_int	ECC alarm interrupt. An interrupt is generated when the number of error bits reaches the preset threshold. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	err_inval_int	Uncorrectable ECC error interrupt In 8-bit ECC mode, if errors occur in eight or more bits of the checked 1024-byte data, an interrupt is generated. In 16-bit ECC mode, if errors occur in 16 or more bits of the checked 1024-byte data, an interrupt is generated. In 24-bit ECC mode, if errors occur in 24 or more bits of the checked 1024-byte data, an interrupt is generated. In 28-bit ECC mode, if errors occur in 28 or more bits of the checked 1024-byte data, an interrupt is generated. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	err_val_int	Correctable ECC error interrupt In 8-bit ECC mode, if errors occur in one to eight bits of the checked 1024-byte data, an interrupt is generated. In 16-bit ECC mode, if errors occur in one to 16 bits of the checked 1024-byte data, an interrupt is generated. In 24-bit ECC mode, if errors occur in one to 24 bits of the checked 1024-byte data, an interrupt is generated. In 28-bit ECC mode, if errors occur in one to 28 bits of the checked 1024-byte data, an interrupt is generated. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	op_fail_int	Programming (timeout) failure interrupt in DMA mode 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	op_done_int	Current controller operation completion interrupt. This bit is automatically cleared when the operation register is written. 0: No interrupt is generated. 1: An interrupt is generated.

FMC_INT_EN

FMC_INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x001C	FMC_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ahb_op_int_en	reserved	dma_err_int_en	err_alarm_int_en	err_inval_int_en	err_val_int_en	op_fail_int_en	op_done_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	ahb_op_int_en	CPU read/write internal buffer error interrupt enable when the FMC is reading/writing data from/to the flash memory 0: disabled 1: enabled
[6]	RW	reserved	Reserved
[5]	RW	dma_err_int_en	DMA transfer bus error interrupt enable 0: disabled 1: enabled
[4]	RW	err_alarm_int_en	ECC alarm interrupt enable. An interrupt is generated when the number of error bits reaches the threshold 0: disabled 1: enabled
[3]	RW	err_inval_int_en	ECC uncorrectable error interrupt enable 0: disabled 1: enabled
[2]	RW	err_val_int_en	ECC correctable error interrupt enable 0: disabled 1: enabled
[1]	RW	op_fail_int_en	Programming operation failure interrupt enable in DMA mode 0: disabled 1: enabled
[0]	RW	op_done_int_en	Current operation completion interrupt enable of the FMC 0: disabled 1: enabled

FMC_INT_CLR

FMC_INT_CLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0020	FMC_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ahb_op_int_clr	reserved	dma_err_int_clr	err_alarm_int_clr	err_inval_int_clr	err_val_int_clr	op_fail_int_clr	op_done_int_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	WC	ahb_op_int_clr	ahb_op_err interrupt clear. Writing 1 clears the interrupt.
[6]	WC	reserved	Reserved
[5]	WC	dma_err_int_clr	DMA transfer bus error interrupt clear. Writing 1 clears the interrupt.
[4]	WC	err_alarm_int_clr	err_alarm interrupt clear. Writing 1 clears the interrupt.
[3]	WC	err_inval_int_clr	err_invalid interrupt clear. Writing 1 clears the interrupt.
[2]	WC	err_val_int_clr	err_valid interrupt clear. Writing 1 clears the interrupt.
[1]	WC	op_fail_int_clr	op_fail interrupt clear. Writing 1 clears the interrupt.
[0]	WC	op_done_int_clr	op_done interrupt clear. Writing 1 clears the interrupt.

FMC_CMD

FMC_CMD is a command word configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	FMC_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								cmd1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

[7:0]	RW	cmd1	commands sent to the SPI NOR/SPI NAND flash

FMC_ADDRH

FMC_ADDRH is an upper-byte component address configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	FMC_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	addrh	Upper-byte of the operation address for the SPI NAND flash

FMC_ADDRL

FMC_ADDRL is a lower-byte component address configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	FMC_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	addrl	Lower-byte of the operation address for the flash memory, and component address for the SPI NOR flash

FMC_OP_CFG

FMC_OP_CFG is an operation configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	FMC_OP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				fm_cs	force_cs_en	mem_if_type		addr_num				dummy_num			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	fm_cs	CS corresponding to the flash to be operated used for register operation and invalid for DMA operations 0: CS0 1: CS1
[10]	RW	force_cs_en	CS forcible pull-down enable 0: disabled 1: enabled
[9:7]	RW	mem_if_type	SPI flash interface type select (read operation) 000: standard SPI 001: dual-output/dual-input SPI 010: dual I/O SPI 011: quad-output/quad-input SPI 100: quad I/O SPI 101−111: reserved
[6:4]	RW	addr_num	Number of bytes of the address sent to the flash
[3:0]	RW	dummy_num	Number of bytes to be operated for dummy_en (one byte is equivalent to two clock cycles in 4-wire mode, four clock cycles in 2-wire mode, or eight clock cycles in 1-wire mode)

FMC_DATA_NUM

FMC_DATA_NUM is a data length register.

Offset Address	Register Name	Total Reset Value
0x0038	FMC_DATA_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				op_data_num											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved.
[13:0]	RW	op_data_num	Length of data to be processed during one operation. This register needs to be configured when there is data transfer and does not need to be configured for the DMA operations. This register is valid for the SPI NAND flash only in ECC0 mode.

FMC_OP

FMC_OP is an operation register.

Offset Address	Register Name	Total Reset Value
0x003C	FMC_OP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							dummy_en	cmd1_en	addr_en	write_data_en	reserved			read_data_en	read_status_en	reg_op_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	dummy_en	Dummy byte transfer enable after the address operation is enabled 0: disabled 1: enabled
[7]	RW	cmd1_en	Enable for transmitting command 1 to the flash 0: disabled 1: enabled
[6]	RW	addr_en	Enable for writing the operation address to the flash 0: disabled 1: enabled

[5]	RW	write_data_en	Enable for writing data to the flash 0: disabled 1: enabled Note: read_data_en and write_data_en cannot be 1 at the same time.
[4:3]	RO	reserved	Reserved
[2]	RW	read_data_en	Enable for reading data from the flash 0: disabled 1: enabled Note: read_data_en and write_data_en cannot be 1 at the same time.
[1]	RW	read_status_en	Read component status register enable 0: disabled 1: enabled When this bit is 1, the value of the FMC read component FMC_STATUS is written in the fm_status field of the status register instead of the internal butter.
[0]	RWSC	reg_op_start	Controller status when commands are issued by configuring the FMC_OP register 0: The controller is ready. This bit can be set only to 1 when software issues the command, indicating that the logic is enabled. 1: The controller is busy. This bit is automatically set to 0 after the operation is complete, indicating that the logic is complete.

FMC_DMA_LEN

FMC_DMA_LEN is a DMA operation length register.

Offset Address	Register Name	Total Reset Value
0x0040	FMC_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dma_len																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	dma_len	Data transfer length for DMA operations, in byte. This register is used to configure the spare area length of the SPI NAND flash in ECC0 mode and length of the data to be read from or written to the SPI NOR flash in DMC mode.

FMC_DMA_AHB_CTRL

FMC_DMA_AHB_CTRL is a DMA AHB bus control register.

Offset Address	Register Name	Total Reset Value
0x0048	FMC_DMA_AHB_CTRL	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													burst16_en	burst8_en	burst4_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	burst16_en	Burst16 enable 0: disabled 1: enabled
[1]	RW	burst8_en	Burst8 enable 0: disabled 1: enabled
[0]	RW	burst4_en	Burst4 enable 0: disabled 1: enabled

FMC_DMA_SADDR_D0

FMC_DMA_SADDR_D0 is DDR start address register 0 for DMA operations.

Offset Address	Register Name	Total Reset Value
0x004C	FMC_DMA_SADDR_D0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_d0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_d0	For the SPI NOR flash, this register indicates the DDR start address register for DMA operations. For the SPI NAND flash, this register indicates the DDR operation data base address register for DMA operations.

FMC_DMA_SADDR_OOB

FMC_DMA_SADDR_OOB is a DDR OOB information storage start address register for DMA operations.

Offset Address	Register Name	Total Reset Value
0x005C	FMC_DMA_SADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_oob	DDR base address for the OOB area that stores the data to be read or written

FMC_OP_CTRL

FMC_OP_CTRL is an DMA operation control register.

Offset Address	Register Name	Total Reset Value
0x0068	FMC_OP_CTRL	0x0003_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rd_opcode								wr_opcode								reserved				rd_op_sel		reserved		rw_op	dma_op_ready
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	rd_opcode	SPI NAND/SPI NOR flash, DMA read command, non-bus mode (FAST_READ/READ/DUAL_READ)
[15:8]	RW	wr_opcode	SPI NAND/SPI NOR flash, DMA write command
[7:6]	RO	reserved	Reserved
[5:4]	RW	rd_op_sel	Area of data to be read 00: The whole page is read. 01: Only the OOB is read. 1x: reserved
[3:2]	RO	reserved	Reserved

[1]	RW	rw_op	DMA write/read mode select 0: DMA read mode 1: DMA write mode
[0]	RWSC	dma_op_ready	Controller status when commands are issued by configuring the FMC_OP_CTRL register 0: The controller is ready. This bit can be set only to 1 when software issues the command, indicating that the logic is enabled. 1: The controller is busy. This bit is automatically set to 0 after the operation is complete, indicating that the logic is complete.

FMC_TIMEOUT_WR

FMC_TIMEOUT_WR is a write operation timeout register.

Offset Address	Register Name	Total Reset Value
0x006C	FMC_TIMEOUT_WR	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								timeout_wr																							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	timeout_wr	Program operation busy wait time, timeout period. The timeout period is in the unit of one interface clock cycle for the SPI NAND/SPI NOR flash.

FMC_OP_PARA

FMC_OP_PARA is a data segment ID register for reading/writing to the SPI NAND flash in DMA mode.

Offset Address	Register Name	Total Reset Value
0x0070	FMC_OP_PARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rd_oob_only	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	rd_oob_only	Only the sector that stores the OOB information is read when the flash read command is issued.
[0]	RO	reserved	Reserved

FMC_BOOT_SET

FMC_BOOT_SET is a boot setting register.

Offset Address	Register Name	Total Reset Value
0x0074	FMC_BOOT_SET	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											bb_err	reserved		boot_quad_mode	boot_page0_cfg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	bb_err	Boot failure information 0: bootable 1: boot failure
[3:2]	RO	reserved	Reserved

[1]	RW	boot_quad_mode	Whether to use the 4-wire boot mode for the SPI NAND flash. The reset value is determined by the pin. 0: no. The 1-wire boot mode is used. 1: yes
[0]	RW	boot_page0_cfg	Boot mode select 0: default boot mode 1: boot mode without configuring pins The reset value is determined by the boot_page0_cfg pin.

FMC_LP_CTRL

FMC_LP_CTRL is a low-power control register.

Offset Address	Register Name	Total Reset Value
0x0078	FMC_LP_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								clk_gate_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	clk_gate_en	Clock gating select. If the clock gating is enabled, the low-power design is used and the module working clocks are disabled by logic. 0: All clocks are enabled. 1: Clocks are disabled according to the low-power design.

FMC_ERR_THD

FMC_ERR_THD is an ECC alarm threshold register.

Offset Address	Register Name	Total Reset Value
0x00A8	FMC_ERR_THD	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_err_thd							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	fmc_err_thd	ECC alarm threshold. When the number of error bits reaches the threshold, an ECC alarm interrupt is triggered. NOTE • If an uncorrectable ECC error occurs, an uncorrectable interrupt is reported regardless of the register value. • When the register value is set to 0 or 1, an alarm interrupt is reported as long as an error occurs. • When the configured value exceeds the number of correctable error bits, no alarm interrupt is reported regardless of the number of error bits. Only the correctable error interrupt and uncorrectable error interrupt are generated.

FMC_STATUS

FMC_STATUS is a component operating status register.

Offset Address	Register Name	Total Reset Value
0x00AC	FMC_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fm_status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	fm_status	Component operating status

FMC_MEM_CTRL

FMC_MEM_CTRL is an SRAM pin configuration register.

Offset Address	Register Name	Total Reset Value
0x00B4	FMC_MEM_CTRL	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												mem_ctrl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:3]	RW	mem_emaw	EMAW pin configuration for the single-port SRAM
[2:0]	RW	mem_ema	EMA pin configuration for the single-port SRAM; configuration values of the EMAA and EMAB pins for the dual-port SRAM

VERSION

VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0x00BC	VERSION	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	FMC V100

FMC_ERR_NUM0_BUF0

FMC_ERR_NUM0_BUF0 is an SPI NAND flash error correction information 0 statistics register for the first buffer operation.

Offset Address	Register Name	Total Reset Value
0x00C0	FMC_ERR_NUM0_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num0_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num0_buf0	Number of error bits in the 4 KB data when the page size is 2 KB bit[31:24]: number of error bits in the fourth 1 KB data bit[23:16]: number of error bits in the third 1 KB data bit[15:8]: number of error bits in the second 1 KB data bit[7:0]: number of error bits in the first 1 KB data

FMC_ERR_ALARM_ADDRH

FMC_ERR_ALARM_ADDRH is an upper-byte ECC alarm flash address register.

Offset Address	Register Name	Total Reset Value
0x00D0	FMC_ERR_ALARM_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_err_alarm_addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	fmc_err_alarm_addrh	Upper bytes of the operation address of the flash that triggers the last interrupt when an ECC alarm interrupt is generated

FMC_ERR_ALARM_ADDRL

FMC_ERR_ALARM_ADDRL is a lower-byte ECC alarm flash address register.

Offset Address	Register Name	Total Reset Value
0x00D4	FMC_ERR_ALARM_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fmc_err_alarm_addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fmc_err_alarm_addrl	Lower bytes of the operation address of the flash that triggers the last interrupt when an ECC alarm interrupt is generated

FMC_ECC_INVALID_ADDRH

FMC_ECC_INVALID_ADDRH is an upper-byte ECC uncorrectable address register.

Offset Address	Register Name	Total Reset Value
0x00D8	FMC_ECC_INVALID_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_ecc_invalid_addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	fmc_ecc_invalid_addrh	Upper bytes of the operation address of the flash that triggers the last interrupt when an uncorrectable ECC error occurs

FMC_ECC_INVALID_ADDRL

FMC_ECC_INVALID_ADDRL is a lower-byte ECC uncorrectable address register.

Offset Address	Register Name	Total Reset Value
0x00DC	FMC_ECC_INVALID_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fmc_ecc_invalid_addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fmc_ecc_invalid_addrl	Lower bytes of the operation address of the flash that triggers the last interrupt when an uncorrectable ECC error occurs

Contents

Figures

5 GSF

5.1 Overview

The gigabit switch fabric (GSF) receives and transmits data over two Ethernet ports at 10/100/1000 Mbit/s in full-duplex or half-duplex mode. The Ethernet port exchanges data with the CPU port, and supports the wake on LAN (WoL) functions.

5.2 Function Description

The GSF has the following features:

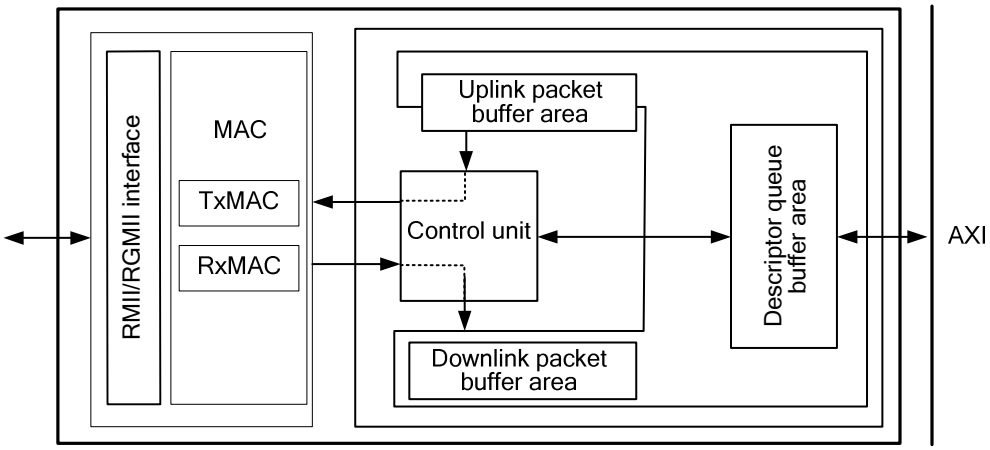
- Supports 10/100/1000 Mbit/s rate.
- Supports the full-duplex or half-duplex mode.
- Supports the media independent interface (MII), reduced media independent interface (RMII), and reduced gigabit media independent interface (RGMII) interfaces.
- Provides the management data input/output (MDIO) interface.
- Supports frame length effectiveness detection and discards long and short frames.
- Supports the cyclic redundancy check (CRC) on receive (RX) frames and discards frames with CRC errors.
- Supports the CRC on transmit (TX) frames.
- Supports short frame filling.
- Supports outloop (that is, line-side loopback) in full-duplex mode.
- Supports count of RX and TX frames.
- Supports filtering of broadcast, multicast, and unicast frames.
- Supports configurable speed control processing of the control packets, IP packets, and broadcast or multicast packets.
- Supports packet filtering.
- Supports the enqueue interrupt and timeout interrupt modes.
- Supports buffer of RX and TX packets.
- Supports WoL.
- Supports scatter gather (SG).
- Supports the TX and RX checksum offload engine (COE).
- Supports TCP segment offload (TSO).

- Supports UDP fragment offload (UFO).

5.3 General Data Flow

Figure 5-1 shows the overall data flow of the GSF GE ports.

Figure 5-1 GSF general data flow



5.4 Port Function Configuration Description

5.4.1 Managing RX and TX Frames

The CPU manages addresses for storing RX and TX frames by configuring the descriptor queue buffer area.

- During reception, the Ethernet module checks whether data packets received from external networks are valid, and then stores the valid packets to the device description repository (DDR) over the bus based on the packet buffer information, including the start address for the packet buffer and packet buffer depth, configured by the CPU.
- During transmission, the Ethernet module obtains the corresponding packets in the DDR over the bus based on the packet buffer information, including the start address for the packet buffer and packet length, configured by the CPU, then packages and transmits the packets to network interfaces.

5.4.2 Configuring Descriptor Queues in RX and TX DDR Buffer Areas

During transmission, the CPU configures the two buffer queues stored in the DDR. During reception, the CPU configures another two buffer queues. The start addresses for the buffer queues are word addresses. A descriptor contains four words and specifies the information about a packet buffer. Table 5-1 describes the data structure of the first two words in the descriptors of the RX and TX buffers.

Table 5-1 Data structure of the first two words in the descriptors of the RX and TX buffers

Name	Width (Bit)	Description
DataBudSAddr	32	Start address of the packet buffer. The byte address format is supported.
DescVld	1	Whether the flag of the descriptor is valid 0: invalid 1: valid
DataLen	11	Valid data volume in the packet buffer (unit: byte)
BufLen	11	Packet buffer depth (unit: byte)

NOTE

The maximum frame length in the RX direction is 1.6 KB, and therefore the space allocated for storing each frame must be greater than 1.6 KB. It is recommended that the space for storing each frame be (1600 + 128) bytes to ensure sufficient space for storing network packet data.

Table 5-2 Data structure of the first two words in the TX buffer

Name	Bit	Bit Name	Description
desc_word1	[31:0]	DataBufSAddr	If the current descriptor is a non-SG descriptor, this bit indicates the start address of the packet buffer. If the current descriptor is an SG descriptor, this bit indicates the start address of the Level-2 linked list.
desc_word2	[31]	hw_own	Ownership of the current descriptor 0: software 1: logic
	[30]	sg_flag	Whether the SG is supported 0: not supported 1: supported Note: When sg_flag is set to 0, tso_flag must be set to 0.
	[29]	coe_flag	Whether checksum offload is executed. 0: no 1: yes
	[28]	tso_flag	Whether TSO is executed 0: no 1: yes
	[27]	reserved	Reserved

Name	Bit	Bit Name	Description
	[26:16]	data_len	When sg_flag is set to 1, this bit indicates the size of the mss in the fragmented packet. When sg_flag is set to 0, this bit indicates the size of the whole packet.
	[15:11]	nfrags_num	Number of nfrags in the SK buffer specified by the current descriptor. The maximum number is 17.
	[10]	vlan_flag	Whether the current packet has a VLAN flag 0: no 1: yes
	[9]	ip_version	IP protocol version of the current packet 0: IPv4 1: IPv6
	[8]	protocol_type	Type of the transmission layer protocol of the current packet 0: TCP 1: UDP
	[7:4]	ip_hdr_len	Length of the IP header of the current packet, in the unit of word (four bytes) If the current packet is an IPv4 packet, the length of the IP header is 5 to 15 words. If the current packet is an IPv6 packet, the length of the IP header is 10 words.
	[3:0]	protocol_hdr_len	If the current packet is a TCP packet, this bit indicates the length of the TCP header, in the unit of word (four bytes). The length ranges from 5 to 15 words. If the current packet is a UDP packet, this bit indicates the length of the UDP header, in the unit of word (four bytes). The length is two words.

5.4.3 Managing RX Interrupts

Generating Interrupts

If the RX enqueue interrupt is enabled and the threshold for reporting the enqueue interrupt is configured, an RX enqueue interrupt is generated when the number of descriptors that the logic writes back to the DDR reaches the configured threshold.

- Enable the rx_bq enqueue interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[17].
- Configure the rx_bq or tx_rq enqueue interrupt threshold register IN_QUEUE_TH bit[7:0].

  Enable the RX timeout interrupt and configure the timeout threshold. After the logic writes back a descriptor, timeout count starts. If the requirements for triggering the RX enqueue interrupt are not met when the timeout count reaches the configured timeout period, an RX timeout interrupt is generated. If the requirements for triggering the RX enqueue and timeout interrupts are met, only the RX enqueue interrupt is generated.
- Enable the rx_bq enqueue timeout interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[28].
- Configure the rx_bq enqueue timeout raw interrupt threshold register RX_BQ_IN_TIMEOUT_TH.

Clearing Interrupts

After the CPU receives an RX enqueue interrupt or RX timeout interrupt, it writes 1 to clear the RX enqueue interrupt and RX timeout interrupt.

5.4.4 Managing TX Interrupts

Generating Interrupts

If the TX enqueue interrupt is enabled and the threshold for reporting the enqueue interrupt is configured, a TX enqueue interrupt is generated when the number of descriptors that the logic writes back to the DDR reaches the configured threshold.

- Enable the tx_rq enqueue interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[19].
- Configure the rx_bq or tx_rq enqueue interrupt threshold register IN_QUEUE_TH bit[23:16].
- Enable the TX timeout interrupt and configure the timeout threshold. After the logic writes back a descriptor, timeout count starts. If the requirements for triggering the RX enqueue interrupt are not met when the timeout count reaches the configured timeout period, a TX timeout interrupt is generated. If the requirements for triggering the TX enqueue and timeout interrupts are met, only the TX enqueue interrupt is generated.
- Enable the tx_bq enqueue timeout interrupt by configuring the PMU raw interrupt register ENA_PMU_INT bit[29].
- Configure the tx_rq enqueue timeout raw interrupt threshold register TX_RQ_IN_TIMEOUT_TH.

Clearing Interrupts

After the CPU receives a TX enqueue interrupt or TX timeout interrupt, it writes 1 to clear the TX enqueue interrupt and TX timeout interrupt.

5.4.5 Configuring the Working Status of the PHY Chip

The GSF provides the MDIO interface to manage the physical layer entity sublayer (PHY) chip. The PHY chip can be written or read through the MDIO interface.

The procedure for reading the PHY chip is as follows:

- The CPU writes the PHY chip address and PHY internal register address to the MDIO single operation register MDIO_SINGLE_CMD bit[12:8] and bit[4:0], respectively, and sets MDIO_SINGLE_CMD bit[20] to 1 and bit[17:16] to 2'b10 to start the MDIO read operation.
- The MDIO writes the data read from the external PHY chip to the MDIO read/write data register MDIO_SINGLE_DATA bit[31:16] and sets the MDIO single operation register MDIO_SINGLE_CMD bit[20] to 0.
- The CPU queries the MDIO read/write data register MDIO_SINGLE_DATA bit[31:16] to obtain the data read by the MDIO from the external PHY chip.

The procedure for writing the PHY chip is as follows:

- The CPU writes the data to be transmitted to the external PHY chip to the MDIO read/write data register MDIO_SINGLE_DATA bit[15:0].
- The CPU writes the PHY chip address and PHY internal register address to the MDIO single operation register MDIO_SINGLE_CMD bit[9:8] and bit[4:0], respectively, and sets MDIO_SINGLE_CMD bit[20] to 1 and bit[17:16] to 1 to start the MDIO write operation.
- The MDIO writes the value of the MDIO read/write data register MDIO_SINGLE_DATA bit[15:0] to the corresponding PHY internal registers and sets the MDIO single operation register MDIO_SINGLE_CMD bit[20] to 0x0.

5.4.6 Switching Operating Modes

The GSF supports the following operating modes and switches between the modes: MII (10M/100Mbit/s), RMII (10/100 Mbit/s) and RGMII (10/100/1000 Mbit/s). The operating mode is switched as follows:

Step 1 Set the corresponding GSF CRG control register 0x12040078 PERI_CRG30 to 0xe to implement the reset, configure bit[8:0] of the GMAC interface control register PERI_CRG35, and set PERI_CRG30 to 0xa to clear the reset so that the configured operating mode takes effect.

Step 2 Enable the MODE_CHANGE_EN register, configure the MAC port rate mode register PORT_MODE, and then disable the MODE_CHANGE_EN register.

NOTE

Do not perform the configuration when the chip is working properly. You are advised to perform the configuration when the chip is initialized.

----End

5.5 Typical Applications

5.5.1 Ethernet Flow Control

The GSF can control the RX packet flow. That is, the GSF discards the subsequent packets when the number of RX packets exceeds the preset maximum quantity.

The GSF controls the flow of the following three types of packets:

- Control packets
- Service packets

- Multicast or broadcast packets

Flow Control of the Control Packets

The flow of control packets is controlled in the following scenarios:

- Within a specified time segment (indicated by T), a limited number of control packets are allowed to pass through. When the count exceeds the configured upper threshold, the subsequent packets are discarded. The time limit T is measured by 125 μs, which is equal to the configured upper threshold.
- If the number of RX addresses of the RX configuration FIFO is less than the number of limited addresses, all RX control packets pass through preferentially. IP packets are filtered out and discarded no matter whether the IP packet flow is controlled or the number of IP packets reaches the configured upper threshold for flow control.

To control the flow of control packets, the following configurations are required:

- Set the control register CONTROL_WORD bit[20] to 1.
- Configure the flow control packet count register FLOW_CTRL_PKG_THRSLD bit[15:0].
- Configure the flow control time threshold register CRF_FLOW_TIME_THRSLD bit[7:0].
- Configure the flow control RX address count register CRF_RX_LEFT_NUM.

Flow Control of Service Packets

The flow control of service packets is the same as that of control packets in the first scenario. In the second scenario, all IP packets will be discarded.

To control the flow of service packets (for example, IP packets), the following configurations are required:

- Set the control register CONTROL_WORD bit[21] to 1.
- Configure the flow control packet count register FLOW_CTRL_PKG_THRSLD bit[31:16].
- Configure the flow control time threshold register CRF_FLOW_TIME_THRSLD bit[7:0].

Flow Control of Broadcast or Multicast Packets

The time limit for flow control of broadcast or multicast packets is 1 μs. Within the time limit, if the count of packets passing through exceeds the upper threshold, the subsequent broadcast or multicast packets are discarded.

To control the flow of broadcast or multicast packets, the following configurations are required:

- Set the control register CONTROL_WORD bit[16] to 1.
- Configure the flow control packet count register for broadcast or multicast packets CRF_BM_PKT_THRSLD.
- Configure the flow control time threshold register for broadcast and multicast packets CRF_BM_TIME_THRSLD.

5.5.2 WoL

The WoL supports wake-up using wake-up frames and magic packets.

Wake_up Frame

The following describes how to configure the filter template by using template 1 as an example (four templates in total):

- Configure valid byte selection register 1 FILTER_0_BYTE_MASK.
- Configure filter template enable register 1 FILTER_COMMAND.
- Configure the CRC position offset register FILTER_OFFSET.
- Configure the software-expected CRC value register FILTER0_1_CRC.
- Set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 1 to enter the power-down mode.
- Set the PMT control and status register PMT_CTRL_STAUTS bit[2] to 1 to enable wake_up frame reception.
- Exit the power-down mode.
  - If you want to exit the power-down mode locally, set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 0.
  - When a wake-up frame is received, the power-down mode is automatically exited. At this time, the Ethernet port automatically receives packets and the software needs to read the raw interrupt register to clear it.

Magic Packet

To receive magic packets, the following configurations are required:

- Set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 1 to enter the power-down mode, and set PMT_CTRL_STAUTS bit[1] to 1 to enable the magic packet reception.
- Exit the power-down mode.
  - If you want to exit the power-down mode locally, set the PMT control and status register PMT_CTRL_STAUTS bit[0] to 0.
  - When a magic packet is received, the power-down mode is automatically exited. At this time, the Ethernet port automatically receives packets and the software needs to read the raw interrupt register to clear it.

5.6 Register Summary

Table 5-3 describes GSF registers.

Table 5-3 Summary of GSF registers (base address: 0x100a_0000)

Offset Address	Register	Description	Page
0x00000000	STATION_ADDR_LOW	Local MAC address register	5-17
0x00000004	STATION_ADDR_HIGH	Local MAC address register	5-17

Offset Address	Register	Description	Page
0x00000008	DUPLEX_SEL_RGMII	Half-duplex selection register	5-18
0x0000000C	FD_FC_TYPE	Flow control frame type domain register	5-18
0x00000014	COL_DISTANCE	Single retransmission packet length threshold register	5-18
0x0000001C	FC_TX_TIMER	Flow control time parameter register	5-19
0x00000020	FD_FC_ADDR_LOW	Flow control frame destination address lower 32 bits register	5-19
0x00000024	FD_FC_ADDR_HIGH	Flow control frame destination address upper 16 bits register	5-20
0x00000030	IPG_TX_TIMER	TX frame inter-packet gap (IPG) register	5-20
0x00000038	PAUSE_THR	TX flow control frame IPG register	5-20
0x0000003C	MAX_FRM_SIZE	Maximum frame length register	5-21
0x00000040	PORT_MODE	Port status register	5-22
0x00000044	PORT_EN	Channel enable register	5-22
0x00000048	PAUSE_EN	Flow control enable register	5-23
0x00000050	SHORT_RUNTS_THR	Short frame threshold register	5-23
0x00000054	DROP_UNK_CTL_FRM	Drop enable register for unknown control frames	5-24
0x00000060	TRANSMIT_CONTROL	Common configuration register	5-24
0x00000064	REC_FILT_CONTROL	RX frame filter control register	5-25
0x00000068	PORT_MC_ADDR_LOW	Multicast address register	5-26
0x0000006C	PORT_MC_ADDR_HIGH	Multicast address register	5-26
0x00000070	MAC_CLR	MAC clear register	5-27
0x00000080	RX_OCTETS_OK_CNT	Byte count register for valid RX frames	5-27
0x00000084	RX_OCTETS_BAD_CNT	Byte count register for error RX frames	5-28
0x00000088	RX_UC_PKTS	MAC frame count register for RX unicast frames	5-28
0x0000008C	RX_MC_PKTS	Frame count register for RX multicast frames	5-28

Offset Address	Register	Description	Page
0x00000090	RX_BC_PKTS	Frame count register for RX broadcast frames	5-29
0x00000094	RX_PKTS_64OCTETS	Frame count register for RX 64-byte frames	5-29
0x00000098	RX_PKTS_65TO127OCTETS	Frame count register for RX frames ranging from 65 bytes to 127 bytes in length	5-29
0x0000009C	RX_PKTS_128TO255OCTETS	Frame count register for RX frames ranging from 128 bytes to 255 bytes in length	5-30
0x000000A0	RX_PKTS_255TO511OCTETS	Frame count register for RX frames ranging from 256 bytes to 511 bytes in length	5-30
0x000000A4	RX_PKTS_512TO1023OCTETS	Frame count register for RX frames ranging from 512 bytes to 1023 bytes in length	5-30
0x000000A8	RX_PKTS_1024TO1518OCTETS	Frame count register for RX frames ranging from 1024 bytes to 1518 bytes in length	5-31
0x000000AC	RX_PKTS_1519TOMAXOCTETS	Frame count register for RX frames ranging from 1519 bytes to the maximum in length	5-31
0x000000B0	RX_FCS_ERRORS	Frame count register for RX frames with CRC errors	5-32
0x000000B4	RX_TAGGED	Frame count register for RX frames with tags	5-32
0x000000B8	RX_DATA_ERR	Frame count register for RX frames with data errors	5-32
0x000000BC	RX_ALIGN_ERRORS	Frame count register for RX frames with byte-alignment errors	5-33
0x000000C0	RX_LONG_ERRORS	Frame count register for RX oversized frames	5-33
0x000000C4	RX_JABBER_ERRORS	Frame count register for RX oversized frames	5-33
0x000000C8	RX_PAUSE_MACCONTROL_FRAMCOUNTER	Frame count register for RX flow control frames	5-34
0x000000CC	RX_UNKNOWN_MACCONTROL_FRAMCOUNTER	Frame count register for RX non-flow-control frames	5-34

Offset Address	Register	Description	Page
0x000000D0	RX_VERY_LONG_ERR_CNT	Frame count register for RX long frames	5-35
0x000000D4	RX_RUNT_ERR_CNT	Frame count register for RX frames less than 64 bytes but greater than or equal to 12 bytes in length	5-35
0x000000D8	RX_SHORT_ERR_CNT	Frame count register for RX frames less than 96 bits in length	5-36
0x00000100	OCTETS_TRANSMITTED_OK	Byte count register for TX normal packets	5-36
0x00000104	OCTETS_TRANSMITTED_BAD	Byte count register for TX bad packets	5-36
0x00000108	TX_UC_PKTS	Frame count register for TX unicast frames	5-37
0x0000010C	TX_MC_PKTS	Frame count register for TX multicast frames	5-37
0x00000110	TX_BC_PKTS	Frame count register for TX broadcast frames	5-37
0x00000114	TX_PKTS_64OCTETS	Frame count register for TX 64-byte frames	5-38
0x00000118	TX_PKTS_65TO127OCTETS	Frame count register for TX frames ranging from 65 bytes to 127 bytes in length	5-38
0x0000011C	TX_PKTS_128TO255OCTETS	Frame count register for TX frames ranging from 128 bytes to 255 bytes in length	5-39
0x00000120	TX_PKTS_255TO511OCTETS	Frame count register for TX frames ranging from 256 bytes to 511 bytes in length	5-39
0x00000124	TX_PKTS_512TO1023OCTETS	Frame count register for TX frames ranging from 512 bytes to 1023 bytes in length	5-40
0x00000128	TX_PKTS_1024TO1518OCTETS	Frame count register for TX frames ranging from 1024 bytes to 1518 bytes in length	5-40
0x0000012C	TX_PKTS_1519TOMAXOCTETS	Frame count register for TX frames greater than 1519 bytes in length	5-41
0x00000144	TX_EXC_COL_ERR_CNT	Count register for packets whose number reaches the maximum retransmission number threshold	5-41

Offset Address	Register	Description	Page
0x0000014C	TX_EXCESSIVE_LENGTH_DROP	Count register for transmission failures caused by oversized frames	5-42
0x00000150	TX_UNDERRUN	Count register for transmission failures caused by internal errors	5-42
0x00000154	TX_TAGGED	Frame count register for TX VLAN frames	5-43
0x00000158	TX_CRC_ERROR	Frame count register for TX frames with valid lengths and CRC errors	5-43
0x0000015C	TX_PAUSE_FRAMES	Frame count register for TX PAUSE frames	5-43
0x000001A8	LINE_LOOP_BACK	Loopback register on the MAC line side	5-44
0x000001B0	CF_CRC_STRIP	CRC strip enable register	5-44
0x000001B4	MODE_CHANGE_EN	Port mode change enable register	5-45
0x000001C0	COL_SLOT_TIME	Count register for half-duplex collision retransmission intervals	5-45
0x000001DC	LOOP_REG	Loopback supplement register	5-46
0x000001E0	RECV_CONTROL	RX control register	5-46
0x000001E8	VLAN_CODE	VLAN code register	5-47
0x000001EC	RX_OVERRUN_CNT	FIFO overrun count register	5-47
0x000001F4	RX_LENGTHFIELD_ERR_CNT	Frame count register for RX frames containing PADs	5-47
0x000001F8	RX_FAIL_COMMA_CNT	COMMA count register for byte delimitation	5-48
0x00000200	MAC_SA_ADDR_L	Source MAC address register	5-48
0x00000204	MAC_SA_ADDR_H	Source MAC address register	5-49
0x00000208	MAC_DA_ADDR_L	Destination MAC address register	5-49
0x0000020C	MAC_DA_ADDR_H	Destination MAC address register	5-49
0x00000210	CRF_MIN_PACKET	Minimum filter packet length register	5-50
0x00000214	CONTROL_WORD	Control register	5-50
0x00000218	FLOW_CTRL_PKG_THRSLD	Flow control packet count register	5-52
0x0000021C	CRF_FLOW_TIME_THRSLD	Flow control time register	5-52

Offset Address	Register	Description	Page
0x00000220+ 4*m	FILTER_LISTm (m ranging from 0 to 15)	Filter list register	5-53
0x00000260	CRF_UDP_NO	UDP port number register	5-53
0x00000264	CRF_TX_FIFO_THRSLD	TX FIFO threshold register	5-54
0x00000268	CRF_RX_FIFO_THRSLD	RX FIFO threshold register	5-54
0x00000280	ERR_GIVEN_PKG_CNT	Count register for dropped packets caused by the frame tailors marked as errors	5-55
0x00000284	SHORT_ERR_PKT_CNT	Short error packet count register	5-55
0x00000288	ERR_FRM_TYPE_CNT	Count register for dropped packets caused by the frame types not listed in the filter list	5-56
0x0000028C	ERR_IP_TYPE_CNT	Count register for dropped packets caused by the IP types not listed in the filter list	5-56
0x00000290	ERR_UDP_CNT	Count register for filtered packets caused by UDP port numbers beyond the specified range	5-57
0x00000294	OVER_FLOW_CNT	Count register for dropped packets caused by the full RX FIFO	5-57
0x00000298	OVER_LENGTH_CNT	Count register for dropped packets whose sizes exceed the upper threshold of the PMU	5-57
0x000002A4	RX_PAUSE_EN	Flow control frame enable register in the RX direction	5-58
0x000002A8	CRF_CFF_DATA_NUM	Configuration FIFO data count register	5-58
0x000002AC	FLOW_OUT_IP_CNT	Count register for dropped IP packets caused by flow control	5-59
0x000002B0	FLOW_OUT_CTRL_CNT	Count register for dropped control packets caused by flow control	5-59
0x00000340	CRF_TX_PAUSE	TX flow control frame control register	5-60
0x00000344	CRF_RX_LEFT_NUM	Flow control RX address count register	5-60
0x00000348	CRF_CTRL_0_TYPE	Control packet type 0 register	5-61
0x0000034C	CRF_CTRL_1_TYPE	Control packet type 1 register	5-61
0x00000350	CRF_CTRL_2_TYPE	Control packet type 2 register	5-61

Offset Address	Register	Description	Page
0x00000354	CRF_CTRL_3_TYPE	Control packet type 3 register	5-62
0x00000358	CRF_BM_PKT_THRSLD	Count threshold register for broadcast/multicast packets under flow control	5-62
0x0000035C	CRF_BM_TIME_THRSLD	Flow control time threshold register for broadcast and multicast packets	5-63
0x000003C0	MDIO_SINGLE_CMD	MDIO single operation register	5-63
0x000003C4	MDIO_SINGLE_DATA	MDIO read/write data register	5-64
0x000003CC	MDIO_CTL	MDIO control register	5-64
0x000003D0	MDIO_RDATA_STATUS	MDIO read data status register	5-66
0x00000500	RX_FQ_START_ADDR	Start address register for the idle descriptor queue	5-66
0x00000504	RX_FQ_DEPTH	Depth register for the idle descriptor queue	5-66
0x00000508	RX_FQ_WR_ADDR	Write address register for the idle descriptor queue	5-67
0x0000050C	RX_FQ_RD_ADDR	Read address register for the idle descriptor queue	5-68
0x00000510	RX_FQ_VLDDESC_CNT	Valid descriptor number register for the idle descriptor queue	5-68
0x00000514	RX_FQ_ALRMPTY_TH	Almost-empty threshold register for the idle descriptor queue	5-69
0x00000518	RX_FQ_REG_EN	Enable register related to idle descriptor queue in the RX direction	5-69
0x0000051C	RX_FQ_ALFULL_TH	Almost-full threshold register for the idle descriptor queue	5-70
0x00000520	RX_BQ_START_ADDR	Start address register for the rx_buff descriptor queue	5-70
0x00000524	RX_BQ_DEPTH	Depth register for the rx_buff descriptor queue	5-71
0x00000528	RX_BQ_WR_ADDR	Write address register for the rx_buff descriptor queue	5-72
0x0000052C	RX_BQ_RD_ADDR	Read address register for the rx_buff descriptor queue	5-72
0x00000530	RX_BQ_FREE_DESC_CNT	Writable descriptor count register for the rx_buff descriptor queue	5-73

Offset Address	Register	Description	Page
0x00000534	RX_BQ_ALEMPTY_TH	Almost-empty threshold register for the rx_buff descriptor queue	5-73
0x00000538	RX_BQ_REG_EN	Enable register related to rx_buff descriptor queue	5-74
0x0000053C	RX_BQ_ALFULL_TH	Almost-full threshold register for the rx_buff descriptor queue	5-75
0x00000580	TX_BQ_START_ADDR	Start address register for the tx_buff descriptor queue	5-75
0x00000584	TX_BQ_DEPTH	Depth register for the tx_buff descriptor queue	5-76
0x00000588	TX_BQ_WR_ADDR	Write address register for the tx_buff descriptor queue	5-76
0x0000058C	TX_BQ_RD_ADDR	Read address register for the tx_buff descriptor queue	5-77
0x00000590	TX_BQ_VLDDESC_CNT	Valid descriptor number register for the tx_buff descriptor queue	5-77
0x00000594	TX_BQ_ALEMPTY_TH	Almost-empty threshold register for the tx_buff descriptor queue	5-78
0x00000598	TX_BQ_REG_EN	Enable register related to tx_buff descriptor queue	5-78
0x0000059C	BQ1_ALFULL_TH	Almost-full threshold register for the tx_buff descriptor queue	5-79
0x000005A0	TX_RQ_START_ADDR	Start address register for the tx_rq descriptor queue	5-79
0x000005A4	TX_RQ_DEPTH	Depth register for the tx_rq descriptor queue	5-80
0x000005A8	TX_RQ_WR_ADDR	Write address register for the tx_rq descriptor queue	5-80
0x000005AC	TX_RQ_RD_ADDR	Read address register for the tx_rq descriptor queue	5-80
0x000005B0	TX_RQ_FREE_DESC_CNT	Writable descriptor count register for the tx_rq descriptor queue	5-81
0x000005B4	TX_RQ_ALEMPTY_TH	Almost-empty threshold register for the tx_rq descriptor queue	5-81
0x000005B8	TX_RQ_REG_EN	Enable register related to the tx_rq descriptor queue	5-82
0x000005BC	TX_RQ_ALFULL_TH	Almost-full threshold register for the tx_rq descriptor queue	5-83

Offset Address	Register	Description	Page
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0x000005C4	ENA_PMU_INT	PMU raw interrupt enable register	5-86
0x000005C8	STATUS_PMU_INT	PMU interrupt status register	5-90
0x000005CC	DESC_WR_RD_ENA	cff read/write descriptor enable register	5-93
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0x000005E8	STOP_CMD	RX and TX packet control stop register	5-96
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0x00000814	U_EEE_TIME_CLK_CNT	Timing pulse count register	5-102
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0x00000A08	FILTER_1_BYTE_MASK	PMT valid byte selection register 1	5-104
0x00000A0C	FILTER_2_BYTE_MASK	PMT valid byte selection register 2	5-105
0x00000A10	FILTER_3_BYTE_MASK	PMT valid byte selection register 3	5-105
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Offset Address	Register	Description	Page
0x00000A20	FILTER2_3_CRC	Software-expected CRC value 2 and 3 register	5-108

5.7 Register Description

STATION_ADDR_LOW

STATION_ADDR_LOW is a local MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000000	STATION_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	station_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	station_addr_low	Lower 32 bits for the source MAC address of MAC_CORE

STATION_ADDR_HIGH

STATION_ADDR_HIGH is a local MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000004	STATION_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																station_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	station_addr_high	Upper 16 bits of the source MAC address of MAC_CORE. The default configurations can be used.

DUPLEX_SEL_RGMII

DUPLEX_SEL_RGMII is a half-duplex selection register.

Offset Address	Register Name	Total Reset Value
0x00000008	DUPLEX_SEL_RGMII	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															duplex_sel_rgmii
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	duplex_sel_rgmii	Half-duplex selection signal 0: half duplex 1: full duplex

FD_FC_TYPE

FD_FC_TYPE is a flow control frame type domain register.

Offset Address	Register Name	Total Reset Value
0x0000000C	FD_FC_TYPE	0x0000_8808

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fd_fc_type															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fd_fc_type	Flow control frame type domain in full-duplex mode

COL_DISTANCE

COL_DISTANCE is a single retransmission packet length threshold register.

Offset Address	Register Name	Total Reset Value
0x00000014	COL_DISTANCE	0x0000_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								col_distance							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	col_distance	Single retransmission packet length threshold

FC_TX_TIMER

FC_TX_TIMER is a flow control time parameter register.

Offset Address	Register Name	Total Reset Value
0x0000001C	FC_TX_TIMER	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fc_tx_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fc_tx_timer	Parameter of the time period during which flow control frames are transmitted. The unit of the time period is measured by how long 512 bits are transmitted. In 100 Mbit/s mode, the unit is equivalent to 128 clock periods. In 1000 Mbit/s mode, the unit is equivalent to 64 clock periods.

FD_FC_ADDR_LOW

FD_FC_ADDR_LOW is a flow control frame destination address lower 32 bits register.

Offset Address	Register Name	Total Reset Value
0x00000020	FD_FC_ADDR_LOW	0xC200_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fd_fc_addr_low																															
Reset	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:0]	RW	fd_fc_addr_low	Lower 32 bits of the destination address of the flow control frame

FD_FC_ADDR_HIGH

FD_FC_ADDR_HIGH is a flow control frame destination address upper 16 bits register.

Offset Address	Register Name	Total Reset Value
0x00000024	FD_FC_ADDR_HIGH	0x0000_0180

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fd_fc_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	fd_fc_addr_high	Upper 16 bits of the destination address of the flow control frame

IPG_TX_TIMER

IPG_TX_TIMER is a TX frame IPG register.

Offset Address	Register Name	Total Reset Value
0x00000030	IPG_TX_TIMER	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ipg_tx_timer							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	ipg_tx_timer	TX frame IPG, in the unit of byte

PAUSE_THR

PAUSE_THR is a TX flow control frame IPG register.

Offset Address	Register Name	Total Reset Value
0x00000038	PAUSE_THR	0x0000_002F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pause_thr															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	pause_thr	IPG of the flow control frame. If the flow control time is longer than the IPG, the MAC transmits the flow control frame automatically. The unit of the time period is measured by how long 512 bits are transmitted. In 100 Mbit/s mode, the unit is equivalent to 128 clock periods. In 1000 Mbit/s mode, the unit is equivalent to 64 clock periods.

MAX_FRM_SIZE

MAX_FRM_SIZE is a maximum frame length register.

Offset Address	Register Name	Total Reset Value
0x0000003C	MAX_FRM_SIZE	0x0000_05EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				max_frm_size											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	1	1	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	max_frm_size	Maximum frame length on the MAC side If the length of an RX frame is greater than the maximum length, the RX frame is regarded as an oversized frame. When the length of a frame to be transmitted is greater than the maximum length, the frame is broken up and then transmitted as an error frame.

PORT_MODE

PORT_MODE is a port status register.

Offset Address	Register Name	Total Reset Value
0x00000040	PORT_MODE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													port_mode		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	port_mode	Current MAC port mode 000: 10 Mbit/s 001: 100 Mbit/s 101: 1000 Mbit/s Other values: reserved

PORT_EN

PORT_EN is a channel enable register.

Offset Address	Register Name	Total Reset Value
0x00000044	PORT_EN	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tx en	rx en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_en	TX channel enable 0: disabled 1: enabled
[1]	RW	rx_en	RX channel enable 0: disabled 1: enabled

[0]	RO	reserved	Reserved

PAUSE_EN

PAUSE_EN is a flow control enable register.

Offset Address	Register Name	Total Reset Value
0x00000048	PAUSE_EN	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														tx fdfc	rx fdfc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	tx_fdfc	Flow control frame transmit enable in full-duplex mode 0: disabled 1: enabled
[0]	RW	rx_fdfc	Flow control frame response enable in full-duplex mode 0: disabled 1: enabled

SHORT_RUNTS_THR

SHORT_RUNTS_THR is a short frame threshold register.

Offset Address	Register Name	Total Reset Value
0x00000050	SHORT_RUNTS_THR	0x0000_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												short_runts_thr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	short_runts_thr	Short frame threshold (for statistics only)

DROP_UNK_CTL_FRM

DROP_UNK_CTL_FRM is a drop enable register for unknown control frames.

Offset Address	Register Name	Total Reset Value
0x00000054	DROP_UNK_CTL_FRM	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															drop_unk_ctl_frm
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	drop_unk_ctl_frm	Processing method of the unknown control frames 0: The unknown control frames are forwarded normally. 1: The unknown control frames are dropped.

TRANSMIT_CONTROL

TRANSMIT_CONTROL is a common configuration register.

Offset Address	Register Name	Total Reset Value
0x00000060	TRANSMIT_CONTROL	0x0000_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pad_enable	crc_add	reserved					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	pad_enable	PAD addition enable 0: disabled 1: enabled
[6]	RW	crc_add	FCS addition enable 0: enabled 1: disabled

[5:0]	RO	reserved	Reserved

REC_FILT_CONTROL

REC_FILT_CONTROL is an RX frame filter control register.

Offset Address	Register Name	Total Reset Value
0x00000064	REC_FILT_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										crc_err_pass	pause_frm_pass	vlan_drop_en	bc_drop_en	mc_match_en	uc_match_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	crc_err_pass	CRC error frame filter enable 0: disabled 1: enabled
[4]	RW	pause_frm_pass	Flow control frame filter enable 0: disabled. This bit takes effect only when flow control is enabled, which is transmitted to the software. 1: enabled. This bit takes effect only when flow control is enabled, which is not transmitted to the software.
[3]	RW	vlan_drop_en	VLAN frame filter enable 0: disabled 1: enabled
[2]	RW	bc_drop_en	Broadcast frame filter enable 0: disabled 1: enabled
[1]	RW	mc_match_en	Multicast frame enable with unmatched DA filter 0: disabled 1: enabled
[0]	RW	uc_match_en	Unicast frame enable with unmatched DA filter 0: disabled 1: enabled

PORT_MC_ADDR_LOW

PORT_MC_ADDR_LOW is a multicast address register.

Offset Address	Register Name	Total Reset Value
0x00000068	PORT_MC_ADDR_LOW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_mc_addr_low																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	port_mc_addr_low	Lower 32 bits of the multicast address, used to check whether the multicast frames match

PORT_MC_ADDR_HIGH

PORT_MC_ADDR_HIGH is a multicast address register.

Offset Address	Register Name	Total Reset Value
0x0000006C	PORT_MC_ADDR_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																port_mc_addr_high															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	port_mc_addr_high	Upper 16 bits of the multicast address, used to check whether the multicast frames match

MAC_CLR

MAC_CLR is a MAC clear register.

Offset Address	Register Name	Total Reset Value
0x00000070	MAC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												soft_rst_mdio	soft_rst_mii	soft_rst_rx	soft_rst_tx
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	soft_rst_mdio	MDIO clear signal 0: invalid 1: valid
[2]	RW	soft_rst_mii	MII clear signal 0: invalid 1: valid
[1]	RW	soft_rst_rx	RX clear signal 0: invalid 1: valid
[0]	RW	soft_rst_tx	TX clear signal 0: invalid 1: valid

RX_OCTETS_OK_CNT

RX_OCTETS_OK_CNT is a byte count register for valid RX frames.

Offset Address	Register Name	Total Reset Value
0x00000080	RX_OCTETS_OK_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_octets_ok_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_octets_ok_cnt	Count of bytes of the valid RX frames, ranging from DA to FCS

RX_OCTETS_BAD_CNT

RX_OCTETS_BAD_CNT is a byte count register for error RX frames.

Offset Address	Register Name	Total Reset Value
0x00000084	RX_OCTETS_BAD_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_octets_bad_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_octets_bad_cnt	Count of bytes of the frames with CRC errors and alignment errors

RX_UC_PKTS

RX_UC_PKTS is a MAC frame count register for RX unicast frames.

Offset Address	Register Name	Total Reset Value
0x00000088	RX_UC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_uc_pkts_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_uc_pkts_cnt	Count of RX unicast frames, excluding bad frames

RX_MC_PKTS

RX_MC_PKTS is a frame count register for RX multicast frames.

Offset Address	Register Name	Total Reset Value
0x0000008C	RX_MC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_mc_pkts_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_mc_pkts_cnt	Count of RX multicast frames, excluding bad frames

RX_BC_PKTS

RX_BC_PKTS is a frame count register for RX broadcast frames.

Offset Address	Register Name	Total Reset Value
0x00000090	RX_BC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bc_pkts_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_bc_pkts_cnt	Count of RX broadcast frames, excluding bad frames

RX_PKTS_64OCTETS

RX_PKTS_64OCTETS is a frame count register for RX 64-byte frames.

Offset Address	Register Name	Total Reset Value
0x00000094	RX_PKTS_64OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pks_64oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pks_64oct_cnt	Count of RX 64-byte frames, including bad frames

RX_PKTS_65TO127OCTETS

RX_PKTS_65TO127OCTETS is a frame count register for RX frames ranging from 65 bytes to 127 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000098	RX_PKTS_65TO127OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pks_65to127_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pks_65to127_oct_cnt	Count of RX frames ranging from 65 bytes to 127 bytes in length, including bad frames

RX_PKTS_128TO255OCTETS

RX_PKTS_128TO255OCTETS is a frame count register for RX frames ranging from 128 bytes to 255 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000009C	RX_PKTS_128TO255OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_128to255_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_128to255_oct_cnt	Count of RX frames ranging from 128 bytes to 255 bytes in length, including bad frames

RX_PKTS_255TO511OCTETS

RX_PKTS_255TO511OCTETS is a frame count register for RX frames ranging from 256 bytes to 511 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000A0	RX_PKTS_255TO511OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_256to511_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_256to511_oct_cnt	Count of RX frames ranging from 256 bytes to 511 bytes in length, including bad frames

RX_PKTS_512TO1023OCTETS

RX_PKTS_512TO1023OCTETS is a frame count register for RX frames ranging from 512 bytes to 1023 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000A4	RX_PKTS_512TO1023OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_512to1023_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_512to1023_oct_cnt	Count of RX frames ranging from 512 bytes to 1023 bytes in length, including bad frames

RX_PKTS_1024TO1518OCTETS

RX_PKTS_1024TO1518OCTETS is a frame count register for RX frames ranging from 1024 bytes to 1518 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000A8	RX_PKTS_1024TO1518OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_1024to1518_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_1024to1518_oct_cnt	Count of RX frames ranging from 1024 bytes to 1518 bytes in length, including bad frames

RX_PKTS_1519TOMAXOCTETS

RX_PKTS_1519TOMAXOCTETS is a frame count register for RX frames ranging from 1519 bytes to the maximum in length.

Offset Address	Register Name	Total Reset Value
0x000000AC	RX_PKTS_1519TOMAXOCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pkts_1519tomax_oct_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pkts_1519tomax_oct_cnt	Count of RX frames ranging from 1519 bytes to the maximum in length, including bad frames

RX_FCS_ERRORS

RX_FCS_ERRORS is a frame count register for RX frames with CRC errors.

Offset Address	Register Name	Total Reset Value
0x000000B0	RX_FCS_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_fcs_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_fcs_errors	Count of RX frames with CRC errors, excluding short frames

RX_TAGGED

RX_TAGGED is a frame count register for RX frames with tags.

Offset Address	Register Name	Total Reset Value
0x000000B4	RX_TAGGED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_tagged																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_tagged	Count of RX frames with tags

RX_DATA_ERR

RX_DATA_ERR is a frame count register for RX frames with data errors.

Offset Address	Register Name	Total Reset Value
0x000000B8	RX_DATA_ERR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_data_err																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_data_err	Count of RX frames with data errors

RX_ALIGN_ERRORS

RX_ALIGN_ERRORS is a frame count register for RX frames with byte-alignment errors.

Offset Address	Register Name	Total Reset Value
0x000000BC	RX_ALIGN_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_align_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_align_errors	Count of RX frames with byte-alignment errors

RX_LONG_ERRORS

RX_LONG_ERRORS is a frame count register for RX oversized frames.

Offset Address	Register Name	Total Reset Value
0x000000C0	RX_LONG_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_long_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_long_errors	Count of RX oversized frames (without CRC errors)

RX_JABBER_ERRORS

RX_JABBER_ERRORS is a frame count register for RX oversized frames.

Offset Address	Register Name	Total Reset Value
0x000000C4	RX_JABBER_ERRORS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_jabber_errors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_jabber_errors	Count of RX oversized frames with CRC errors or non-integer byte count

RX_PAUSE_MACCONTROL_FRAMCOUNTER

RX_PAUSE_MACCONTROL_FRAMCOUNTER is a frame count register for RX flow control frames.

Offset Address	Register Name	Total Reset Value
0x000000C8	RX_PAUSE_MACCONTROL_FRAMCOUNTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_pause_maccontrol_framecounter																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_pause_maccontrol_framecounter	Count of RX flow control frames. The CRC must be correct when it is valid.

RX_UNKNOWN_MACCONTROL_FRAMCOUNTER

RX_UNKNOWN_MACCONTROL_FRAMCOUNTER is a frame count register for RX non-flow-control frames.

Offset Address	Register Name	Total Reset Value
0x000000CC	RX_UNKNOWN_MACCONTROL_FRAMCOUNTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_unknown_maccontrol_framecounter																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_unknown_maccontrol_framecounter	Count of RX non-flow control frames

RX_VERY_LONG_ERR_CNT

RX_VERY_LONG_ERR_CNT is a frame count register for RX long frames.

Offset Address	Register Name	Total Reset Value
0x000000D0	RX_VERY_LONG_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_very_long_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_very_long_err_cnt	Count of RX long frames (with the length more than twice the maximum frame length)

RX_RUNT_ERR_CNT

RX_RUNT_ERR_CNT is a frame count register for RX frames less than 64 bytes but greater than or equal to 12 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000D4	RX_RUNT_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_runt_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_runt_err_cnt	Count of RX frames less than 64 bytes but greater than or equal to 12 bytes in length

RX_SHORT_ERR_CNT

RX_SHORT_ERR_CNT is a frame count register for RX frames less than 12 bytes in length.

Offset Address	Register Name	Total Reset Value
0x000000D8	RX_SHORT_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_short_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_short_err_cnt	Count of RX frames less than 12 bytes in length.

OCTETS_TRANSMITTED_OK

OCTETS_TRANSMITTED_OK is a byte count register for TX normal packets.

Offset Address	Register Name	Total Reset Value
0x00000100	OCTETS_TRANSMITTED_OK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_transmitted_ok																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	octets_transmitted_ok	Count of bytes of the transmitted normal packets, excluding the preambles and SFDs

OCTETS_TRANSMITTED_BAD

OCTETS_TRANSMITTED_BAD is a byte count register for TX bad packets.

Offset Address	Register Name	Total Reset Value
0x00000104	OCTETS_TRANSMITTED_BAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_transmitted_bad																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	octets_transmitted_bad	Count of bytes of the TX bad packets

TX_UC_PKTS

TX_UC_PKTS is a frame count register for TX unicast frames.

Offset Address	Register Name	Total Reset Value
0x00000108	TX_UC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_uc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_uc_pkts	Count of TX unicast frames, excluding bad packets

TX_MC_PKTS

TX_MC_PKTS is a frame count register for TX multicast frames.

Offset Address	Register Name	Total Reset Value
0x0000010C	TX_MC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_mc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_mc_pkts	Count of TX multicast frames, excluding bad packets

TX_BC_PKTS

TX_BC_PKTS is a frame count register for TX broadcast frames.

Offset Address	Register Name	Total Reset Value
0x00000110	TX_BC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_bc_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_bc_pkts	Count of TX broadcast frames, excluding bad packets

TX_PKTS_64OCTETS

TX_PKTS_64OCTETS is a frame count register for TX 64-byte frames.

Offset Address	Register Name	Total Reset Value
0x00000114	TX_PKTS_64OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_64octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_64octets	Count of TX 64-byte frames, including bad packets

TX_PKTS_65TO127OCTETS

TX_PKTS_65TO127OCTETS is a frame count register for TX frames ranging from 65 bytes to 127 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000118	TX_PKTS_65TO127OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_65to127octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_65to127octets	Count of TX frames ranging from 65 bytes to 127 bytes in length, including bad packets

TX_PKTS_128TO255OCTETS

TX_PKTS_128TO255OCTETS is a frame count register for TX frames ranging from 128 bytes to 255 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000011C	TX_PKTS_128TO255OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_128to255octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_128to255octets	Count of TX frames ranging from 128 bytes to 255 bytes in length, including bad packets

TX_PKTS_255TO511OCTETS

TX_PKTS_255TO511OCTETS is a frame count register for TX frames ranging from 256 bytes to 511 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000120	TX_PKTS_255TO511OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_256to511octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_256to511octets	Count of TX frames ranging from 256 bytes to 511 bytes in length, including bad packets

TX_PKTS_512TO1023OCTETS

TX_PKTS_512TO1023OCTETS is a frame count register for TX frames ranging from 512 bytes to 1023 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000124	TX_PKTS_512TO1023OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_512to1023octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_512to1023octets	Count of TX frames ranging from 512 bytes to 1023 bytes in length, including bad packets

TX_PKTS_1024TO1518OCTETS

TX_PKTS_1024TO1518OCTETS is a frame count register for TX frames ranging from 1024 bytes to 1518 bytes in length.

Offset Address	Register Name	Total Reset Value
0x00000128	TX_PKTS_1024TO1518OCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_1024to1518octets																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_1024to1518octets	Count of TX frames ranging from 1024 bytes to 1518 bytes in length, including bad packets

TX_PKTS_1519TOMAXOCTETS

TX_PKTS_1519TOMAXOCTETS is a frame count register for TX frames greater than 1519 bytes in length.

Offset Address	Register Name	Total Reset Value
0x0000012C	TX_PKTS_1519TOMAXOCTETS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pkts_1519tomaxoctes																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pkts_1519tomaxoctes	Count of TX frames greater than 1519 bytes in length, including bad packets

TX_EXC_COL_ERR_CNT

TX_EXC_COL_ERR_CNT is a count register for packets whose number reaches the maximum retransmission number threshold.

Offset Address	Register Name	Total Reset Value
0x00000144	TX_EXC_COL_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_exc_col_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_exc_col_err_cnt	Count of packets whose number reaches the maximum retransmission number threshold

TX_EXCESSIVE_LENGTH_DROP

TX_EXCESSIVE_LENGTH_DROP is a count register for transmission failures caused by oversized frames.

Offset Address	Register Name	Total Reset Value
0x0000014C	TX_EXCESSIVE_LENGTH_DROP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_excessive_length_drop																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_excessive_length_drop	Count of transmission failures caused by oversized frames

TX_UNDERRUN

TX_UNDERRUN is a count register for transmission failures caused by internal errors.

Offset Address	Register Name	Total Reset Value
0x00000150	TX_UNDERRUN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_underrun																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_underrun	Count of transmission failures caused by internal errors

TX_TAGGED

TX_TAGGED is a frame count register for TX VLAN frames.

Offset Address	Register Name	Total Reset Value
0x00000154	TX_TAGGED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_tagged																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_tagged	Count of TX VLAN frames The value of the Type field equals to that of the 0x8100 packet.

TX_CRC_ERROR

TX_CRC_ERROR is a frame count register for TX frames with valid lengths and CRC errors.

Offset Address	Register Name	Total Reset Value
0x00000158	TX_CRC_ERROR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_crc_error																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_crc_error	Count of TX frames with valid lengths and CRC errors

TX_PAUSE_FRAMES

TX_PAUSE_FRAMES is a frame count register for TX PAUSE frames.

Offset Address	Register Name	Total Reset Value
0x0000015C	TX_PAUSE_FRAMES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_pause_frames																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	tx_pause_frames	Count of TX PAUSE frames

LINE_LOOP_BACK

LINE_LOOP_BACK is a loopback register on the MAC line side.

Offset Address	Register Name	Total Reset Value
0x000001A8	LINE_LOOP_BACK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								line_loop_back
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	line_loop_back	MAC line-side loopback enable 0: disabled 1: enabled

CF_CRC_STRIP

CF_CRC_STRIP is a CRC strip enable register.

Offset Address	Register Name	Total Reset Value
0x000001B0	CF_CRC_STRIP	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								cf_crc_strip
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	cf_crc_strip	RX CRC strip enable on the MAC side 0: disabled. The four bytes of the CRC are regarded as part of the packet. 1: enabled. The four bytes of the CRC are stripped from the packet.

MODE_CHANGE_EN

MODE_CHANGE_EN is a port mode change enable register.

Offset Address	Register Name	Total Reset Value
0x000001B4	MODE_CHANGE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mode_change_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	mode_change_en	port_mode change enable 0: disabled 1: enabled

COL_SLOT_TIME

COL_SLOT_TIME is a count register for half-duplex collision retransmission intervals.

Offset Address	Register Name	Total Reset Value
0x000001C0	COL_SLOT_TIME	0x0000_40FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cf2bc_slottime																cf2bc_random_seed							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:8]	RW	cf2bc_slottime	Interval for half-duplex collision retransmission
[7:0]	RW	cf2bc_random_seed	Random multiple radix for half-duplex collision retransmission

LOOP_REG

LOOP_REG is a loopback supplement register.

Offset Address	Register Name	Total Reset Value
0x000001DC	LOOP_REG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cf_ext_drive_lp	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	cf_ext_drive_lp	Generation of the read/write enable signals of the MAC data during loopback on the line side 0: The read/write enable signals are generated in the MAC. 1: The read/write enable signals are generated based on the MAC enable signals read by the downlink FIFO.
[0]	RO	reserved	Reserved

RECV_CONTROL

RECV_CONTROL is an RX control register.

Offset Address	Register Name	Total Reset Value
0x000001E0	RECV_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											runt_pkt_en	strip_pad_en	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved

[4]	RW	runt_pkt_en	Transparent transmission enable of the RX short frames 0: discarded and not transmitted to the software 1: transmitted to the software
[3]	RW	strip_pad_en	PAD for stripping RX frames enable 0: disabled 1: enabled
[2:0]	RO	reserved	Reserved

VLAN_CODE

VLAN_CODE is a VLAN code register.

Offset Address	Register Name	Total Reset Value
0x000001E8	VLAN_CODE	0x0000_8100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cf_vlan_code															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	cf_vlan_code	Ethernet Type field configuration

RX_OVERRUN_CNT

RX_OVERRUN_CNT is a FIFO overrun count register.

Offset Address	Register Name	Total Reset Value
0x000001EC	RX_OVERRUN_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_overrun_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_overrun_cnt	Count of FIFO overruns on the MAC application side

RX_LENGTHFIELD_ERR_CNT

RX_LENGTHFIELD_ERR_CNT is a frame count register for RX frames containing PADs.

Offset Address	Register Name	Total Reset Value
0x000001F4	RX_LENGTHFIELD_ERR_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_lengthfield_err_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_lengthfield_err_cnt	Count of RX frames containing PADs and with the length of not 64 bytes when the PAD strip enable is valid

RX_FAIL_COMMA_CNT

RX_FAIL_COMMA_CNT is a COMMA count register for byte delimitation.

Offset Address	Register Name	Total Reset Value
0x000001F8	RX_FAIL_COMMA_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_fail_comma_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	rx_fail_comma_cnt	Count of COMMA codes when two or more COMMA codes exist during byte delimitation

MAC_SA_ADDR_L

MAC_SA_ADDR_L is a source MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000200	MAC_SA_ADDR_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_sa_addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mac_sa_addr_l	Lower 32 bits of the source MAC address used by the PMU, which are inserted into the lower 32 bits of the source address (SA) field

MAC_SA_ADDR_H

MAC_SA_ADDR_H is a source MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000204	MAC_SA_ADDR_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mac_sa_addr_h															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	mac_sa_addr_h	Upper 16 bits of the source MAC address used by the PMU

MAC_DA_ADDR_L

MAC_DA_ADDR_L is a destination MAC address register.

Offset Address	Register Name	Total Reset Value
0x00000208	MAC_DA_ADDR_L	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_da_addr_l																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mac_da_addr_l	Lower 32 bits of the destination MAC address used by the PMU, which are inserted into the lower 32 bits of the destination address field

MAC_DA_ADDR_H

MAC_DA_ADDR_H is a destination MAC address register.

Offset Address	Register Name	Total Reset Value
0x0000020C	MAC_DA_ADDR_H	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				crf_tx_max_packet												mac_da_addr_h															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26:16]	RW	crf_tx_max_packet	Maximum length of the normal and SG packets allowed by the PMU
[15:0]	RW	mac_da_addr_h	Upper 16 bits of the destination MAC address used by the PMU

CRF_MIN_PACKET

CRF_MIN_PACKET is a minimum filter packet length register.

Offset Address	Register Name	Total Reset Value
0x00000210	CRF_MIN_PACKET	0x0000_0F2A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tso_version												reserved								crf_tx_min_packet				reserved				crf_rx_min_packet			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:20]	RO	tso_version	TSO version 100: single-byte combination version 200: SG or COE version 300: TSO version
[19:14]	RO	reserved	Reserved
[13:8]	RW	crf_tx_min_packet	Minimum length of the TX packet. The default length is 15 bytes.
[7:6]	RO	reserved	Reserved
[5:0]	RW	crf_rx_min_packet	Minimum length of the RX packet. The default length is 42 bytes.

CONTROL_WORD

CONTROL_WORD is a control register.

Offset Address	Register Name	Total Reset Value
0x00000214	CONTROL_WORD	0x00C0_0640

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						crf_tx_standard	reserved			crf_ip_flow_ctrl	crf_ctrl_flow_ctrl	reserved		crf_filt_unused_pkg	crf_bm_flow_ctrl	crf_peel_dsa	crf_add_da_sa	crf_large_packet											
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	crf_tx_standard	Configuration standard for the transmit waterline of the TX FIFO 0: The standard is set based on the packet and empty threshold. If the TX FIFO contains a complete packet or the number of valid data items in the TX FIFO is equal to or greater than the threshold multiplied by 4, a read request is sent to the MAC. 1: The standard is set based on the packet. If the TX FIFO contains a complete packet, a read request is sent to the MAC.
[24:22]	RO	reserved	Reserved
[21]	RW	crf_ip_flow_ctrl	IP packet flow control enable 0: disabled 1: enabled
[20]	RW	crf_ctrl_flow_ctrl	Control packet flow control enable 0: disabled 1: enabled
[19:18]	RO	reserved	Reserved
[17]	RW	crf_filt_unused_pkg	Invalid packets filter enable 0: disabled 1: enabled
[16]	RW	crf_bm_flow_ctrl	Multicast/broadcast packet flow control enable 0: disabled 1: enabled
[15]	RW	crf_peel_dsa	DA/SA stripping control enable 0: disabled 1: enabled

[14]	RW	crf_add_da_sa	DA/SA addition control enable 0: disabled 1: enable
[13:0]	RW	crf_large_packet	Maximum length configured for packets. The default length is 1600 bytes (maximum length of packets used by the PMU).

FLOW_CTRL_PKG_THRSLD

FLOW_CTRL_PKG_THRSLD is a flow control packet number threshold register.

Offset Address	Register Name	Total Reset Value
0x00000218	FLOW_CTRL_PKG_THRSLD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crf_ip_pkg_thrsld																crf_ctrl_pkg_thrsld															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	crf_ip_pkg_thrsld	Upper threshold of the number of IP packets. When the number of IP packets that are received within period T exceeds the configured value, the flow is controlled. Otherwise, the flow is not controlled.
[15:0]	RW	crf_ctrl_pkg_thrsld	Upper threshold of the number of control packets. When the number of control packets that are received within period T exceeds the configured value, the flow is controlled. Otherwise, the flow is not controlled.

CRF_FLOW_TIME_THRSLD

CRF_FLOW_TIME_THRSLD is a flow control time register.

Offset Address	Register Name	Total Reset Value
0x0000021C	CRF_FLOW_TIME_THRSLD	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								crf_flow_time_thrsld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	crf_flow_time_thrsld	Flow control time, measured by 125 μs Flow control time T = (crf_flow_time_thrsld + 1) x 125 μs

FILTER_LISTm

FILTER_LISTm (*m* ranging from 0 to 15) is a filter list register.

Offset Address	Register Name	Total Reset Value
0x00000220 + 4 x m	FILTER_LISTm	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														crf_filt_cfg0	crf_filt_id0	crf_filt_frm_type0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	crf_filt_cfg0	Configured row or not 0: not configured 1: configured The content of this list needs to be parsed only when crf_filt_cfg is set to 1. Otherwise, the content of this list can be ignored.
[16]	RW	crf_filt_id0	Type of the list 0: MAC frame 1: IP
[15:0]	RW	crf_filt_frm_type0	Configured filter type When the ID is 0, 16 bits of crf_filt_frm_type are valid. When the ID is 1, the lower 8 bits of crf_filt_frm_type are valid, and the upper 8 bits are ignored.

CRF_UDP_NO

CRF_UDP_NO is a UDP port number register.

Offset Address	Register Name	Total Reset Value
0x00000260	CRF_UDP_NO	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crf_udp_max_no																reserved															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	crf_udp_max_no	Maximum number of the UDP ports
[15:0]	RO	reserved	Reserved

CRF_TX_FIFO_THRSLD

CRF_TX_FIFO_THRSLD is a TX FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x00000264	CRF_TX_FIFO_THRSLD	0x0271_017C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								crf_tx_p_full_th								reserved				crf_tx_p_empty_th											
Reset	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	crf_tx_p_full_th	Upper threshold of the TX FIFO When the number of valid data packets in the TX FIFO quadruples crf_tx_p_full_th, packets are not transferred from the SDRAM. After the threshold is set, the TX FIFO has sufficient space to receive a packet with the longest frame. The maximum frame length of the packet can be set in CONTROL_WORD bit[13:0] and must meet the following formula: CONTROL_WORD bit[13:0] < 8192 – 4(crf_tx_p_full_th)
[15:11]	RO	reserved	Reserved
[10:0]	RW	crf_tx_p_empty_th	Lower threshold of the TX FIFO When the number of valid data packets in the TX FIFO quadruples crf_tx_p_full_th, data can be read from the FX FIFO. It is recommended that this threshold be set to 0x14.

CRF_RX_FIFO_THRSLD

CRF_RX_FIFO_THRSLD is an RX FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x00000268	CRF_RX_FIFO_THRSLD	0x0E10_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				crf_rx_p_full_th												reserved				crf_rx_p_empty_th											
Reset	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	crf_rx_p_full_th	Upper threshold of the RX FIFO When the number of valid data packets in the RX FIFO quadruples crf_rx_p_full_th, new packets are not written to the RX FIFO. After the threshold is set, the RX FIFO has sufficient space to receive a packet with the longest frame. The maximum frame length of the packet can be set in CONTROL_WORD bit[13:0] and must meet the following formula: CONTROL_WORD[13:0] < (8192 – 4(crf_rx_p_full_th)
[15:12]	RO	reserved	Reserved
[11:0]	RW	crf_rx_p_empty_th	Lower threshold of the RX FIFO. When the number of valid data packets in the RX FIFO quadruples crf_rx_p_empty_th, data can be read from the RX FIFO. This threshold must be set to 0x200 at least.

ERR_GIVEN_PKG_CNT

ERR_GIVEN_PKG_CNT is a count register for dropped packets caused by the frame tailors marked as errors.

Offset Address	Register Name	Total Reset Value
0x00000280	ERR_GIVEN_PKG_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_given_pkg_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_given_pkg_cnt	Count of dropped packets caused by the frame tailors marked as errors

SHORT_ERR_PKT_CNT

SHORT_ERR_PKT_CNT is a short error packet count register.

Offset Address	Register Name	Total Reset Value
0x00000284	SHORT_ERR_PKT_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	short_err_pkt_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	short_err_pkt_cnt	Count of short error packets

ERR_FRM_TYPE_CNT

ERR_FRM_TYPE_CNT is a count register for dropped packets caused by the frame types not listed in the filter list.

Offset Address	Register Name	Total Reset Value
0x00000288	ERR_FRM_TYPE_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_frm_type_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_frm_type_cnt	Count of dropped packets caused by the frame types not listed in the filter list

ERR_IP_TYPE_CNT

ERR_IP_TYPE_CNT is a count register for dropped packets caused by the IP types not listed in the filter list.

Offset Address	Register Name	Total Reset Value
0x0000028C	ERR_IP_TYPE_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_ip_type_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_ip_type_cnt	Count of the dropped packets caused by the IP types not listed in the filter list

ERR_UDP_CNT

ERR_UDP_CNT is a count register for filtered packets caused by UDP port numbers beyond the specified range.

Offset Address	Register Name	Total Reset Value
0x00000290	ERR_UDP_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_udp_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	err_udp_cnt	Count of filtered packets caused by UDP port numbers beyond the specified range

OVER_FLOW_CNT

OVER_FLOW_CNT is a count register for dropped packets caused by the full RX FIFO.

Offset Address	Register Name	Total Reset Value
0x00000294	OVER_FLOW_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	over_flow_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	over_flow_cnt	Count of dropped packets caused by the full RX FIFO

OVER_LENGTH_CNT

OVER_LENGTH_CNT is a count register for dropped packets whose size exceeds the upper threshold of the PMU.

Offset Address	Register Name	Total Reset Value
0x00000298	OVER_LENGTH_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	over_length_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	over_length_cnt	Count of dropped packets whose size exceeds the upper threshold of the PMU

RX_PAUSE_EN

RX_PAUSE_EN is a flow control frame enable register in the RX direction.

Offset Address	Register Name	Total Reset Value
0x000002A4	RX_PAUSE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													rx_fifo_pause_en	rx_bq_pause_en	rx_fq_pause_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_fifo_pause_en	rx_fifo flow control frame enable 0: disabled 1: enabled
[1]	RW	rx_bq_pause_en	rx_bq flow control frame enable 0: disabled 1: enabled
[0]	RW	rx_fq_pause_en	rx_fq flow control frame enable 0: disabled 1: enabled

CRF_CFF_DATA_NUM

CRF_CFF_DATA_NUM is a configuration FIFO data count register.

Offset Address	Register Name	Total Reset Value
0x000002A8	CRF_CFF_DATA_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crf_rx_cfg_num																crf_tx_cfg_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	crf_rx_cfg_num	Count of valid descriptors remained in the rx_fq FIFO
[15:0]	RW	crf_tx_cfg_num	Count of valid descriptors remained in the tx_bq FIFO

FLOW_OUT_IP_CNT

FLOW_OUT_IP_CNT is a count register for dropped IP packets caused by flow control.

Offset Address	Register Name	Total Reset Value
0x000002AC	FLOW_OUT_IP_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flow_out_ip_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	flow_out_ip_cnt	Count of dropped IP packets caused by flow control

FLOW_OUT_CTRL_CNT

FLOW_OUT_CTRL_CNT is a count register for dropped control packets caused by flow control.

Offset Address	Register Name	Total Reset Value
0x000002B0	FLOW_OUT_CTRL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flow_out_ctrl_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RC	flow_out_ctrl_cnt	Count of dropped control packets caused by flow control

CRF_TX_PAUSE

CRF_TX_PAUSE is a TX flow control frame control register.

Offset Address	Register Name	Total Reset Value
0x00000340	CRF_TX_PAUSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															crf_tx_pause_auto
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	crf_tx_pause_auto	Flow control frame control register, specifying the way in which the MAC transmits flow control frames 0: The MAC determines whether to transmit flow control frames according to the actual traffic. When the RX FIFO of the PMU is full or to be full, the MAC transmits flow control frames automatically. 1: The MAC is forced to transmit flow control frames.

CRF_RX_LEFT_NUM

CRF_RX_LEFT_NUM is a flow control RX address count register.

Offset Address	Register Name	Total Reset Value
0x00000344	CRF_RX_LEFT_NUM	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								crf_rx_left_num							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	crf_rx_left_num	When the remaining count of addresses in the RX configuration FIFO is less than the configured value, the control packets are allowed to pass only. The data packets are filtered out.

CRF_CTRL_0_TYPE

CRF_CTRL_0_TYPE is a control packet type 0 register.

Offset Address	Register Name	Total Reset Value
0x00000348	CRF_CTRL_0_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_0_type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_0_type	Control packet type 0. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_1_TYPE

CRF_CTRL_1_TYPE is a control packet type 1 register.

Offset Address	Register Name	Total Reset Value
0x0000034C	CRF_CTRL_1_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_1_type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_1_type	Control packet type 1. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_2_TYPE

CRF_CTRL_2_TYPE is a control packet type 2 register.

Offset Address	Register Name	Total Reset Value
0x00000350	CRF_CTRL_2_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_2_type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	crf_ctrl_2_type	Control packet type 2. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_CTRL_3_TYPE

CRF_CTRL_3_TYPE is a control packet type 3 register.

Offset Address	Register Name	Total Reset Value
0x00000354	CRF_CTRL_3_TYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_ctrl_3_type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	crf_ctrl_3_type	Control packet type 3. When the frame type of an RX packet matches the configured type, the RX packet is the control packet.

CRF_BM_PKT_THRSLD

CRF_BM_PKT_THRSLD is a count threshold register for broadcast/multicast packets under flow control.

Offset Address	Register Name	Total Reset Value
0x00000358	CRF_BM_PKT_THRSLD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																crf_bm_pkt_thrsld																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	crf_bm_pkt_thrsld	Upper threshold of the number of broadcast/multicast packets under flow control. When the number of broadcast/multicast packets that are received during the flow control time exceeds the configured value, the flow is controlled; otherwise, the flow is not controlled.

CRF_BM_TIME_THRSLD

CRF_BM_TIME_THRSLD is a flow control time threshold register for broadcast and multicast packets.

Offset Address	Register Name	Total Reset Value
0x0000035C	CRF_BM_TIME_THRSLD	0x0000_2710

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												crf_bm_time_thrsld																				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	crf_bm_time_thrsld	Flow control time threshold for broadcast and multicast packets, measured by 1 μs. When the count equals the configured threshold, a time limit is reached.

MDIO_SINGLE_CMD

MDIO_SINGLE_CMD is an MDIO single operation register.

Offset Address	Register Name	Total Reset Value
0x000003C0	MDIO_SINGLE_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											mdio_cmd	reserved				op_code				reserved				phy_addr				reserved				reg_addr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20]	RW	mdio_cmd	Operation completion through the MDIO indicator 0: The operation through the MDIO is complete. 1: The operation through the MDIO starts.

[19:18]	RO	reserved	Reserved
[17:16]	RW	op_code	MDIO operation type 00: Reserved 01: Write 10: Read 11: Reserved
[15:13]	RO	reserved	Reserved
[12:8]	RW	phy_addr	5 bits of the external PHY address
[7:5]	RO	reserved	Reserved
[4:0]	RW	reg_addr	Internal address of the PHY component

MDIO_SINGLE_DATA

MDIO_SINGLE_DATA is an MDIO read/write data register.

Offset Address	Register Name	Total Reset Value
0x000003C4	MDIO_SINGLE_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdio_rd_data																mdio_wr_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	mdio_rd_data	Data that is read back from the external PHY through the MDIO
[15:0]	RW	mdio_wr_data	Data that is written through the MDIO

MDIO_CTL

MDIO_CTL is an MDIO control register.

Offset Address	Register Name	Total Reset Value
0x000003CC	MDIO_CTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												mdio_in_work	mdio_in_work_en	autoscan_en	mdc_speed
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	mdio_in_work	Single operation through the MDIO indicator 0: The single operation is not performed. 1: The single operation is performed.
[2]	RW	mdio_in_work_en	MDIO_IN_WORK bit validity indicator 0: The MDIO_IN_WORK bit is invalid. 1: The MDIO_IN_WORK bit is valid.
[1]	RW	autoscan_en	Automatic detection enable 0: disabled 1: enabled (It controls the automatic scanning enable for all the PHY addresses. The value can be set to 1 because there is only one PHY currently.)
[0]	RW	mdc_speed	Frequency of the MDIO interface clock 0: The frequency of the MDIO interface clock is 2.5 MHz. 1: The frequency of the MDIO interface clock is 18 MHz.

MDIO_RDATA_STATUS

MDIO_RDATA_STATUS is an MDIO read data status register.

Offset Address	Register Name	Total Reset Value
0x000003D0	MDIO_RDATA_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mdio_rdata_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RC	mdio_rdata_status	Whether the data read by the MDIO is valid 0: valid 1: invalid

RX_FQ_START_ADDR

RX_FQ_START_ADDR is a start address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000500	RX_FQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fq_start_addr	Start address of the idle descriptor queue. When rx_fq_start_addr_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

RX_FQ_DEPTH

RX_FQ_DEPTH is a depth register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000504	RX_FQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fq_depth																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	fq_depth	Depth of the idle descriptor queue in the RX direction. It indicates the number of words, not the number of descriptors. When rx_fq_depth_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

RX_FQ_WR_ADDR

RX_FQ_WR_ADDR is a write address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000508	RX_FQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	fq_wr_addr	Write address of the idle descriptor queue in the RX direction.

RX_FQ_RD_ADDR

RX_FQ_WR_ADDR is a read address register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000050C	RX_FQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	fq_rd_addr	Read address of the idle descriptor queue in the RX direction. When rx_fq_rd_addr_en of the RX_FQ_REG_EN register is set to 1, the register can be read and written. When rx_fq_rd_addr_en is set to 0, the register is read-only.

RX_FQ_VLDDESC_CNT

RX_FQ_VLDDESC_CNT is a valid descriptor number register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000510	RX_FQ_VLDDESC_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fq_vlddesc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	fq_vlddesc_cnt	Count of valid descriptors in the idle descriptor queue in the RX direction

RX_FQ_ALRMPTY_TH

RX_FQ_ALRMPTY_TH is an almost-empty threshold register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000514	RX_FQ_ALRMPTY_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_pause_low_th																fq_alempty_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	fq_pause_low_th	Lower flow control threshold of the rx_fq queue. If the count of valid descriptors is less than or equal to the value of fq_pause_low_th, a signal for sending flow control frames is generated.
[15:0]	RW	fq_alempty_th	Almost-empty threshold of the idle descriptor queue in the RX direction

RX_FQ_REG_EN

RX_FQ_REG_EN is an enable register related to the idle descriptor queue in the RX direction.

Offset Address	Register Name	Total Reset Value
0x00000518	RX_FQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													rx_fq_start_addr_en	rx_fq_depth_en	rx_fq_rd_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_fq_start_addr_en	Software write enable for the RX_FQ_START_ADDR register 0: The RX_FQ_START_ADDR register is protected, and software cannot be written. 1: Software of the RX_FQ_START_ADDR register can be written.

[1]	RW	rx_fq_depth_en	Software write enable for the RX_FQ_DEPTH register 0: The RX_FQ_DEPTH register is protected, and software cannot be written. 1: Software of the RX_FQ_DEPTH register can be written.
[0]	RW	rx_fq_rd_addr_en	Software write enable for the RX_FQ read address register 0: The RX_FQ read address register is protected, and software cannot be written. 1: Software of the RX_FQ read address register can be written.

RX_FQ_ALFULL_TH

RX_FQ_ALFULL_TH is an almost-full threshold register for the idle descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000051C	RX_FQ_ALFULL_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fq_pause_hi_th																fq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	fq_pause_hi_th	Upper flow control threshold for the rx_fq queue. If the count of valid descriptors is greater than or equal to the value of fq_pause_hi_th, a signal for sending flow control frames is set to 0, indicating that the flow control frames are not transmitted.
[15:0]	RW	fq_alfull_th	Almost-full threshold of the idle descriptor queue in the RX direction

RX_BQ_START_ADDR

RX_BQ_START_ADDR is a start address register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000520	RX_BQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rx_bq_start_addr	Start address of the buff descriptor queue in the RX direction. When rx_bq_start_addr_en in the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

RX_BQ_DEPTH

RX_BQ_DEPTH is a depth register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000524	RX_BQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rx_bq_depth																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	rx_bq_depth	Depth of the buff descriptor queue in the RX direction. It indicates the number of words, not the number of descriptors. When rx_bq_depth_en of the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

RX_BQ_WR_ADDR

RX_BQ_WR_ADDR is a write address register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000528	RX_BQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rx_bq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	rx_bq_wr_addr	Write address of the buff descriptor queue in the RX direction. When rx_bq_wr_addr_en of the RX_BQ_REG_EN register is set to 1, the register can be read and written. When rx_bq_wr_addr_en is set to 0, the register is read-only.

RX_BQ_RD_ADDR

RX_BQ_RD_ADDR is a read address register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000052C	RX_BQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rx_bq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	rx_bq_rd_addr	Read address of the buff descriptor queue in the RX direction

RX_BQ_FREE_DESC_CNT

RX_BQ_FREE_DESC_CNT is a writable descriptor count register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000530	RX_BQ_FREE_DESC_CNT	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rx_bq_free_desc_cnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rx_bq_free_desc_cnt	Count of writable descriptors in the buff descriptor queue in the RX direction

RX_BQ_ALEMPTY_TH

RX_BQ_ALEMPTY_TH is an almost-empty threshold register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000534	RX_BQ_ALEMPTY_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_pause_low_th																rx_bq_alempty_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rx_bq_pause_low_th	Flow control threshold of the rx_bq queue. If the count of writable descriptors is less than or equal to the value of bq_pause_low_th, an indicator for sending flow control frames is generated.
[15:0]	RW	rx_bq_alempty_th	Almost-empty threshold of the buff descriptor queue in the RX direction

RX_BQ_REG_EN

RX_BQ_REG_EN is an enable register related to the buff descriptor queue in the RX direction.

Offset Address	Register Name	Total Reset Value
0x00000538	RX_BQ_REG_EN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								rx_bq_start_addr_en	rx_bq_depth_en	rx_bq_wr_addr_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	rx_bq_start_addr_en	Software write enable for the RX_BQ_START_ADDR register 0: The RX_BQ_START_ADDR register is protected, and software cannot be written. 1: Software of the RX_BQ_START_ADDR register can be written.
[1]	RW	rx_bq_depth_en	Software write enable for the RX_BQ_DEPTH register 0: The RX_BQ_DEPTH register is protected, and software cannot be written. 1: Software of the RX_BQ_DEPTH register can be written.
[0]	RW	rx_bq_wr_addr_en	Software write enable for the RX_BQ write address register 0: The RX_BQ write address register is protected, and software cannot be written. 1: Software of the RX_BQ write address register can be written.

RX_BQ_ALFULL_TH

RX_BQ_ALFULL_TH is an almost-full threshold register for the rx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000053C	RX_BQ_ALFULL_TH	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_bq_pause_hi_th																rx_bq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rx_bq_pause_hi_th	Upper flow control threshold for the rx_bq queue. If the count of writable descriptors is greater than or equal to the value of bq_pause_hi_th, the indicator for sending flow control frames is set to 0, indicating that the flow control frames are not transmitted.
[15:0]	RW	rx_bq_alfull_th	Almost-full threshold of the buff descriptor queue in the RX direction

TX_BQ_START_ADDR

TX_BQ_START_ADDR is a start address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000580	TX_BQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_bq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_bq_start_addr	Start address of the buff descriptor queue in the TX direction. When tx_bq_start_addr_en in the TX_BQ_REG_EN register is set to 1, the register can be read and written. When tx_bq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

TX_BQ_DEPTH

TX_BQ_DEPTH is a depth register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000584	TX_BQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_bq_depth															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	tx_bq_depth	Depth of the buff descriptor queue in the TX direction. It indicates the number of words, not the number of descriptors. When tx_bq_depth_en of the TX_BQ_REG_EN register is set to 1, the register can be read and written. When tx_bq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

TX_BQ_WR_ADDR

TX_BQ_WR_ADDR is a write address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000588	TX_BQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_bq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_bq_wr_addr	Write address of the buff descriptor queue in the TX direction

TX_BQ_RD_ADDR

TX_BQ_RD_ADDR is a read address register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000058C	TX_BQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_bq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_bq_rd_addr	Read address of the buff descriptor queue in the TX direction. When rx_bq_rd_addr_en of the TX_BQ_REG_EN register is set to 1, the register can be read and written. When tx_bq_rd_addr_en is set to 0, the register is read-only.

TX_BQ_VLDDESC_CNT

TX_BQ_VLDDESC_CNT is a valid descriptor number register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000590	TX_BQ_VLDDESC_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_bq_vlddesc_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_bq_vlddesc_cnt	Count of valid descriptors in the buff descriptor queue in the TX direction

TX_BQ_ALEMPTY_TH

TX_BQ_ALEMPTY_TH is an almost-empty threshold register for the tx_buff descriptor queue.

Offset Address	Register Name	Total Reset Value
0x00000594	TX_BQ_ALEMPTY_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_bq_alempty_th																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_bq_alempty_th	Almost-empty threshold of the buff descriptor queue in the TX direction

TX_BQ_REG_EN

TX_BQ_REG_EN is an enable register related to the buff descriptor queue in the TX direction.

Offset Address	Register Name	Total Reset Value
0x00000598	TX_BQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tx_bq_start_addr_en	tx_bq_depth_en	tx_bq_rd_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_bq_start_addr_en	Software write enable for the TX_BQ_START_ADDR register 0: The TX_BQ_START_ADDR register is protected, and software cannot be written. 1: Software of the TX_BQ_START_ADDR register can be written.

[1]	RW	tx_bq_depth_en	Software write enable for the TX_BQ_DEPTH register 0: The TX_BQ_DEPTH register is protected, and software cannot be written. 1: Software of the TX_BQ_DEPTH register can be written.
[0]	RW	tx_bq_rd_addr_en	Software write enable for the TX_BQ read address register 0: The TX_BQ read address register is protected, and software cannot be written. 1: Software of the TX_BQ read address register can be written.

BQ1_ALFULL_TH

BQ1_ALFULL_TH is an almost-full threshold register for the buff1 descriptor queue.

Offset Address	Register Name	Total Reset Value
0x0000059C	BQ1_ALFULL_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bq1_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	bq1_alfull_th	Almost-full threshold of the buff1 descriptor queue in the TX direction

TX_RQ_START_ADDR

TX_RQ_START_ADDR is a start address register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A0	TX_RQ_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_rq_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_rq_start_addr	Start address of the recycle descriptor queue in the TX direction. When tx_rq_start_addr_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_start_addr_en is set to 0, the register is read-only. Only word addresses are supported.

TX_RQ_DEPTH

TX_RQ_DEPTH is a depth register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A4	TX_RQ_DEPTH	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_depth																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:0]	RW	tx_rq_depth	Depth of the recycle descriptor queue in the TX direction. It indicates the number of words, not the number of descriptors. When tx_rq_depth_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_depth_en is set to 0, the register is read-only. The depth must be set to an integral multiple of 8. It is recommended that this field be set to at least 0x400.

TX_RQ_WR_ADDR

TX_RQ_WR_ADDR is a write address register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005A8	TX_RQ_WR_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_wr_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_rq_wr_addr	Write address of the recycle descriptor queue in the TX direction. When tx_rq_wr_addr_en of the TX_RQ_REG_EN register is set to 1, the register can be read and written. When tx_rq_wr_addr_en is set to 0, the register is read-only.

TX_RQ_RD_ADDR

TX_RQ_RD_ADDR is a read address register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005AC	TX_RQ_RD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_rq_rd_addr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	tx_rq_rd_addr	Read address of the recycle descriptor queue in the TX direction.

TX_RQ_FREE_DESC_CNT

TX_RQ_FREE_DESC_CNT is a writable descriptor count register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005B0	TX_RQ_FREE_DESC_CNT	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_free_desc_cnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_rq_free_desc_cnt	Count of writable descriptors in the recycle descriptor queue in the TX direction

TX_RQ_ALEMPTY_TH

TX_RQ_ALEMPTY_TH is an almost-empty threshold register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005B4	TX_RQ_ALEMPTY_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_alempty_th																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	tx_rq_alempty_th	Almost-empty threshold of the recycle descriptor queue in the TX direction

TX_RQ_REG_EN

TX_RQ_REG_EN is an enable register related to the tx_rq descriptor queue

Offset Address	Register Name	Total Reset Value
0x000005B8	TX_RQ_REG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													tx_rq_start_addr_en	tx_rq_depth_en	tx_rq_wr_addr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	tx_rq_start_addr_en	Software write enable for the TX_RQ_START_ADDR register 0: The TX_RQ_START_ADDR register is protected, and software cannot be written. 1: Software of the TX_RQ_START_ADDR register can be written.
[1]	RW	tx_rq_depth_en	Software write enable for the TX_RQ_DEPTH register 0: The TX_RQ_DEPTH register is protected, and software cannot be written. 1: Software of the TX_RQ_DEPTH register can be written.
[0]	RW	tx_rq_wr_addr_en	Software write enable for the TX_RQ write address register 0: The TX_RQ write address register is protected, and software cannot be written. 1: Software of the TX_RQ write address register can be written.

TX_RQ_ALFULL_TH

TX_RQ_ALFULL_TH is an almost-full threshold register for the tx_rq descriptor queue.

Offset Address	Register Name	Total Reset Value
0x000005BC	TX_RQ_ALFULL_TH	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tx_rq_alfull_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	tx_rq_alfull_th	Almost-full threshold of the recycle descriptor queue in the TX direction

RAW_PMU_INT

RAW_PMU_INT is a PMU raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000005C0	RAW_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	raw_mac_fifo_err_int	raw_tx_rq_in_timeout_int	raw_rx_bq_in_timeout_int	raw_txoutcff_full_int	raw_txoutcff_empty_int	raw_txcff_full_int	raw_txcff_empty_int	raw_rxoutcff_full_int	raw_rxoutcff_empty_int	raw_rxcff_full_int	raw_rxcff_empty_int	raw_tx_rq_in_int	raw_tx_bq_out_int	raw_rx_bq_in_int	raw_rx_fq_out_int	raw_tx_rq_empty_int	raw_tx_rq_full_int	raw_tx_rq_alempty_int	raw_tx_rq_alfull_int	raw_tx_bq_empty_int	raw_tx_bq_full_int	raw_tx_bq_alempty_int	raw_tx_bq_alfull_int	raw_rx_bq_empty_int	raw_rx_bq_full_int	raw_rx_bq_alempty_int	raw_rx_bq_alfull_int	raw_rx_fq_empty_int	raw_rx_fq_full_int	raw_rx_fq_alempty_int	raw_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	raw_mac_fifo_err_int	Raw interrupt of FIFO empty and full errors in the MAC address, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[29]	RW	raw_tx_rq_in_timeout_int	Raw interrupt of descriptor enqueue timeout in the RQ queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[28]	RW	raw_rx_bq_in_timeout_int	Raw interrupt of descriptor enqueue timeout in the BQ queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[27]	RW	raw_txoutcff_full_int	Raw interrupt of full DESC_OUTCFF in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[26]	RW	raw_txoutcff_empty_int	Raw interrupt of empty DESC_OUTCFF in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[25]	RW	raw_txcff_full_int	Raw interrupt of full DESC_FIFO in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[24]	RW	raw_txcff_empty_int	Raw interrupt of empty DESC_FIFO in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[23]	RW	raw_rxoutcff_full_int	Raw interrupt of full DESC_OUTCFF in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[22]	RW	raw_rxoutcff_empty_int	Raw interrupt of empty DESC_OUTCFF in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[21]	RW	raw_rxcff_full_int	Raw interrupt of full DESC_FIFO in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[20]	RW	raw_rxcff_empty_int	Raw interrupt of empty DESC_FIFO in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[19]	RW	raw_tx_rq_in_int	Raw interrupt of descriptor (multiple or single) enqueue in the tx_rq queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[18]	RW	raw_tx_bq_out_int	Raw interrupt of descriptor (multiple or single) dequeue in the tx_bq queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[17]	RW	raw_rx_bq_in_int	Raw interrupt of descriptor (multiple or single) enqueue in the rx_bq queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	RW	raw_rx_fq_out_int	Raw interrupt of descriptor (multiple or single) dequeue in the rx_fq queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15]	RW	raw_tx_rq_empty_int	Raw interrupt of the empty recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[14]	RW	raw_tx_rq_full_int	Raw interrupt of the full recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[13]	RW	raw_tx_rq_alempty_int	Raw interrupt of the almost-empty recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[12]	RW	raw_tx_rq_alfull_int	Raw interrupt of the almost-full recycle descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	RW	raw_tx_bq_empty_int	Raw interrupt of the empty buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[10]	RW	raw_tx_bq_full_int	Raw interrupt of the full buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[9]	RW	raw_tx_bq_alempty_int	Raw interrupt of the almost-empty buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[8]	RW	raw_tx_bq_alfull_int	Raw interrupt of the almost-full buff descriptor queue in the TX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7]	RW	raw_rx_bq_empty_int	Raw interrupt of the empty buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RW	raw_rx_bq_full_int	Raw interrupt of the full buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	RW	raw_rx_bq_alempty_int	Raw interrupt of the almost-empty buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RW	raw_rx_bq_alfull_int	Raw interrupt of the almost-full buff descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	RW	raw_rx_fq_empty_int	Raw interrupt of the empty idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RW	raw_rx_fq_full_int	Raw interrupt of the full idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RW	raw_rx_fq_alempty_int	Raw interrupt of the almost-empty idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RW	raw_rx_fq_alfull_int	Raw interrupt of the almost-full idle descriptor queue in the RX direction, cleared by writing 1 to this bit 0: No raw interrupt is generated. 1: A raw interrupt is generated.

ENA_PMU_INT

ENA_PMU_INT is a PMU raw interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x000005C4	ENA_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ena_mac_fifo_err_int	ena_tx_rq_in_timeout_int	ena_rx_bq_in_timeout_int	ena_txoutcff_full_int	ena_txoutcff_empty_int	ena_txcff_full_int	ena_txcff_empty_int	ena_rxoutcff_full_int	ena_rxoutcff_empty_int	ena_rxcff_full_int	ena_rxcff_empty_int	ena_tx_rq_in_int	ena_tx_bq_out_int	ena_rx_bq_in_int	ena_rx_fq_out_int	ena_tx_rq_empty_int	ena_tx_rq_full_int	ena_tx_rq_alempty_int	ena_tx_rq_alfull_int	ena_tx_bq_empty_int	ena_tx_bq_full_int	ena_tx_bq_alempty_int	ena_tx_bq_alfull_int	ena_rx_bq_empty_int	ena_rx_bq_full_int	ena_rx_bq_alempty_int	ena_rx_bq_alfull_int	ena_rx_fq_empty_int	ena_rx_fq_full_int	ena_rx_fq_alempty_int	ena_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	ena_mac_fifo_err_int	Internal FIFO empty and full error interrupt enable in the MAC address 0: disabled 1: enabled
[29]	RW	ena_tx_rq_in_timeout_int	Descriptor enqueue timeout interrupt enable in the RQ queue in the TX direction 0: disabled 1: enabled
[28]	RW	ena_rx_bq_in_timeout_int	Descriptor enqueue timeout interrupt enable in the BQ queue in the RX direction 0: disabled 1: enabled
[27]	RW	ena_txoutcff_full_int	Full DESC_OUTCFF interrupt enable in the TX direction 0: disabled 1: enabled
[26]	RW	ena_txoutcff_empty_int	Empty DESC_OUTCFF interrupt enable in the TX direction 0: disabled 1: enabled
[25]	RW	ena_txcff_full_int	Full DESC_FIFO interrupt enable in the TX direction 0: disabled 1: enabled
[24]	RW	ena_txcff_empty_int	Empty DESC_FIFO interrupt enable in the TX direction 0: disabled 1: enabled

[23]	RW	ena_rxoutcff_full_int	Full DESC_OUTCFF interrupt enable in the RX direction 0: disabled 1: enabled
[22]	RW	ena_rxoutcff_empty_int	Empty DESC_OUTCFF interrupt enable in the RX direction 0: disabled 1: enabled
[21]	RW	ena_rxcff_full_int	Full DESC_FIFO interrupt enable in the RX direction 0: disabled 1: enabled
[20]	RW	ena_rxcff_empty_int	Empty DESC_FIFO interrupt enable in the RX direction 0: disabled 1: enabled
[19]	RW	ena_tx_rq_in_int	Descriptor (multiple or single) enqueue interrupt enable in the tx_rq queue in the TX direction 0: disabled 1: enabled
[18]	RW	ena_tx_bq_out_int	Descriptor (multiple or single) dequeue interrupt enable in the tx_bq queue in the TX direction 0: disabled 1: enabled
[17]	RW	ena_rx_bq_in_int	Descriptor (multiple or single) enqueue interrupt enable in the rx_bq queue in the RX direction 0: disabled 1: enabled
[16]	RW	ena_rx_fq_out_int	Descriptor (multiple or single) dequeue interrupt enable in the rx_fq queue in the RX direction 0: disabled 1: enabled
[15]	RW	ena_tx_rq_empty_int	Empty recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[14]	RW	ena_tx_rq_full_int	Full recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[13]	RW	ena_tx_rq_alempty_int	Almost-empty recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled

[12]	RW	ena_tx_rq_alfull_int	Almost-full recycle descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[11]	RW	ena_tx_bq_empty_int	Empty buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[10]	RW	ena_tx_bq_full_int	Full buff descriptor queue interrupt enable in the TX direction 1: enabled 0: disabled
[9]	RW	ena_tx_bq_alempty_int	Almost-empty buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[8]	RW	ena_tx_bq_alfull_int	Almost-full buff descriptor queue interrupt enable in the TX direction 0: disabled 1: enabled
[7]	RW	ena_rx_bq_empty_int	Empty buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[6]	RW	ena_rx_bq_full_int	Full buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[5]	RW	ena_rx_bq_alempty_int	Almost-empty buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[4]	RW	ena_rx_bq_alfull_int	Almost-full buff descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[3]	RW	ena_rx_fq_empty_int	Empty idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[2]	RW	ena_rx_fq_full_int	Full idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled

[1]	RW	ena_rx_fq_alempty_int	Almost-empty idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled
[0]	RW	ena_rx_fq_alfull_int	Almost-full idle descriptor queue interrupt enable in the RX direction 0: disabled 1: enabled

STATUS_PMU_INT

STATUS_PMU_INT is a PMU interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000005C8	STATUS_PMU_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	status_mac_fifo_err_int	status_tx_rq_in_timeout_int	status_rx_bq_in_timeout_int	status_txoutcff_full_int	status_txoutcff_empty_int	status_txcff_full_int	status_txcff_empty_int	status_rxoutcff_full_int	status_rxoutcff_empty_int	status_rxcff_full_int	status_rxcff_empty_int	status_tx_rq_in_int	status_tx_bq_out_int	status_rx_bq_in_int	status_rx_fq_out_int	status_tx_rq_empty_int	status_tx_rq_full_int	status_tx_rq_alempty_int	status_tx_rq_alfull_int	status_tx_bq_empty_int	status_tx_bq_full_int	status_tx_bq_alempty_int	status_tx_bq_alfull_int	status_rx_bq_empty_int	status_rx_bq_full_int	status_rx_bq_alempty_int	status_rx_bq_alfull_int	status_rx_fq_empty_int	status_rx_fq_full_int	status_rx_fq_alempty_int	status_rx_fq_alfull_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	status_mac_fifo_err_int	Status of the MAC internal FIFO empty and full error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[29]	RW	status_tx_rq_in_timeout_int	Status of the TX RQ queue descriptor enqueue timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[28]	RW	status_rx_bq_in_timeout_int	Status of the RX BQ queue descriptor enqueue timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[27]	RW	status_txoutcff_full_int	Status of the TX DESC_OUTCFF full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[26]	RW	status_txoutcff_empty_int	Status of the TX DESC_OUTCFF empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RW	status_txcff_full_int	Status of the TX DESC_FIFO full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RW	status_txcff_empty_int	Status of the TX DESC_FIFO empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[23]	RW	status_rxoutcff_full_int	Status of the RX DESC_OUTCFF full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[22]	RW	status_rxoutcff_empty_int	Status of the RX DESC_OUTCFF empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[21]	RW	status_rxcff_full_int	Status of the RX DESC_FIFO full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[20]	RW	status_rxcff_empty_int	Status of the RX DESC_FIFO empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[19]	RW	status_tx_rq_in_int	Status of the tx_rq queue descriptor (multiple or single) enqueue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RW	status_tx_bq_out_int	Status of the tx_bq queue descriptor (multiple or single) dequeue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RW	status_rx_bq_in_int	Status of the rx_bq queue descriptor (multiple or single) enqueue interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RW	status_rx_fq_out_int	Status of the rx_fq queue descriptor (multiple or single) dequeue interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[15]	RW	status_tx_rq_empty_int	Status of the TX recycle descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RW	status_tx_rq_full_int	Status of the TX recycle descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RW	status_tx_rq_alempty_int	Status of the TX recycle descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[12]	RW	status_tx_rq_alfull_int	Status of the TX recycle descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RW	status_tx_bq_empty_int	Status of the TX buff descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RW	status_tx_bq_full_int	Status of the TX buff descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RW	status_tx_bq_alempty_int	Status of the TX buff descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RW	status_tx_bq_alfull_int	Status of the TX buff descriptor queue almost-full interrupt 1: An interrupt is generated. 0: No interrupt is generated.
[7]	RW	status_rx_bq_empty_int	Status of the RX buff descriptor queue empty interrupt 1: An interrupt is generated. 0: No interrupt is generated.
[6]	RW	status_rx_bq_full_int	Status of the RX buff descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RW	status_rx_bq_alempty_int	Status of the RX buff descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RW	status_rx_bq_alfull_int	Status of the RX buff descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[3]	RW	status_rx_fq_empty_int	Status of the RX idle descriptor queue empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RW	status_rx_fq_full_int	Status of the RX idle descriptor queue full interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RW	status_rx_fq_almpty_int	Status of the RX idle descriptor queue almost-empty interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RW	status_rx_fq_alfull_int	Status of the RX idle descriptor queue almost-full interrupt 0: No interrupt is generated. 1: An interrupt is generated.

DESC_WR_RD_ENA

DESC_WR_RD_ENA is a cff read/write descriptor enable register.

Offset Address	Register Name	Total Reset Value
0x000005CC	DESC_WR_RD_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_outcff_wr_desc_ena	rx_cff_rd_desc_ena	tx_outcff_wr_desc_ena	tx_cff_rd_desc_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	rx_outcff_wr_desc_ena	RX_OUTCFF write descriptor to RX_BQ enable in the RX direction 0: disabled 1: enabled
[2]	RW	rx_cff_rd_desc_ena	RX_CFF read descriptor from the idle descriptor queue enable in the RX direction 0: disabled 1: enabled

[1]	RW	tx_outcff_wr_desc_ena	TX_OUTCFF write descriptor to TX_RQ enable in the TX direction 0: disabled 1: enabled
[0]	RW	tx_cff_rd_desc_ena	TX_CFF read descriptor from TX_BQ enable in the TX direction 0: disabled 1: enabled

IN_QUEUE_TH

IN_QUEUE_TH is an rx_bq or tx_rq enqueue interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05D8	IN_QUEUE_TH	0x0001_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_rq_in_th								reserved								rx_bq_in_th							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	tx_rq_in_th	Threshold for reporting descriptor enqueue interrupts in the TX direction. The threshold must be greater than or equal to 1.
[15:8]	RO	reserved	Reserved
[7:0]	RW	rx_bq_in_th	Threshold for reporting descriptor enqueue interrupts in the RX direction. The threshold must be greater than or equal to 1.

OUT_QUEUE_TH

OUT_QUEUE_TH is an rx_fq or tx_bq dequeue interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05DC	OUT_QUEUE_TH	0x0001_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_bq_out_th								reserved								rx_fq_out_th							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:16]	RW	tx_bq_out_th	Threshold for reporting descriptor dequeue interrupts in the TX direction
[15:8]	RO	reserved	Reserved
[7:0]	RW	rx_fq_out_th	Threshold for reporting descriptor dequeue interrupts in the RX direction

RX_BQ_IN_TIMEOUT_TH

RX_BQ_IN_TIMEOUT_TH is an rx_bq enqueue timeout raw interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05E0	RX_BQ_IN_TIMEOUT_TH	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_bq_in_timeout_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_bq_in_timeout_th	Threshold for reporting descriptor enqueue timeout interrupts in the BQ queue in the RX direction

TX_RQ_IN_TIMEOUT_TH

TX_RQ_IN_TIMEOUT_TH is a tx_rq enqueue timeout raw interrupt threshold register.

Offset Address	Register Name	Total Reset Value
0x05E4	TX_RQ_IN_TIMEOUT_TH	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_rq_in_timeout_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_rq_in_timeout_th	Threshold for reporting descriptor enqueue timeout interrupts in the RQ queue in the TX direction

STOP_CMD

STOP_CMD is an RX and TX packet control stop register.

Offset Address	Register Name	Total Reset Value
0x05E8	STOP_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														tx_stop_en	rx_stop_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	tx_stop_en	Packet TX stop enable 0: disabled 1: enabled
[0]	RW	rx_stop_en	Packet RX stop enable 0: disabled 1: enabled

FLUSH_CMD

FLUSH_CMD is a recycle descriptor enable register.

Offset Address	Register Name	Total Reset Value
0x05EC	FLUSH_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tx_flush_cmd	rx_flush_cmd	tx_flush_flag_down	tx_flush_flag_up	rx_flush_flag_down	rx_flush_flag_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	tx_flush_cmd	Recycle descriptor command in the TX direction, instructing the descriptors to enter the tx_rq queue 0: The recycle descriptor configuration command is invalid. 1: The recycle descriptor configuration command is valid.
[4]	RW	rx_flush_cmd	Recycle descriptor command in the RX direction, instructing the descriptors to enter the rx_bq queue 0: The recycle descriptor configuration command is invalid. 1: The recycle descriptor configuration command is valid.
[3]	RW	tx_flush_flag_down	Recycle descriptor stop indicator in the TX direction. After descriptors are recycled, the logic sets tx_flush_flag to 1, and the software writes 1 to clear the register.
[2]	RW	tx_flush_flag_up	Recycle descriptor stop indicator in the TX direction. After RX and TX packets are stopped, the logic sets tx_flush_flag to 1, indicating that the software can recycle the descriptors. The software writes 1 to clear the register.
[1]	RW	rx_flush_flag_down	Recycle descriptor stop indicator in the RX direction. After descriptors are recycled, the logic sets rx_flush_flag_down to 1, and the software writes 1 to clear the register.
[0]	RW	rx_flush_flag_up	Recycle descriptor indicator in the RX direction. After RX packets are stopped, the logic sets rx_flush_flag_up to 1, indicating that the software can recycle the descriptors. The software writes 1 to clear the register.

U_EEE_INTR_SRC

U_EEE_INTR_SRC is an LPI status register in the RX and TX directions.

Offset Address	Register Name	Total Reset Value
0x0800	U_EEE_INTR_SRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											tx_lpi_cond	rx_leave_lpi	rx_entry_lpi	tx_leave_lpi	tx_entry_lpi
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	tx_lpi_cond	LPI status in the TX direction 0: The TX FIFO and TX descriptors cannot be empty simultaneously. 1: The TX FIFO and TX descriptors are empty simultaneously.
[3]	RW	rx_leave_lpi	LPI exit in the RX direction 0: not exited 1: exited
[2]	RW	rx_entry_lpi	LPI enter in the RX direction 0: not entered 1: entered
[1]	RW	tx_leave_lpi	LPI exit in the TX direction 0: not exited 1: exited
[0]	RW	tx_entry_lpi	LPI enter in the TX direction 0: not entered 1: entered

U_EEE_INTR_EN

U_EEE_INTR_EN is an interrupt mask and enable register in the RX and TX directions.

Offset Address	Register Name	Total Reset Value
0x0804	U_EEE_INTR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tx_lpi_cond_msk	rx_leave_lpi_msk	rx_entry_lpi_msk	tx_leave_lpi_msk	tx_entry_lpi_msk	tx_lpi_cond_en	rx_leave_lpi_en	rx_entry_lpi_en	tx_leave_lpi_en	tx_entry_lpi_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	tx_lpi_cond_msk	LPI status interrupt mask in the TX direction 0: not masked 1: masked
[8]	RW	rx_leave_lpi_msk	LPI status exit interrupt mask in the RX direction 0: not masked 1: masked
[7]	RW	rx_entry_lpi_msk	LPI status enter interrupt mask in the RX direction 0: not masked 1: masked
[6]	RW	tx_leave_lpi_msk	LPI status exit interrupt mask in the TX direction 0: not masked 1: masked
[5]	RW	tx_entry_lpi_msk	LPI status enter interrupt mask in the TX direction 0: not masked 1: masked
[4]	RW	tx_lpi_cond_en	LPI status interrupt enable in the TX direction 0: Disable interrupts. 1: Enable interrupts.
[3]	RW	rx_leave_lpi_en	LPI status interrupt enable exit in the RX direction 0: Disable interrupts. 1: Enable interrupts.
[2]	RW	rx_entry_lpi_en	LPI status interrupt enable enter in the RX direction 0: Disable interrupts. 1: Enable interrupts.

[1]	RW	tx_leave_lpi_en	LPI status interrupt enable exit in the TX direction 0: Disable interrupts. 1: Enable interrupts.
[0]	RW	tx_entry_lpi_en	LPI status interrupt enable enter in the TX direction 0: Disable interrupts. 1: Enable interrupts.

U_EEE_ENABLE

U_EEE_ENABLE is an EEE enable signal register.

Offset Address	Register Name	Total Reset Value
0x0808	U_EEE_ENABLE	0x00F4_2400

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	eee_ls_timer							gmii_mode	cond_intr_keep	tx_lpi_assert	eee_enable
Reset	0 0 0 0	0 0 0 0	1 1 1 1	0 1 0 0	0 0 1 0	0 1 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	eee_ls_timer	Buffer time for the buffer software to enable the hardware to enter the LPI when phy_link_sts is set to 1. The default time is 1s.
[3]	RW	gmii_mode	GMII mode select 0: MII mode 1: GMII mode
[2]	RW	cond_intr_keep	Interrupt signal TX frequency 0: The hardware sends only one tx_lpi_cond interrupt. 1: The interrupt is enabled on the rising edge of each clock in LPI mode in the TX direction.
[1]	RW	tx_lpi_assert	Software configuring the hardware to enter the LPI state 0: The hardware does not enter the LPI state. 1: The hardware enters the LPI state.
[0]	RW	eee_enable	EEE module enable 0: disabled 1: enabled

U_EEE_TIMER

U_EEE_TIMER is an LPI time threshold register.

Offset Address	Register Name	Total Reset Value
0x080C	U_EEE_TIMER	0x001E_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lpi_tw_timer																lpi_cond_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	lpi_tw_timer	Wake-up time of the register from the LPI mode to normal mode. The default time is 30 μs.
[15:0]	RW	lpi_cond_timer	Duration when the TX FIFO and EX_DESC are empty at the same time. When the duration is equal to the value of lpi_cond_timer, the register enters the LPI mode.

U_EEE_LINK_STATUS

U_EEE_LINK_STATUS is an EEE status register.

Offset Address	Register Name	Total Reset Value
0x0810	U_EEE_LINK_STATUS	0x0000_3F20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intr_cnt																eee_tx_lpi_stay	eee_rx_lpi_stay_ff3	version										reserved	eee_auto	eee_hold_txdesc_read	phy_link_sts
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	intr_cnt	EEE interrupt count
[15]	RO	eee_tx_lpi_stay	Whether the TX register is in LPI state 0: The TX register is not in LPI state. 1: The TX register is in LPI state.
[14]	RO	eee_rx_lpi_stay_ff3	Whether the RX register is in LPI state 0: The TX register is not in LPI state. 1: The TX register is in LPI state.

[13:4]	RO	version	Logical version number
[3]	RO	reserved	Reserved
[2]	RW	eee_auto	Automatic EEE entry and exit 0: The logic enters or exits the EEE mode by using the software and logic interrupt. 1: The logic automatically enters or exits the EEE without the intervention of software.
[1]	RW	eee_hold_txdesc_read	Whether the MAC can obtain packets from the TX FIFO in LPI status 0: yes 1: no
[0]	RW	phy_link_sts	PHY connection state 0: link_down 1: link_up

U_EEE_TIME_CLK_CNT

U_EEE_TIME_CLK_CNT is a timing pulse count register.

Offset Address	Register Name	Total Reset Value
0x0814	U_EEE_TIME_CLK_CNT	0x0000_007D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_period_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:0]	RW	clk_period_cnt	Count register used to generate a 1 μs timing pulse in the hardware. The clock cycle is 8 ns when the clock frequency is 125 MHz.

PMT_CTRL_STAUTS

PMT_CTRL_STAUTS is a PMT control and status register.

Offset Address	Register Name	Total Reset Value
0x0A00	PMT_CTRL_STAUTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						scr_wkupfrm_glbucast	reserved		rcvd_wkup_frm	rcvd_mgk_pkt	reserved	scr_intr_en	scr_wkupfrm_en	scr_mgkpkt_en	scr_power_down
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	scr_wkupfrm_glbucast	Whether the unicast frame used to configure the MAC address is the wake-up frame 0: The unicast frame is not regarded as the wake-up frame. 1: The unicast frame used to configure the MAC address is regarded as the valid wake-up frame.
[8:7]	RO	reserved	Reserved
[6]	RW	rcvd_wkup_frm	Whether a wake_up frame is received 0: no 1: yes
[5]	RW	rcvd_mgk_pkt	Whether the magic packet is received. 0: no 1: yes
[4]	RO	reserved	Reserved
[3]	RW	scr_intr_en	PMT interrupt enable 0: disabled 1: enabled
[2]	RW	scr_wkupfrm_en	wake_up frame receive enable 0: disabled 1: enabled
[1]	RW	scr_mgkpkt_en	Magic packet receive enable 0: disabled 1: enabled
[0]	RW	scr_power_down	Power-down mode enable 0: Exit the power-down mode. 1: Enter the power-down mode.

FILTER_0_BYTE_MASK

FILTER_0_BYTE_MASK is PMT valid byte selection register 0.

Offset Address	Register Name	Total Reset Value
0x0A04	FILTER_0_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter0bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter0bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask. If a bit is 1, the corresponding byte is valid.

FILTER_1_BYTE_MASK

FILTER_1_BYTE_MASK is PMT valid byte selection register 1.

Offset Address	Register Name	Total Reset Value
0x0A08	FILTER_1_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter1bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter1bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

FILTER_2_BYTE_MASK

FILTER_2_BYTE_MASK is PMT valid byte selection register 2.

Offset Address	Register Name	Total Reset Value
0x0A0C	FILTER_2_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter2bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter2bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

FILTER_3_BYTE_MASK

FILTER_3_BYTE_MASK is PMT valid byte selection register 3.

Offset Address	Register Name	Total Reset Value
0x0A10	FILTER_3_BYTE_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter3bytemsk																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wkupfrm_filter3bytemsk	Bit[31] must be set to low, indicating that the mask is valid. Bit[30:0] are used for byte mask.

FILTER_COMMAND

FILTER_COMMAND is a PMT template selection and multicast enable register.

Offset Address	Register Name	Total Reset Value
0x0A14	FILTER_COMMAND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				wkupfrm_filter3mcast	reserved		wkupfrm_filter3en	reserved				wkupfrm_filter2mcast	reserved		wkupfrm_filter2en	reserved				wkupfrm_filter1mcast	reserved		wkupfrm_filter1en	reserved				wkupfrm_filter0mcast	reserved		wkupfrm_filter0en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	wkupfrm_filter3mcast	Address type specified by template 3 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[26:25]	RO	reserved	Reserved.
[24]	RW	wkupfrm_filter3en	Filter template 3 enable 0: disabled 1: enabled
[23:20]	RO	reserved	Reserved
[19]	RW	wkupfrm_filter2mcast	Address type specified by template 2 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[18:17]	RO	reserved	Reserved
[16]	RW	wkupfrm_filter2en	Filter template 2 enable 0: disabled 1: enabled
[15:12]	RO	reserved	Reserved

[11]	RW	wkupfrm_filter1mcast	Address type specified by template 1 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[10:9]	RO	reserved	Reserved.
[8]	RW	wkupfrm_filter1en	Filter template 1 enable 0: disabled 1: enabled
[7:4]	RO	reserved	Reserved
[3]	RW	wkupfrm_filter0mcast	Address type specified by template 0 0: The match of address type is determined based on the valid bytes of the corresponding template and CRC offset address. 1: The address is successfully filtered when the destination address is a valid multicast address.
[2:1]	RO	reserved	Reserved.
[0]	RW	wkupfrm_filter0en	Filter template 0 enable 0: disabled 1: enabled

FILTER_OFFSET

FILTER_OFFSET is a CRC position offset register.

Offset Address	Register Name	Total Reset Value
0x0A18	FILTER_OFFSET	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wkupfrm_filter3offset		wkupfrm_filter2offset		wkupfrm_filter1offset		wkupfrm_filter0offset	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wkupfrm_filter3offset	Template 3 of the four templates, used to calculate the CRC position offset
[23:16]	RW	wkupfrm_filter2offset	Template 2 of the four templates, used to calculate the CRC position offset
[15:8]	RW	wkupfrm_filter1offset	Template 1 of the four templates, used to calculate the CRC position offset
[7:0]	RW	wkupfrm_filter0offset	Template 0 of the four templates, used to calculate the CRC position offset

FILTER0_1_CRC

FILTER0_1_CRC is a software-expected CRC value 0 and 1 register.

Offset Address	Register Name	Total Reset Value
0x0A1C	FILTER0_1_CRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter1crc																wkupfrm_filter0crc															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wkupfrm_filter1crc	CRC value expected by software of template 1 in the four templates
[15:0]	RW	wkupfrm_filter0crc	CRC value expected by software of template 1

FILTER2_3_CRC

FILTER2_3_CRC is a software-expected CRC value 2 and 3 register.

Offset Address	Register Name	Total Reset Value
0x0A20	FILTER2_3_CRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupfrm_filter3crc																wkupfrm_filter2crc															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wkupfrm_filter3crc	CRC value expected by software of template 3
[15:0]	RW	wkupfrm_filter2crc	CRC value expected by software of template 2

Contents

Figures

6 Video Codec

6.1 VEDU

6.1.1 Overview

The video encoding/decoding unit (VEDU) is a codec that supports H.264 protocol and performs encoding by using hardware. It features low CPU usage, low bus bandwidth, low delay, and low power consumption.

6.1.2 Features

The VEDU has the following features:

- ITU-T H.264 High Profile/main profile/baseline profile@ level 4.2 encoding
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four sub-block types of 16x16, 16x8, 8x16, and 8x8 for inter-prediction
  - Prediction modes of intra4x4, intra8x8, and intra16x16
  - Trans4x4 and trans8x8
  - Context-based adaptive binary arithmetic coding (CABAC) and context-based adaptive variable-length coding (CAVLC) entropy encoding
  - De-blocking filtering
  - IPCM encoding
- Input picture format of Semi-planar YCbCr4:2:0
- H.264&JPEG encoding and decoding of multiple streams (For Hi3521A)
  - 4x1080p@30 fps H.264 encoding+4x CIF@30 fps H.264 encoding+1x1080p@30 fps H.264 decoding+4x1080p@2fps JPEG encoding
  - 8x720p@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4x720p@30 fps H.264 decoding+8x720p@2fps JPEG encoding
  - 16x960H@30 fps H.264 encoding+16xCIF@30 fps H.264 encoding+4x960H@30 fps H.264 decoding+16x960H@2 fps JPEG encoding
  - 16xD1@30 fps H.264 encoding+16xCIF@30 fps H.264 encoding+8xD1@30 fps H.264 decoding+16xD1@2 fps JPEG encoding
  - 5x1080p@30 fps H.264 decoding
  - 10x720p@30 fps H.264decoding
  - 4x720p@30 fps JPEG decoding

- H.264&JPEG encoding and decoding of multiple streams (For Hi3520D V300)
  - 4x720p@30 fps H.264 encoding+4xCIF@30 fps H.264 encoding+4x720p@30 fps H.264 decoding+4x720p@2fps JPGE encoding
  - 8x960H@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+1x960H@30 fps H.264 decoding + 8x960H@2fps JPEG encoding
  - 8xD1@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4xD1@30 fps H.264 decoding +8x960H@2fps JPEG encoding
  - 2x1080p@30 fps H.264 decoding
  - 4x720p@30 fps H.264 decoding
  - 4x720p@30 fps JPEG decoding
- Configurable picture resolutions
  - Minimum picture resolution: 160 x 64
  - Maximum picture resolution: 2048 x 2048
  - Step of the picture width or height: 4
- Region of interest (ROI) encoding
  - A maximum of eight ROIs
  - ROI encoding control
- On-screen display (OSD) encoding protection control
- OSD front-end overlaying
  - OSD overlaying before encoding for a maximum of eight regions. The format of the OSD picture can be ARGB1555 (16 bits) or ARBG4444.
  - OSD overlaying at the maximum picture size and at the 2-pixel-aligned position
  - 129-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Constant bit rate (CBR) mode and variable bit rate (VBR) mode
- Fixed QP encoding
- Output bit rate ranging from 2 kbit/s to 40 Mbit/s
- SVC_T

The VEDU has the following decoding features

- Supports ITU-T H.264 high profile/main profile/baseline profile@ level 4.2 encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four sub-block types of 16x16, 16x8, 8x16, and 8x8 for inter-prediction
  - Prediction modes of intra4x4, intra8x8, and intra16x16
  - Trans4x4 and trans8x8
  - CABAC and CAVLC entropy decoding
  - De-blocking filtering
  - IPCM decoding
  - ASO and FMO not supported
  - B slice decoding not supported
  - Decoding by field not supported
  - MBAFF not supported
  - Weighted prediction not supported

- Reports the luminance statistics on a complete frame.
- Supports the following picture resolutions:
  - Minimum picture resolution: 80 x 64
  - Maximum picture resolution: 4096 x 4096

6.1.3 Function Description

Figure 6-1 shows the encoding functional block diagram of the VEDU.

Based on related protocols and algorithms, the VEDU supports motion estimation, inter-prediction, intra-prediction, motion vector prediction, transform/quantization, inverse transform/inverse quantization, variable length code (VLC) encoding, stream generation, and de-blocking filtering. The video firmware (FMW) controls the bit rate and handles interrupts.

Before the VEDU starts video encoding, the software allocates three types of buffers for the VENC in the external DDR SDRAM:

- Input picture buffer

  The VEDU reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the VICAP module.
- Reconstruction/Reference picture buffer

  The VEDU writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of the subsequent pictures. During the encoding of P frames, reference pictures are read from this buffer.
- Stream buffer

  This buffer stores encoded streams. The VEDU writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-1 Encoding functional block diagram of the VEDU

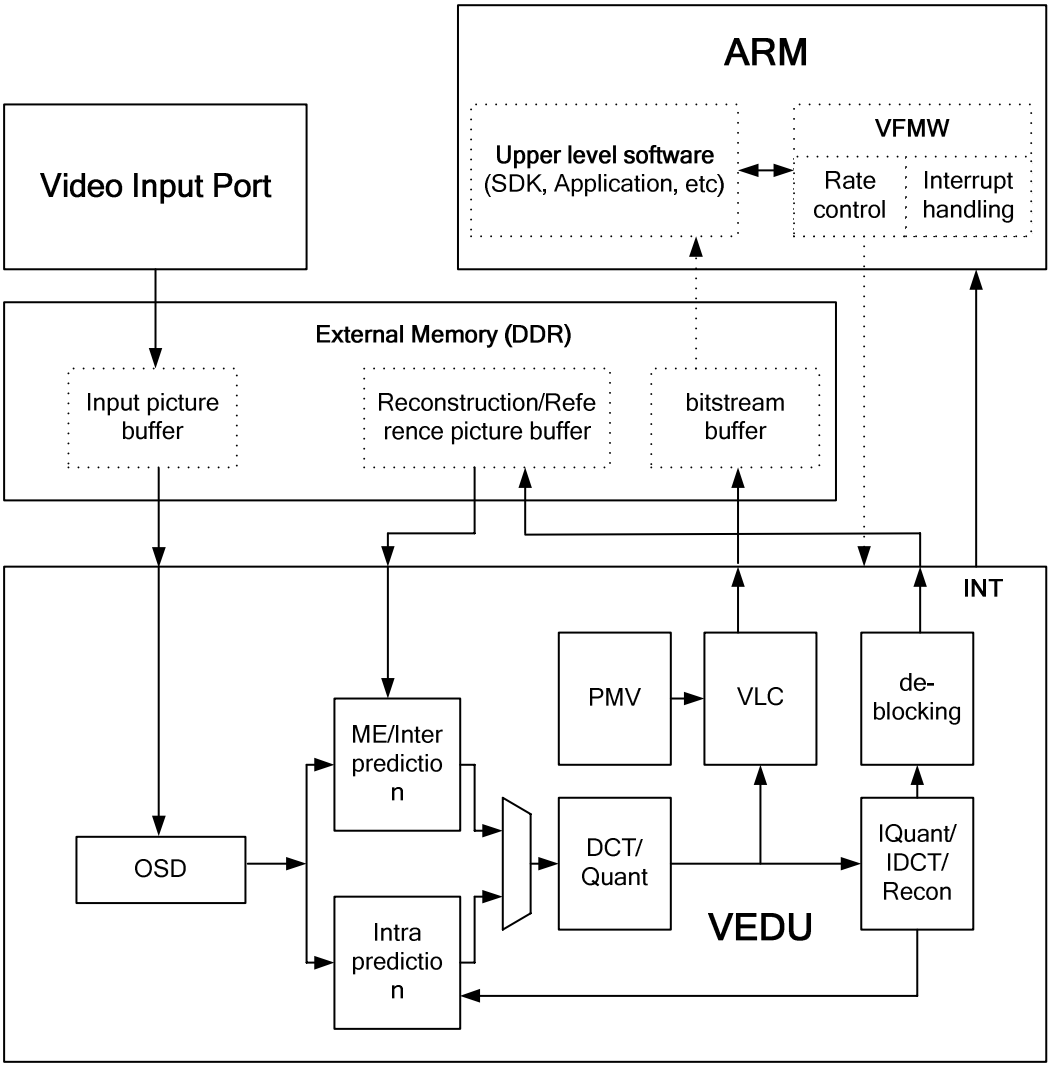


Figure 6-2 shows the decoding functional block diagram of the VEDU.

The VEDU decodes H.264 streams by slice. The VFMW decodes the slice header and the streams before the slice header, and the VEDU hardware decodes the slice data and the streams after the slice data.

Before the VEDU starts encoding, the software allocates three types of buffers for the VEDU in the external DDR SDRAM:

- Reconstruction/Reference buffer

  The VEDU writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of the subsequent pictures to be decoded. When P frames are being decoded, reference pictures are read from this buffer.

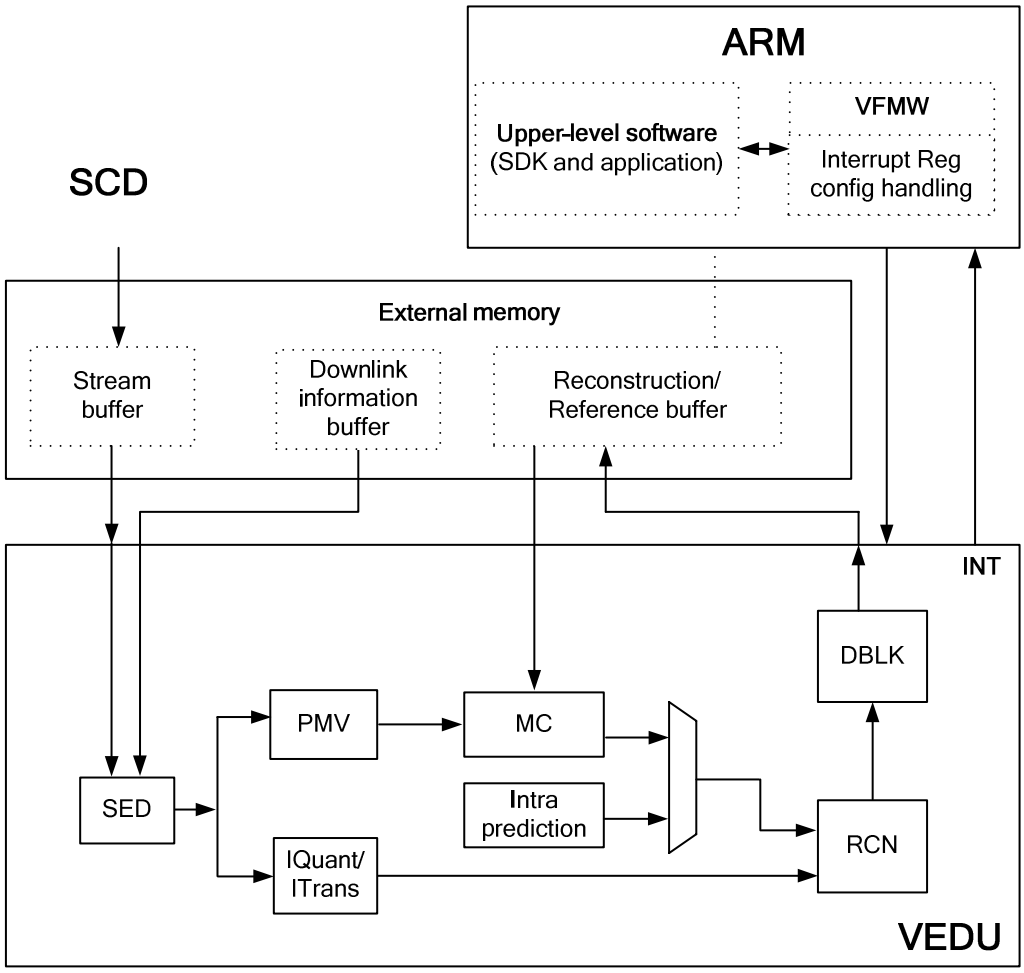
- Stream buffer

  This buffer stores the streams to be decoded. These streams are from the start code detect (SCD) module.

- Downlink information buffer

This buffer stores the input streams to be decoded and the streams before the slice data.

Figure 6-2 Decoding functional block diagram of the VEDU



6.2 JPGE/JPGD

6.2.1 Overview

The JPGE provides high-performance encoding performance by using hardware. It supports 8K x 8K snapshot or HD MJPEG encoding.

The JPEG decoder (JPGD) decodes static JPEG and Motion-JPEG pictures.

6.2.2 Features

The JPGE has the following features:

- ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
- Microprogrammed control unit (MCU) using the interleaved sequence
- Multiple input picture formats

  - Planar YCbCr4:2:0
  - Planar YCbCr4:2:2
  - Planar YCbCr4:4:4
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
  - Package YUYV
- At most 33.1 megapixels/s (1080p@16 fps)
- Configurable picture resolutions
  - Minimum picture resolution: 32 x 32
  - Maximum picture resolution: 8192 x 8192
- Picture width or height step of 4
- Configurable quantization tables

  An independent quantization table for the Y component, Cb component, and Cr component respectively
- OSD front-end overlaying
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlapping with the maximum size of the source picture and within the picture position range
  - 129-level alpha blending
  - OSD overlaying control

The JPGD has the following features:

- Supports the advanced eXtensible interface (AXI).
- Supports interrupts.
- Supports ITU-T81 baseline profile decoding.
  - JPEG picture decoding of YUV components in five formats including YUV 4:0:0, YUV4:2:0, YUV4:2:2 1x2, YUV4:2:2 2x1, and YUV 4:4:4.
  - A maximum of four Huffman tables including two direct coefficient (DC) tables and two alternating coefficient (AC) tables.
  - A maximum of three quantization tables.
  - Sequential decoding.
  - Discrete cosine transform-based (DCT-based) JPEG decoding.
  - 8-bit depth.
  - Interleaved scanning.
- Supports 1/2, 1/4, or 1/8 frequency domain scaling.
- Decodes the static pictures with the maximum resolution 8096x8096 and with the minimum resolution 1x1.
- Supports the semi-planar output storage format with the maximum resolution 8096x8096.
- Supports segment decoding of compressed streams.
- Provides 4x720p@30fps JPGE decoding, satisfying the strict real-time requirements of various decoding systems.
- Supports frequency domain scaling to reduce the usage of the memory and bandwidth during decoding.

6.2.3 Function Description

Figure 6-3 shows the functional block diagram of the JPGE.

Based on the protocols that require a large number of operands, the JPGE supports OSD, level shift, discrete cosine transform (DCT), quantization, scanning, VLC encoding, and stream generation. The VFMW configures quantization tables and handles interrupts.

Before the JPGE is enabled for video encoding, the software allocates two types of buffers for the JPGE in the external DDR SDRAM:

- Input picture buffer

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the VICAP module.

- Stream buffer

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-3 Functional block diagram of the JPGE

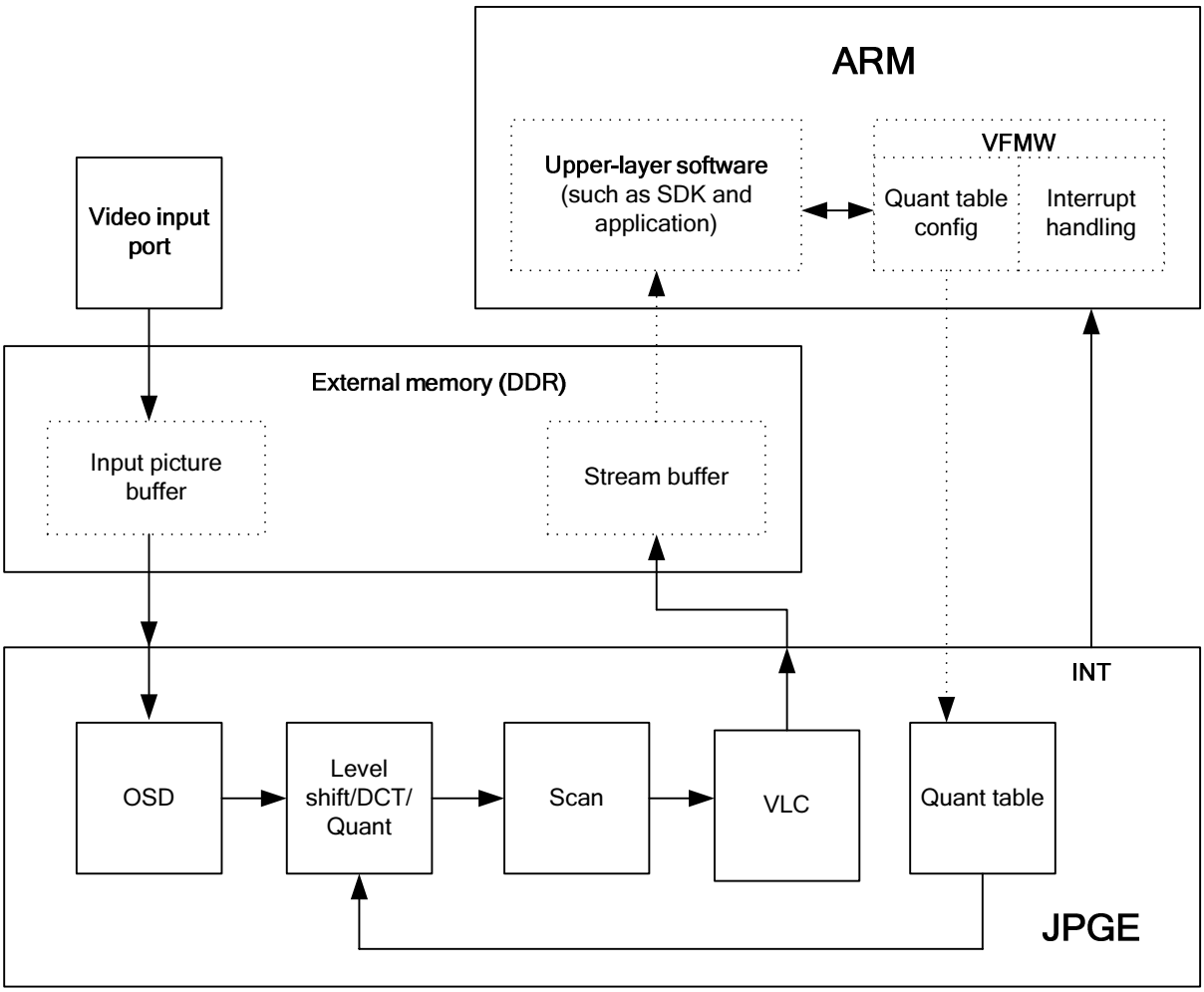


Figure 6-4 shows the JPGD architecture.

Figure 6-4 JPGD architecture

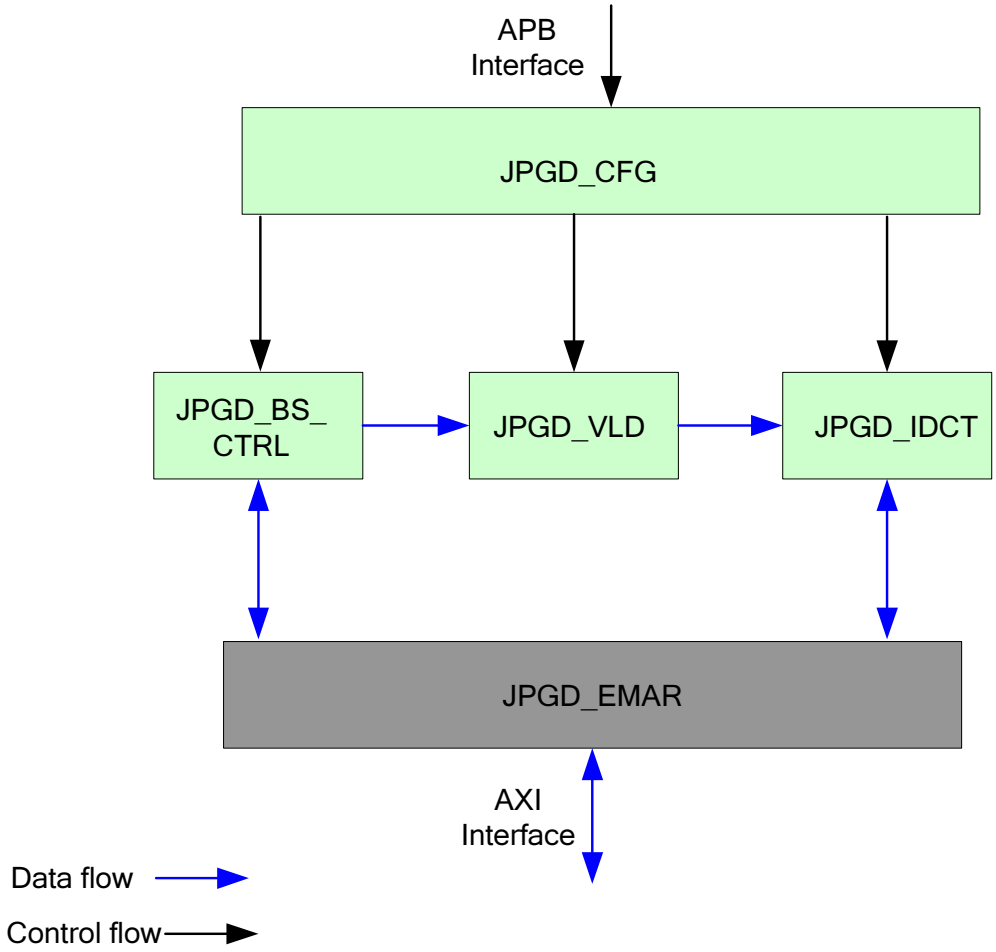


Table 6-1 describes the internal modules of the JPGD.

Table 6-1 Internal modules of the JPGD

Module	Description
JPGD_BS_CTRL	This module reads and shifts streams. It contains a shift barrel that sends valid streams to downstream modules for decoding.
JPGD_VLD	This module decodes Huffman variable-length codes and performs inverse scanning and dequantization on coefficients after decoding.
JPGD_IDCT	This module performs inverse discrete cosine transform (IDCT) and scales the frequency domain.
JPGD_EMAR	This module is related to the AXI bus and implements bus async processing and data storage.

Module	Description
JPGD_CFG	This module receives the configuration information about the host, and configures each functional module based on the configuration information. In addition, this module starts the decoder, generates interrupts, and reports the internal status information about the decoder to the host.

6.2.4 JPGD Operating Mode

6.2.4.1 Classification of Software and Hardware

Figure 6-5 shows the structure of JPEG streams.

Figure 6-5 Structure of JPEG streams

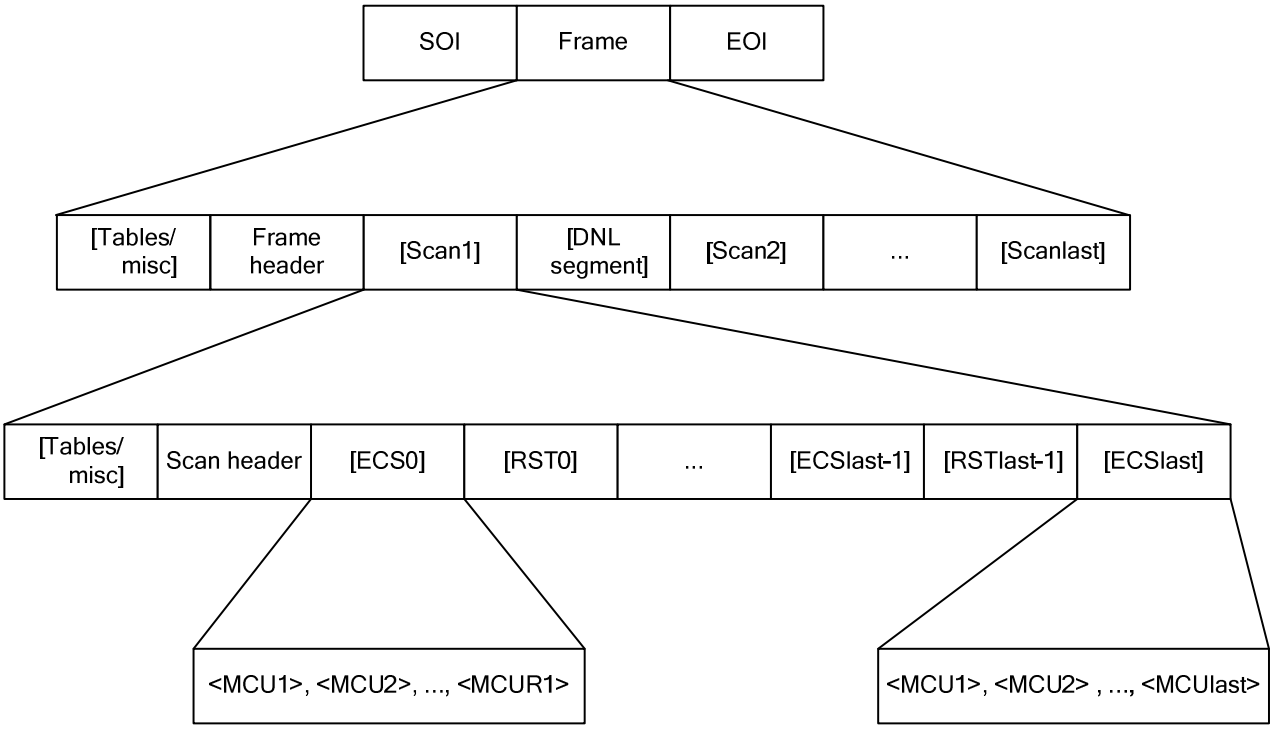


Figure 6-5 is a generalized structure diagram. For the JPEG streams, the scan header and its upper layer are parsed by software; the ECS layer and RSTn flags are parsed by hardware.

6.2.4.2 Interaction Between Software and Hardware

The JPGD is performed by software and hardware, and the software and hardware interact with each other during decoding.

- Except the process of resuming streams, software and hardware interact by frames.
  - Software and hardware interact once for each JPEG frame.
  - Software and hardware also interact once for each Motion-JPEG frame.

- Software and hardware can interact in query mode or in interrupt mode. Interrupts are generated in any of the following ways:
  - An interrupt is generated after the current picture is decoded. This interrupt indicates that the current picture is decoded completely and stored in the external memory and the JPEG decoding is complete. As the baseline picture has only one scan layer, when the decoding of the scan layer is complete, it indicates that a picture is decoded.
  - An interrupt is generated when the currently configured streams are used up. This interrupt indicates that an error occurs during the current decoding process. Therefore, the JPGD cannot continue to decode pictures and the decoding process ends.
  - After the currently configured streams are used up, the decoder is started to continue to perform decoding when new streams are configured by software–.

Contents

7 Video and Graphics Processing

7.1 VPSS

7.1.1 Overview

The video processing subsystem (VPSS) implements video processing. The functions include Gaussian 3D adaptive noise reduction (NR), deinterlacing (DEI), edge smoothing, dynamic contrast enhancement, video covering, video cropping, overlaying of videos and OSDs, scaling, adding borders to pictures, adding letterboxes to pictures, and blocking.

The VPSS has the following features:

- Processing of video sources with the 1280-pixel width by using a single frame
- A maximum of four video outputs
- Overlaying of eight regions of OSDs and videos
- OSD input format of ARGB1555, ARGB4444, or ARGB8888
- Video covering of four areas
- Spatial-domain denoising and time-domain denoising
- Deinterlacing
- Dynamic contrast enhancement of pictures
- Video mosaic overlaying
- Video cropping
- Separate configuration of the picture border size and color (the four borders of a picture must have the same color)
- Block division for the video source whose width is greater than 1280 pixels
- Configuration of register linked lists
- Input or output data format of semi-planar 420/422
- Video data compression only for the large stream channel. The other three channels do not support video data compression.

7.1.2 Features

The following describes the major features:

- Denoising: The NR module removes the Gaussian noises from pictures by configuring parameters. Then pictures become smooth and the encoding bit rate is reduced.

- DEI: The DEI module restores the interlaced video source to the progressive video source.
- Pictures added with borders: Borders can be added to picture edges, and the picture border width and color can be separately specified.
- OSD overlaying: The data at the video layer is overlaid with the data at the graphics layer, and then the overlaid data is output. At most eight regions can be overlaid with the OSD
- Picture added with the letterbox: The letterbox with configurable color and width can be added to the external edges of a valid picture
- Cover overlaying: The video or picture can be overlaid with a Cover region.
- Video cropping: A region of interest (ROI) can be cropped from the original picture and transmitted to subsequent modules for processing
- Picture blocking: A picture can be vertically divided into multiple sub-pictures with widths less than 1280 pixels. The sub-pictures are separately processed and then combined into the target picture. In blocking mode, the maximum width of the original picture is 4096 pixels.
- Scaling: Low-frequency filtering is supported when the input and output resolution are different. At most 15 times zoom out and 16 times zoom in are supported.
- Dynamic contrast adjustment: The contrast can be dynamically adjusted based on the picture luminance.
- Video mosaic overlaying: At most four regions with configurable sizes can be overlaid with the mosaic region.

7.2 VGS

7.2.1 Overview

The video graphics system (VGS) implements video and graphics processing. The functions include OSD overlaying, scaling, dynamic contrast enhancement, luminance region statistics, video cropping, video covering, drawing lines, rotation, adding borders to scaled pictures, adding letterboxes to pictures, and blocking.

The VGS has the following features:

- Processing of video sources with the1280-pixel width by using a single frame
- At most one video output
- Overlaying of OSDs and videos for one region
- OSD input format of ARGB1555, ARGB4444, or ARGB8888
- Separate configuration of the picture border size and color (the four borders of a picture must have the same color)
- Block division for the video source whose width is greater than 1280 pixels
- Configuration of register linked lists
- Video cropping
- Input or output data format of semi-planar420 or semi-planar422
- Linear storage for output data
- Video data decompression. That is, the input can be compressed video data
- Rotation by 90° or 270°

- Video covering of single areas
- Video cropping
- Statistics of the region luminance sum
- Line drawing

7.2.2 Features

The following describes the major features:

- Pictures added with borders: This function for the VGS is the same as that for the VPSS.
- OSD overlaying: This function for the VGS is the same as that for the VPSS except that at most one region can be overlaid with the OSD.
- Picture added with the letterbox: This function for the VGS is the same as that for the VPSS.
- Video cropping: This function for the VGS is the same as that for the VPSS.
- Line drawing: At most four lines with configurable angle, length, and width can be drawn on the source picture.
- Rotation: The source picture can be rotated by 90° anticlockwise or clockwise.
- Picture blocking: This function for the VGS is the same as that for the VPSS.
- Scaling: This function for the VGS is the same as that for the VPSS.
- Dynamic contrast adjustment: This function for the VGS is the same as that for the VPSS.

7.3 TDE

7.3.1 Overview

The two-dimensional engine (TDE) draws graphics using hardware. This significantly reduces the CPU usage and improves the utilization of the memory bandwidth.

The graphics data interface includes two channels: source channel 1 and source channel 2. Their functions are as follows:

- Source channel 1 implements direct copy and direct filling during a single-source operation.
- Source channel 2 implements complicated functions such as scaling and anti-flicker during a single-source operation.
- Source channel 1 works with source channel 2 to implement color blending and process the pictures in macroblock format.

7.3.2 Function Description

The TDE has the following features:

- Source bitmap 1 supports the formats of ARGB4444, ARGB1555, ARGB8888, YCbCr422, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, YCbCr888, AYCbCr8888, YCbCr422, byte, halfword, YCbCr400MB, YCbCr422MBH, YCbCr422MBV, YCbCr420MB, and YCbCr444MB.

- Source bitmap 2 supports the formats of ARGB4444, ARGB1555, ARGB8888, YCbCr422, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, YCbCr400MB, YCbCr422MBH, YCbCr422MBV, YCbCr420MB, and YCbCr444MB.
- The output bitmap supports the formats of ARGB4444, ARGB1555, ARGB8888, YCbCr422, RGB444, RGB565, RGB888, ARGB8565, CLUT1, CLUT4, CLUT8, A1, A8, YCbCr888, AYCbCr8888, YCbCr422, byte, halfword, YCbCr400MB, YCbCr422MBH, YCbCr422MBV, YCbCr420MB, and YCbCr444MB.
- Supports only the little-endian system.
- Allows the formats of source bitmap 1, source bitmap 2, and output bitmaps to be configured separately.
- Supports gamma correction and adjustable contrast and luminance.
- Supports the conversion between RGB and YCbCr.
- Supports direct copy.
- Supports direct filling.
- Supports 2D resize.
- Supports anti-flicker.
- Supports clip.
- Supports alpha blending.
- Supports colorkey.
- Supports clip mask.
- Supports inverse scanning.
- Provides status interrupts.

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Tables

8 Motion Detect Unit

8.1 Overview

As a high-performance hardware acceleration intellectual property (IP), the motion detect unit (MDU) is used to detect the motion status and video occlusion, implement modeling on the video background, and calculate the information about the object (OBJ) region. The OBJ region is a rectangular motion part of the current frame. By using the advanced eXtensible interface (AXI) master bus, the MDU reads picture information, and writes the updated information about the background, sum of absolute differences (SADs), and OBJ regions. By using the slave advanced high-performance bus (APB), the MDU obtains register configurations.

8.2 Function Description

The MDU provides the following features:

- Calculates and outputs the SAD in the unit of 8x8 or 16x16.
- Detects OBJ regions and outputs the information about the OBJ regions.
- Refreshes the background.
- Supports the input of uncompressed data but not the input of compressed data.

8.3 Operating Mode

8.3.1 Software and Hardware for Motion Detection

The software performs the following operations for the pictures to be encoded:

- Allocates the storage space in the double-data rate (DDR).
- Calls the hardware to capture videos or perform scaling.
- Schedules multiple motion detection operations, specifies and divides the regions to be detected, and generates addresses.

The hardware calculates the SADs of input pictures. The details are as follows:

- Detects OBJ regions based on the SAD and threshold, and refreshes the background.

- Outputs the information about OBJ regions, background, and SADs based on the settings of the software.

8.3.2 Software and Hardware for Video Occlusion Detection

Based on the size of OBJ regions output by the hardware, the software checks whether the occlusion threshold is reached. If the threshold is reached, the background is forbidden to refresh, but motion detection is still performed. When the size of OBJ regions is greater than the occlusion threshold, an occlusion alarm is generated.

8.4 Register Summary

Table 8-1 describes the MDU registers.

Table 8-1 Summary of the MDU registers (base address: 0x1315_0000)

Offset Address	Register	Description	Page
0x0000	MDU_INTSTAT	Interrupt status register	8-3
0x0004	MDU_INTEN	Interrupt enable register	8-4
0x0008	MDU_RAWINT	Raw interrupt register	8-5
0x000C	MDU_INTCLR	Interrupt clear register	8-5
0x0020	MDU_VEDIMGSIZE	Picture size configuration register	8-6
0x0024	MDU_MODE	Mode configuration register	8-7
0x0028	MDU_START	MDU start register	8-8
0x002C	MDU_AXI_OUTSTD_NUM	AXI outstanding configuration register	8-8
0x0040	MDU_REF_YADDR	Luminance storage address register of the reference picture	8-9
0x0044	MDU_REF_YSTRIDE	Luminance stride register of the reference picture	8-9
0x0048	MDU_CUR_YADDR	Luminance storage address register of the current picture	8-10
0x004C	MDU_CUR_YSTRIDE	Luminance stride register of the current picture	8-10
0x0060	MDU_MBSAD_ADDR	Macroblock SAD storage address register	8-11
0x0064	MDU_MBSAD_STRIDE	Macroblock SAD storage stride register	8-11
0x0070	MDU_BACKGROUND_ADDR	Luminance storage address register of the background	8-12

Offset Address	Register	Description	Page
0x0074	MDU_BACKGROUND_STRIDE	Luminance stride register of the background	8-12
0x0078	MDU_OBJ_ADDR	OBJ region storage address register	8-12
0x007C	MDU_BG_UP_WEIGHT	Background refresh weight register	8-13
0x0080	MDU_MBSAD_TH	Macroblock motion detection threshold register	8-14
0x0084	MDU_TIMEOUT	Timeout upper limit register	8-14
0x0090	MDU_WND_SIZE	SAD output window configuration register	8-14
0x0094	MDU_MIN_OBJ_SIZE	Minimum window configuration register for boundary search	8-15
0x0098	MDU_MAX_OBJ_CNT	Maximum window configuration register for boundary search	8-16
0x009C	MDU_OBJ_CNT	OBJ region information readback register	8-16
0x00A0	MDU_MAX_OBJ_SIZE	Maximum OBJ region readback register	8-16
0x00A4	MDU_TOTAL_OBJ_SIZE	All OBJ region information readback register	8-17
0x00A8	MDU_MOVE_PIX_CNT	Motion pixel statistics register for an entire frame	8-18
0x00AC	MDU_OBJ_CNT1	OBJ region information readback register based on the background	8-18
0x00B0	MDU_MAX_OBJ_SIZE1	Maximum OBJ region readback register based on the background	8-18
0x00B4	MDU_TOTAL_OBJ_SIZE1	All OBJ region information readback register based on the background	8-19
0x00B8	MDU_MOVE_PIX_CNT1	Motion pixel statistics register for an entire frame based on the background	8-19

8.5 Register Description

MDU_INTSTAT

MDU_INTSTAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	MDU_INTSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err	mdu_cfg_err	reserved																												mdu_timeout	mdu_endofpic
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	mdu_bus_err	Bus read/write error.
[30]	RO	mdu_cfg_err	Register configuration error.
[29:2]	RO	reserved	Reserved.
[1]	RO	mdu_timeout	MDU timeout interrupt. This interrupt is valid when the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT.
[0]	RO	mdu_endofpic	End of picture indicator of the MDU, active high.

MDU_INTEN

MDU_INTEN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0004	MDU_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_en	mdu_cfg_err_en	reserved																												mdu_timeout_en	mdu_endofpic_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mdu_bus_err_en	BUS read/write error interrupt enable. 0: disabled 1: enabled

[30]	RW	mdu_cfg_err_en	Register configuration error interrupt enable. 0: disabled 1: enabled
[29:2]	RO	reserved	Reserved.
[1]	RW	mdu_timeout_en	MDU timeout interrupt enable. When the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT, this interrupt is valid. 0: disabled 1: enabled
[0]	RW	mdu_endofpic_en	End of picture interrupt enable of the MDU 0: disabled 1: enabled

MDU_RAWINT

MDU_RAWINT is a raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	MDU_RAWINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_raw	mdu_cfg_err_raw	reserved																												mdu_timeout_raw	mdu_endofpic_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	mdu_bus_err_raw	Raw bus read/write error interrupt, active high.
[30]	RO	mdu_cfg_err_raw	Raw register configuration error interrupt, active high.
[29:2]	RO	reserved	Reserved.
[1]	RO	mdu_timeout_raw	Raw MDU timeout interrupt, active high.
[0]	RO	mdu_endofpic_raw	Raw end of picture interrupt of the MDU, active high.

MDU_INTCLR

MDU_INTCLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x000C	MDU_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_bus_err_clr	mdu_cfg_err_clr	reserved																												mdu_timeout_clr	mdu_endofpic_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mdu_bus_err_clr	Bus read/write error clear, active high.
[30]	RW	mdu_cfg_err_clr	Register configuration error clear, active high.
[29:2]	RO	reserved	Reserved.
[1]	RW	mdu_timeout_clr	MDU timeout interrupt clear. When the timeout detection mode of the MDU is enabled and the working cycle of the MDU is greater than the threshold configured by MDU_TIMEOUT, this interrupt is valid.
[0]	RW	mdu_endofpic_clr	End of picture indicator clear of the MDU, active high.

MDU_VEDIMGSIZE

MDU_VEDIMGSIZE is a picture size configuration register.

Offset Address	Register Name	Total Reset Value
0x0020	MDU_VEDIMGSIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				imgheightinpixelsminus1												reserved				imgwidthinpixelsminus1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved.
[28:16]	RW	imgheightinpixelsminus1	Picture height. The value is in the unit of pixel, and the configured value is obtained by subtracting 1 from the actual height. For example, if the picture height is 352 pixels, this field must be set to 351 pixels. The maximum picture height is 960 pixels.
[15:13]	RO	reserved	Reserved.

[12:0]	RW	imgwidthinpixelsminus1	Picture width. The value is in the unit of pixel, and the configured value is obtained by subtracting 1 from the actual width. For example, if the picture width is 288 pixels, this field must be set to 287 pixels. The maximum picture width is 960 pixels.

MDU_MODE

MDU_MODE is a mode configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	MDU_MODE	0x0000_019C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							mcpi_clkgate_en	mcpi_wrlock_en	timeout_en	md_mod	bg_update_en	eg_find_en	obj_out_en	sad_out_en	sad_mad_sel
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved.
[8]	RW	mcpi_clkgate_en	Clock gating enable.
[7]	RW	mcpi_wrlock_en	Register configuration lock enable. If this field is enabled, registers cannot be configured even if the MDU is started until the detection ends. This avoids modifications made to registers.
[6]	RW	timeout_en	MDU timeout detection enable. If this field is enabled, the upper limits of the working cycle that is configured using MDU_TIMEOUT by the software can be automatically queried. 0: disabled 1: enabled
[5]	RW	md_mod	Motion detection mode. 0: background algorithm 1: frame reference algorithm
[4]	RW	bg_update_en	Background refresh enable. 0: disabled 1: enabled This field is valid only when md_mod is set to 0 (background algorithm).

[3]	RW	eg_find_en	Joint detection enable for OBJ regions. 0: disabled 1: enabled If the background algorithm is selected, only the last joint detection based on the background is disabled.
[2]	RW	obj_out_en	OBJ region output enable. If this field is enabled, MDU_OBJ_ADDR must be configured. 0: disabled 1: enabled
[1]	RW	sad_out_en	SAD output enable. If this field is enabled, MDU_MBSAD_ADDR and MDU_MBSAD_STRIDE must be configured. 0: disabled 1: enabled
[0]	RW	sad_mad_sel	Number of SAD output bits. 0: 8 bits 1: 16 bits

MDU_START

MDU_START is an MDU start register.

Offset Address	Register Name	Total Reset Value
0x0028	MDU_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								mdu_start
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	mdu_start	MDU start control. 0: The MDU does not work. 1: The MDU is started.

MDU_AXI_OUTSTD_NUM

MDU_AXI_OUTSTD_NUM is an AXI outstanding configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	MDU_AXI_OUTSTD_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														axi_outstd_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved.
[2:0]	RW	axi_outstd_num	AXI outstanding configuration. The count value is numbered from 0 and the actual value is obtained by adding 1 to the count value.

MDU_REF_YADDR

MDU_REF_YADDR is a luminance storage address register of the reference picture.

Offset Address	Register Name	Total Reset Value
0x0040	MDU_REF_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_ref_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_ref_yaddr	Storage address of the Y component of the reference picture. The input raw picture must be Qword-aligned (128 bits). That is, the lower four bits of the address are 0. The hardware automatically sets the lower four bits of the address to 0.

MDU_REF_YSTRIDE

MDU_REF_YSTRIDE is a luminance stride register of the reference picture.

Offset Address	Register Name	Total Reset Value
0x0044	MDU_REF_YSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_ref_ystride																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_ref_ystride	Luminance stride, in bytes. The lower four bits of Ystride must be set to 0. This is to ensure that the address is 128-bit-aligned after the picture is wrapped. The hardware automatically sets the lower four bits of Ystride to 0. The stride must be an integral multiple of 64 bytes.

MDU_CUR_YADDR

MDU_CUR_YADDR is a luminance storage address register of the current picture.

Offset Address	Register Name	Total Reset Value
0x0048	MDU_CUR_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_cur_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_cur_yaddr	Storage address of the Y component of the raw picture. The input raw picture must be Qword-aligned (128 bits). That is, the lower four bits of the address are 0. The hardware automatically sets the lower four bits of the address to 0.

MDU_CUR_YSTRIDE

MDU_CUR_YSTRIDE is a luminance stride register of the current picture.

Offset Address	Register Name	Total Reset Value
0x004C	MDU_CUR_YSTRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_cur_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_cur_ystride	Luminance stride, in bytes. The lower four bits of Ystride must be set to 0. This is to ensure that the address is 128-bit-aligned after the picture is wrapped. The hardware automatically sets the lower four bits of Ystride to 0. The stride must be an integral multiple of 64 bytes.

MDU_MBSAD_ADDR

MDU_MBSAD_ADDR is a macroblock SAD storage address register.

Offset Address	Register Name	Total Reset Value
0x0060	MDU_MBSAD_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_mbsad_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_mbsad_addr	Address for storing the macroblock SAD. The address must be Qword-aligned. Therefore, the lower four bits must be 0.

MDU_MBSAD_STRIDE

MDU_MBSAD_STRIDE is a macroblock SAD storage stride register.

Offset Address	Register Name	Total Reset Value
0x0064	MDU_MBSAD_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_mbsad_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.

[15:0]	RW	mdu_mbsad_stride	Macroblock SAD stride, in bytes. The stride must be 128-bit-aligned. Therefore, the lower four bits must be 0.

MDU_BACKGROUND_ADDR

MDU_BACKGROUND_ADDR is a luminance storage address register of the background.

Offset Address	Register Name	Total Reset Value
0x0070	MDU_BACKGROUND_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bg_yaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	bg_yaddr	Background address. The address must be Qword-aligned. Therefore, the lower four bits must be 0.

MDU_BACKGROUND_STRIDE

MDU_BACKGROUND_STRIDE is a luminance stride register of the background.

Offset Address	Register Name	Total Reset Value
0x0074	MDU_BACKGROUND_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bg_ystride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	bg_ystride	Background stride, in bytes. The stride must be 128-bit-aligned. Therefore, the lower four bits must be 0.

MDU_OBJ_ADDR

MDU_OBJ_ADDR is an OBJ region storage address register.

Offset Address	Register Name	Total Reset Value
0x0078	MDU_OBJ_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	obj_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	obj_addr	Address for storing OBJ regions. The address must be Qword-aligned. Therefore, the lower four bits must be 0. An OBJ region is stored as follows: The coordinates of the left, top, right, and bottom points of the OBJ region are stored in sequence in four 16-bit spaces. Therefore, two 32-bit DDRs are used to store an OBJ region. When the DDR is allocated by using the software, the minimum DDR size is calculated as follows: 2 x 32 bits x Maximum number of OBJ regions

MDU_BG_UP_WEIGHT

MDU_BG_UP_WEIGHT is a background refresh weight register.

Offset Address	Register Name	Total Reset Value
0x007C	MDU_BG_UP_WEIGHT	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																src_weight								weight_sum_exp_2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:8]	RW	src_weight	New picture weight.
[7:0]	RW	weight_sum_exp_2	Exponent of 2 to the weighted sum. When the MDU generates a new background by overlaying the source picture with the existing background, the following formula is used: (Background pixel x ((1<<weight_sum_exp_2) – src_weight) + Pixel of source picture x bg_weight) >> weight_sum_exp_2) The background weight bg_weight is calculated as follows: ((1<<weight_sum_exp_2) – src_weight) The greater the value obtained from background weight bg_weight minus source weight src_weight, the more slowly the background is refreshed. The default value is 0x1, and the maximum value is 0x8.

MDU_MBSAD_TH

MDU_MBSAD_TH is a macroblock motion detection threshold register.

Offset Address	Register Name	Total Reset Value
0x0080	MDU_MBSAD_TH	0x0000_001E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mdu_mbsad_th															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	mdu_mbsad_th	Threshold for detecting the motion status of the 4x4 macroblock. All calculations of the MDU are based on the 4x4 macroblock.

MDU_TIMEOUT

MDU_TIMEOUT is a timeout upper limit register.

Offset Address	Register Name	Total Reset Value
0x0084	MDU_TIMEOUT	0x0360_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mdu_timeout																															
Reset	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	mdu_timeout	Maximum number of working cycles.

MDU_WND_SIZE

MDU_WND_SIZE is a SAD output window configuration register.

Offset Address	Register Name	Total Reset Value
0x0090	MDU_WND_SIZE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sad_wnd_size
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	RW	sad_wnd_size	Size of the SAD output window. The calculations of the MDU are based on the 4x4 macroblock. After the sad_out_en bit of the mode register is enabled, the MDU adds the values of multiple 4x4 macroblocks based on the settings of sad_wnd_size, and outputs the value to the DDR. 0: 8x8 1: 16x16 (default)

MDU_MIN_OBJ_SIZE

MDU_MIN_OBJ_SIZE is the minimum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0094	MDU_MIN_OBJ_SIZE	0x0300_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	egsearch_timeout																min_obj_size_h								min_obj_size_w							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	egsearch_timeout	Boundary search timeout. If the number of points of an OBJ region is greater than the value, the boundary search of the OBJ region stops, and the search for the next region starts.
[15:8]	RW	min_obj_size_h	Minimum height of the OBJ region. The OBJ region whose height is smaller than this value is not reported. The value 1 of min_obj_size_h indicates a 4x4 macroblock.
[7:0]	RW	min_obj_size_w	Minimum width of the OBJ region. The OBJ region whose width is smaller than this value is not reported. The value 1 of min_obj_size_w indicates a 4x4 macroblock.

MDU_MAX_OBJ_CNT

MDU_MAX_OBJ_CNT is the maximum window configuration register for boundary search.

Offset Address	Register Name	Total Reset Value
0x0098	MDU_MAX_OBJ_CNT	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																max_obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved.
[15:0]	RW	max_obj_cnt	Maximum value for detecting the OBJ regions.

MDU_OBJ_CNT

MDU_OBJ_CNT is an OBJ region information readback register.

Offset Address	Register Name	Total Reset Value
0x009C	MDU_OBJ_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index																obj_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index	Maximum OBJ region index. For the statistics register whose name does not contain the digital suffix, the statistics are obtained when the SAD is calculated and the OBJ region is searched for the first time based on the frame reference algorithm or background algorithm.
[15:0]	RO	obj_cnt	Number of detected OBJ regions.

MDU_MAX_OBJ_SIZE

MDU_MAX_OBJ_SIZE is a maximum OBJ region readback register.

Offset Address	Register Name	Total Reset Value
0x00A0	MDU_MAX_OBJ_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	max_obj_size	Maximum size of the OBJ region. This value is used to detect video occlusion. The value is in the unit of pixel. The software calculates the percentage of OBJ regions based on this value and compares the value with the size threshold of the OBJ region. If the value is greater than the threshold, the frame occlusion is considered, and the subsequent frames for detecting video occlusion are not used to refresh the background. In addition, the system checks whether the size of the OBJ region is greater than the threshold for consecutive times. If the occlusion time is greater than the time threshold, video occlusion is considered, and an alarm is generated.

MDU_TOTAL_OBJ_SIZE

MDU_TOTAL_OBJ_SIZE is an all OBJ region information readback register.

Offset Address	Register Name	Total Reset Value
0x00A4	MDU_TOTAL_OBJ_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_obj_size	Total size of all OBJ regions. This value is used to detect whether a camera is sprayed. The working principle is the same as that of the max_obj_size field. The MDU adds the sizes of all OBJ regions. The size is in the unit of pixel. The size of each OBJ region is calculated as follows: number of 4x4 macroblocks x 16 **NOTE** • In some cases, the OBJ regions may overlap, and the total size of OBJ regions may be greater than the size of the original picture. • Based on the 4x4 macroblock, the height and width of each OBJ region are calculated as follows: Width = (Horizontal coordinate of the right point – Horizontal coordinate of the left point) + 1 Height = (Vertical coordinate of the bottom point – Vertical coordinate of the top point) + 1

MDU_MOVE_PIX_CNT

MDU_MOVE_PIX_CNT is a motion pixel statistics register for an entire frame.

Offset Address	Register Name	Total Reset Value
0x00A8	MDU_MOVE_PIX_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	move_pix_cnt	Number of motion pixels of an entire frame. This value can be used to detect video occlusion. The working principle is the same as that of the max_obj_size field. Note: The value of this register is based on pixels. Therefore, the register value may be different from the value of total_obj_size.

MDU_OBJ_CNT1

MDU_OBJ_CNT1 is an OBJ region information readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00AC	MDU_OBJ_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_index1																obj_cnt1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	max_obj_index1	Index of the maximum OBJ region based on the background. The registers with the suffix 1 indicate statistics registers. The statistics are obtained when the background algorithm is used and the SAD is calculated and the OBJ region is searched for the second time.
[15:0]	RO	obj_cnt1	Number of detected OBJ regions based on the background.

MDU_MAX_OBJ_SIZE1

MDU_MAX_OBJ_SIZE1 is a maximum OBJ region readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00B0	MDU_MAX_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	max_obj_size1	Maximum size of the OBJ region based on the background. This value is used to detect video occlusion, and is in the unit of pixel. The software calculates the percentage of OBJ regions based on this value and compares the value with the size threshold of the OBJ region. If the value is greater than the threshold, the frame occlusion is considered, and the subsequent frames for detecting video occlusion are not used to refresh the background. In addition, the system checks whether the size of the OBJ region is greater than the threshold for consecutive times. If the occlusion time is greater than the time threshold, video occlusion is considered, and an alarm is generated.

MDU_TOTAL_OBJ_SIZE1

MDU_TOTAL_OBJ_SIZE1 is a all OBJ region information readback register based on the background.

Offset Address	Register Name	Total Reset Value
0x00B4	MDU_TOTAL_OBJ_SIZE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_obj_size1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	total_obj_size1	Sum of the sizes of all OBJ regions based on the background. This value is used to detect whether a camera is sprayed. The working principle is the same as that of the max_obj_size field.

MDU_MOVE_PIX_CNT1

MDU_MOVE_PIX_CNT1 is a motion pixel statistics register for an entire frame based on the background.

Offset Address	Register Name	Total Reset Value
0x00B8	MDU_MOVE_PIX_CNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	move_pix_cnt1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	move_pix_cnt1	Number of motion pixels of an entire frame based on the background. This value can be used to detect video occlusion. The working principle is the same as that of the max_obj_size field.

Contents

Figures

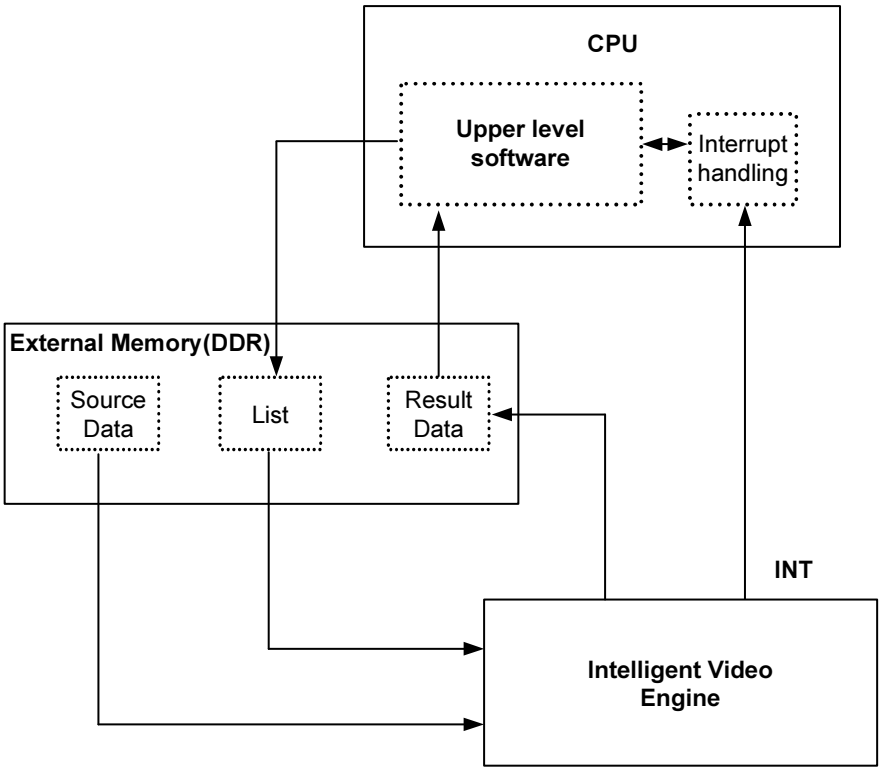
Tables

9 IVE

9.1 Overview

The intelligent video engine (IVE) module is used to accelerate hardware processing. It provides a series of basic calculation functions and some time-consuming functions used in the intelligent analysis algorithm.

Figure 9-1 Position of the IVE in the system



9.2 Function Description

The IVE has the following features:

- DMA: Supports direct copying, alternative copying, and memory filling.
- Filter: Supports 5x5 template filtering.
- Color space conversion (CSC): Supports the color space conversion of YUV2RGB, YUV2HSV, YUV2LAB, and RGB2YUV.
- FilterAndCSC: Combines 5x5 template filtering and CSC.
- Sobel: Supports the Sobel-like gradient calculation of 5x5 template.
- MagAndAng/Canny: Supports 5x5 template calculation and Canny edge extraction.
- Erode: Supports 5x5 template erode.
- Dilate: Supports 5x5 template dilate.
- Thresh\Thresh_S16\Thresh_U16: Supports image thresh processing.
- And\Or\Xor: Supports the AND, OR, or XOR operation on two images.
- Add\Sub: Deals with the weighted plus and minus of two images.
- Integ: Supports the integral calculation.
- Hist: Supports the histogram statistics.
- Map: Assigns values to images by using 256-level mapping.
- 16BitTo8Bit: Performs linear conversion from 16-bit data to 8-bit data.
- OrdStatFilter: Supports the sequence statistic filtering, including the median filtering, maximum filtering, and minimum filtering.
- NCC: Calculates the correlation coefficients of two images with the same size.
- CCL: Marks connected regions.
- GMM: Creates the GMM for a gray image and RGB image.
- LBP: Supports the calculation in simple partial thresh mode.
- NormGrad: Performs a normalized gradient calculation.
- LKOpticalFlow: Tracks the LK optical flow.
- STCorner: Detects the ShiTomasi point.
- GradFg: Supports the gradient foreground calculation.
- MatchBgModel\UpdateBgModel: Supports background match and background refresh.
- Sum of absolute difference (SAD): Supports the calculation of the accumulated sum of the absolute pixel differences corresponding to two images by block.
- Supports separate soft reset.
- Supports 128-bit AXI bus and 32-bit APB.
- Supports linked-list interrupt, node interrupt, and timeout interrupt.
- Supports input formats including SP400, semi-planar420 (SP420), semi-planar422 (SP422), package, and planar.
- Supports output formats including SP400, SP420, SP422, package, and planar.
- Supports non-16-byte-aligned read and write addresses for some operators.

9.3 Operating Mode

9.3.1 Input and Output Data Formats

The w and h in Figure 9-2 to Figure 9-12 indicate the width and height of images in pixels. Unless otherwise specified, the sequence for storing data is the same as that in the little endian

system. The following sections use word as the storage unit. In actual applications, the data alignment format varies with operators. The input and output format for operators described in section 9.3.2 "Supported Functions" are also different.

Figure 9-2 SP422 storage format

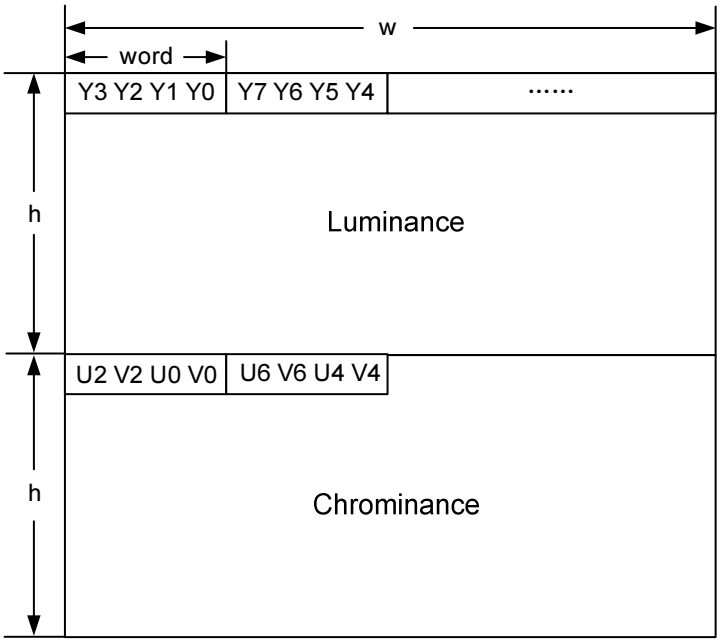


Figure 9-3 SP420 storage format

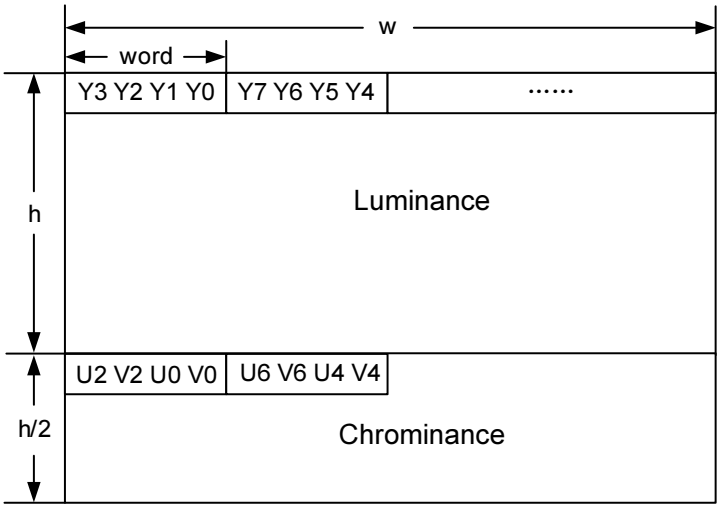


Figure 9-4 Storage format of the 8-bit single component data in the memory

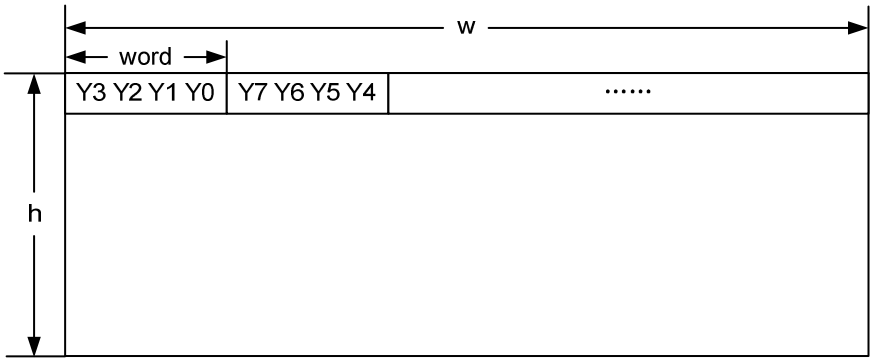


Figure 9-5 Package storage format

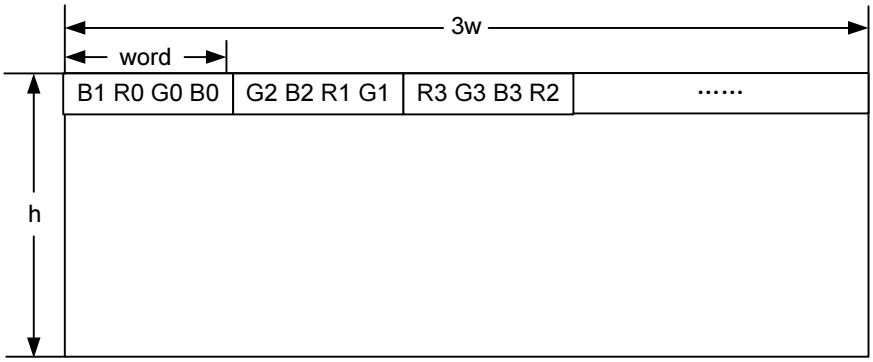


Figure 9-6 Planar storage format

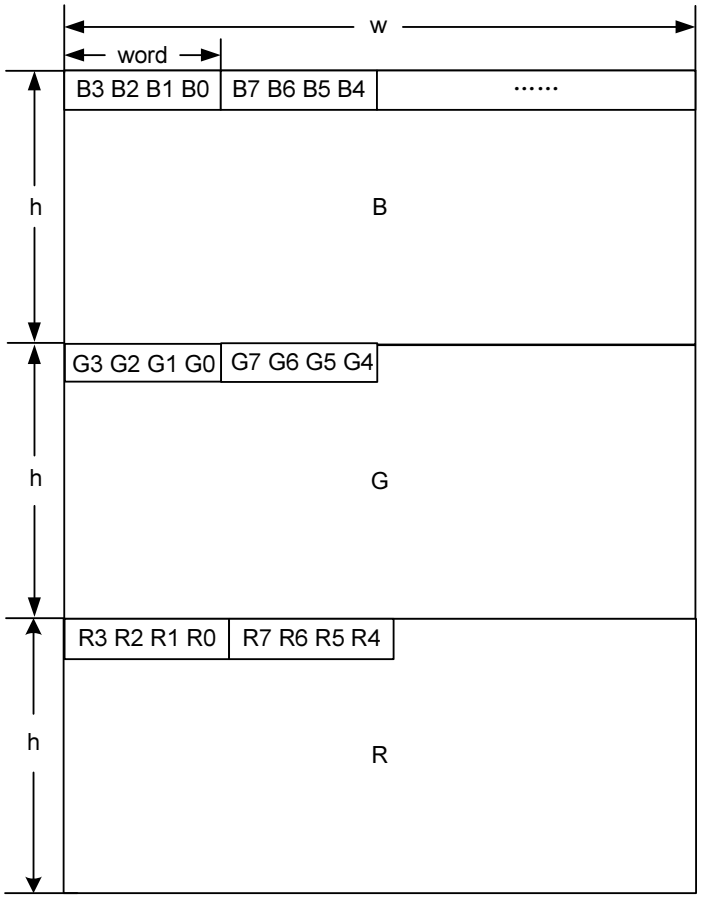


Figure 9-7 Storage format of the 16-bit single component data in the memory

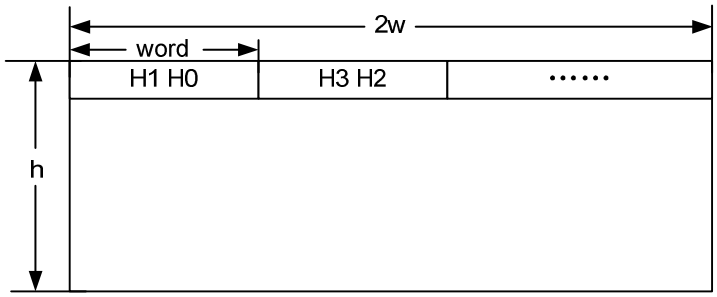


Figure 9-8 Storage format of the 32-bit single component data in the memory

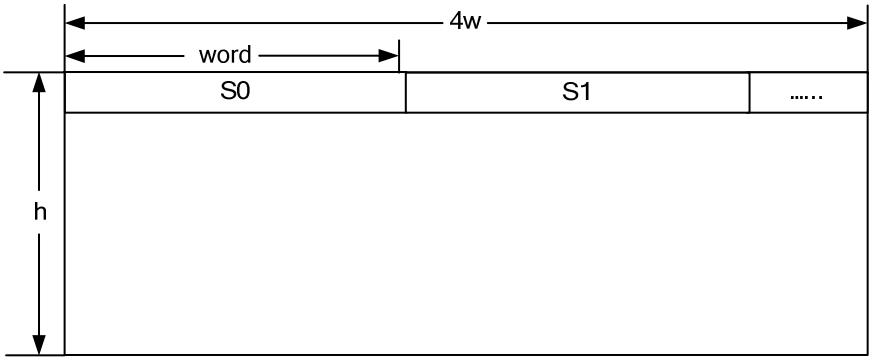


Figure 9-9 Storage format of the 64-bit single component data in the memory

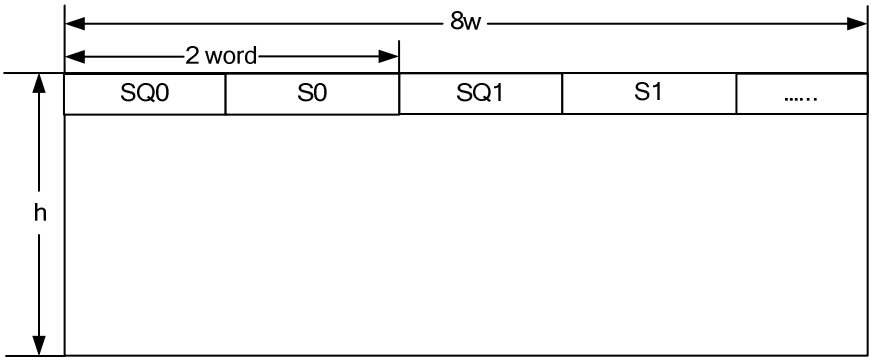


Figure 9-10 Storage format of NCC output data in the memory

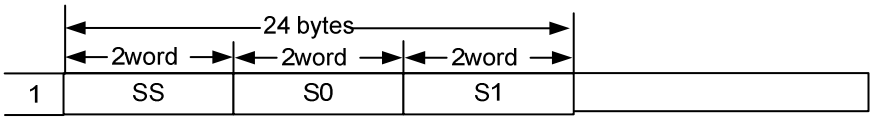
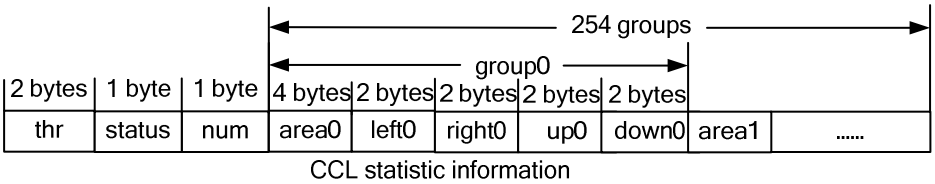
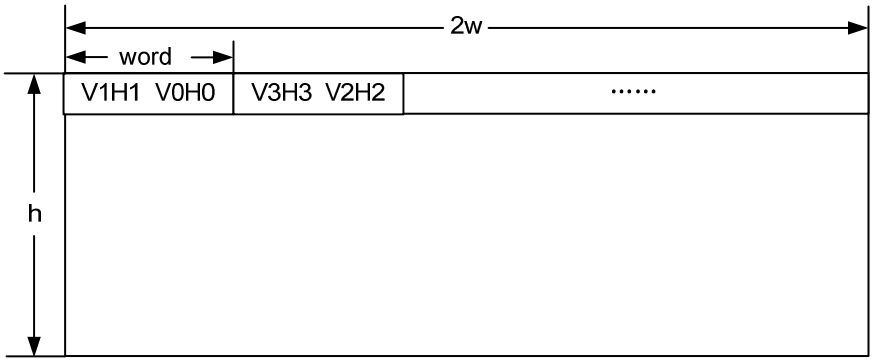


Figure 9-11 Storage format of CCL statistics in the memory (in sequence)



CCL statistic information

Figure 9-12 Storage format of 16-bit interleaving data (in the horizontal and vertical directions) in the memory



9.3.2 Supported Functions

DMA

1. Direct copy mode

This mode allows you to quickly transfer the data of rectangle regions. In this mode, the source data is transferred to the destination region through the internal fast channel, and directly overwrites the data of the destination region.

- Region size (in byte): 32 x 1 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single-component data, as shown in Figure 9-4.

2. Alternative copy mode

This mode allows you to transfer the data of rectangle regions indirectly. In this mode, the source data with a specified size is transferred to the destination region at a specified distance in horizontal and vertical directions.

- Region size (in byte): 32 x 1 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single-component data, as shown in Figure 9-4.
- Others: The width of the source data must be an integral multiple of the distance.

3. Memset mode (3 bytes)

This mode allows you to set the memory in rectangle regions, and fill the destination region by three bytes.

- Region size (in byte): 32 x 1 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.

- Input and output formats: No input data is available. The output is 8-bit single-component data, as shown in Figure 9-4.

4. Memset mode (8 bytes)

This mode allows you to set the memory in rectangle regions, with 8 byte as the unit for filling the target region.

- Region size (in byte): 32 x 1 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: No input data is available. The output is 8-bit single-component data, as shown in Figure 9-4.

Filter

The filter function allows the output of the source image after filtering it based on the 5x5 template.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the strides of the output components must be the same.
- The following lists the three input and output formats:
  - Both the input and output are 8-bit single-component data, as shown in Figure 9-4.
  - Both the input and output are SP420 data, as shown in Figure 9-3.
  - Both the input and output are SP422 data, as shown in Figure 9-2.

CSC

The CSC among YUV2RGB, YUV2HSV, YUV2LAB, and RGB2YUV is supported.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the strides of the output components must be the same.
- Input and output formats:
  - SP420 > package; SP420 > planar
  - SP422 > package; SP422 > planar
  - Package > SP420; package > SP422
  - planar > SP420; planar > SP422

  Figure 9-3 and Figure 9-2 show the SP420 format and SP422 format respectively.

  Figure 9-5 shows the package format.

  Figure 9-6 shows the planar format.

FilterAndCSC

The FilterAndCSC function indicates that the YUV SP420/SP422 images are filtered based on the 5x5 template and then the color space is converted into YUV2RGB for output.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the strides of the output components must be the same.

- Input and output formats:
  - SP420 > package; SP420 > planar
  - SP422 > package; SP422 > planar

  Figure 9-3 and Figure 9-2 show the SP420 format and SP422 format respectively. Figure 9-5 shows the package format. Figure 9-6 shows the planar format.

Sobel

This function implements vertical and horizontal Sobel filtering based on the 5x5 template.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the strides of the output components must be the same.
- Input and output formats:
  - The input is an 8-bit single-component image, as shown in Figure 9-4.
  - Only H or V is output, as shown in Figure 9-7.
  - Both H and V are output, as shown in Figure 9-7.

MagAndAng

The MagAndAng indicates that gradient magnitude and angle are calculated. It supports the thresh operation for TO_ZERO.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the strides of the output components must be the same.
- Input and output formats:
  - The input is the 8-bit single-component image, as shown in Figure 9-5.
  - The output is the 16-bit single-component amplitude image, as shown in Figure 9-7.
  - The output is the 8-bit single-component angle image, as shown in Figure 9-4.

Dilate

This function implements dilation of a binary image based on the 5x5 template.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single-component data, as shown in Figure 9-4.

Erode

This function implements erosion of a binary image based on the 5x5 template.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single-component data, as shown in Figure 9-4.

Thresh

This function performs thresh processing for an image using specified thresh. Eight modes are available.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single-component data, as shown in Figure 9-4.

And

This function implements the calculation for source data 2 and 1, and outputs the data to the destination region.

- Resolution: 64 x 64 to 1920 x 1080. The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is an 8-bit single-component data of source 1.
  - The input is an 8-bit single-component data of source 2.
  - The output is the 8-bit single-component data that is the result after calculation, as shown in Figure 9-4.

Sub

This function performs the subtraction of the data from sources 2 and 1, and outputs the data to the destination region.

- Resolution: 64 x 64 to 1920 x 1080. The two input images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - An 8-bit single-component minuend
  - An 8-bit single-component subtrahend
  - An 8-bit single-component data that is the result after calculation, as shown in Figure 9-4

Or

This function performs the Or calculation of the data from sources 2 and 1, and outputs the data to the destination region.

- Resolution: 64 x 64 to 1920 x 1080. The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:

- The two input images are 8-bit single-component images.
- The output is an 8-bit single-component image, as shown in Figure 9-4.

Integral

This function performs the calculation of integrogram and square sum integrogram, and supports the output of sum integrogram, square sum integrogram, and the combination of the sum integrogram and square sum integrogram (the accumulated component sum occupied the lower 28-bit, and the accumulated component square sum occupied the upper 36-bit).

- Resolution: 32 x 16 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is an 8-bit single-component image, as shown in Figure 9-4.
  - As shown in Figure 9-8, if a sum integrogram is output, the output is a 32-bit single-component image. As shown in Figure 9-9, if a square sum integrogram is output or is output together with a sum integrogram, the output is a 64-bit single-component image.

Histogram

This function performs the 256-segment histogram statistics. The input is a single component, and the output is the statistics of a 32-bit 256-segment histogram.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is 8-bit single-component data, as shown in Figure 9-4.
  - The output is a 32-bit single-component data that is the statistical result, as shown in Figure 9-8.

Thresh_S16

This function implements thresh processing of signed 16-bit data to signed 8-bit data. It supports four comparison modes.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is 16-bit single-component data, as shown in Figure 9-7.
  - The output is the converted 8-bit single-component data, as shown in Figure 9-4.

Thresh_U16

This function implements thresh processing of unsigned 16-bit data to unsigned 8-bit data. It supports two comparison modes.

- Resolution: 64 x 64 to 1920 x 1080

- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is 16-bit single-component data, as shown in Figure 9-7.
  - The output is the converted 8-bit single-component data, as shown in Figure 9-4.

16BitTo8Bit

This function implements linear conversion of 16-bit data to 8-bit data. It supports four comparison modes.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output formats:
  - The input is 16-bit data, as shown in Figure 9-7.
  - The output is the converted 8-bit data, as shown in Figure 9-4.

OrdStatFilter

Supports median filtering, maximum value filtering, and minimum filtering in sequence based on a 3x3 template.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output formats: Both the input and output are 8-bit single-component images, as shown in Figure 9-4.

Map

This function outputs new data by mapping the source data to the 256-segment unsigned 8-bit mapping configured by the user.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses must be byte-aligned, and the mapping table and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is 8-bit single-component data, as shown in Figure 9-4.
  - The input is an 8-bit mapping table with a fixed entry length of 256.
  - The output is 8-bit single-component data after mapping, as shown Figure 9-4.

Add

This function implements the sum of the weighted values of two gray images. The weight of the two images can be configured independently.

- Resolution: 64 x 64 to 1920 x 1080. The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.

- Input and output data formats:
  - The input is the data of two 8-bit single-component images, as shown in Figure 9-4.
  - The output is the sum of data of two 8-bit single-component image, as shown Figure 9-4.

Xor

This function performs the Xor operation for two binary image data.

- Resolution: 64 x 64 to 1920 x 1080. The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single-component images, as shown in Figure 9-4.
  - The output is 8-bit single-component data after the Xor operation, as shown in Figure 9-4.

NCC

This function calculates the cross correlation coefficient of two gray scale images of the same resolution.

- Resolution: 20 x 20 to 1920 x 1080. The two inputted images should be of the same resolution.
- Address alignment mode: The input address must be byte-aligned, and the output address as well as the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single-component images, as shown in Figure 9-4.
  - The output contains three types of data, namely the accumulative product of two images, accumulative product of square sum of image 1, and the accumulative product of square sum of image 2 (in sequence), as shown in Figure 9-10.

CCL

This function marks eight connected regions.

- Resolution: 64 x 64 to 1024 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single-component image, as shown in Figure 9-4. The 16-bit output data indicates the minimum area of the output valid connected components.
  - The 8-bit output data indicates whether the area of the detected connected components is greater than the threshold.
  - The output is the coordinate and area of the circumscribed rectangle for each connected component, as shown in Figure 9-11. The original image is changed to an 8-bit single component image after the labeling of the connected components, as shown in Figure 9-4.

GMM

The GMM performs the inputted GMM background modeling for the gray images and RGB package images. Three or five Gauss models are supported.

- Resolution: 64 x 64 to 720 x 576
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single-component image or RGB package image, as shown in Figure 9-4 and Figure 9-5.
  - The input is the model data.
  - The output is 8-bit single-component foreground data, as shown in Figure 9-4.
  - The output is the updated model data.
  - The output is the background data and the corresponding input is an 8-bit single-component image or RGB package image, as shown in Figure 9-4 and Figure 9-5.

CannyHysEdge

- This function performs the threshold processing for the magnetic hysteresis, limited non-maximum values, outputted strong and weak edge image and the strong edge coordinate detected by the Canny edge resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single-component angle image, as shown in Figure 9-4.
  - The input is a 16-bit single-component amplitude image, as shown in Figure 9-7.
  - The output is an 8-bit single-component edge mark image, as shown in Figure 9-4.
  - The output is a 32-bit single-component data stack, as shown in Figure 9-8.
  - The output is a 32-bit value that indicates the stack size.

LBP

This function performs the partial thresh processing. It extracts the texture of partial images.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input data format:
  - The input is 8-bit single-component data.
  - The output is 8-bit single-component destination data, as shown in Figure 9-4.

NormGrad

This function performs the normalized gradient calculation. The gradient components are all normalized to eight bits.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the strides of the output components must be the same.

- Input and output data formats:
  - The input is 8-bit single-component data, as shown in Figure 9-4.
  - When out_fmt is set to 0x00, 0x01, or 0x02, the output is 8-bit single-component data, as shown in Figure 9-4. When out_fmt is set to 0x03, the output is 16-bit interleaving data of H and V, as shown in Figure 9-12.

LKOpticalFlow

This function performs the optical flow estimation. A maximum of 200 points are supported.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single-component image of the previous frame.
  - The input is an 8-bit single-component image of the current frame, as shown in Figure 9-4.
  - The input is the angular coordinate, as shown in Figure 9-9. The lower 32 bits indicate the horizontal coordinate, and the upper 32 bits indicate the vertical coordinate.
  - The angular motion vector is both the input and the output, as shown in Figure 9-9. The lower 32 bits indicate the status of success and failure of the tracing. The upper 32 bits indicate the angle displacement vector.

STBoxFltAndEigCalc

This function performs the box filtering during the point calculation, and calculates the response value and maximum response value of the points.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input data format:
  - The input is the vertical and horizontal 16-bit interleaving data, as shown in Figure 9-12.
  - The output is 16-bit single-component data, as shown in Figure 9-7.
  - The output is the 16-bit maxEig.

STCandiCorner

This function filters the points from Shi-Tomasi-like candidate points.

- Resolution: 64 x 64 to 1920 x 1080. The resolution of the inputted two images should be the same.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single-component image.
  - The output is an 8-bit single-component image, as shown in Figure 9-4.

GradFg

This function calculates the gradient foreground based on the gradient of the background images and current frame images.

- Resolution: 64 x 64 to 1920 x 1024
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the background differential foreground image, as shown in Figure 9-4.
  - The input is the current gradient interleaving image.
  - The input is the background gradient interleaving image, as shown in Figure 9-12.
  - The output is the gradient foreground image, as shown in Figure 9-4.

MatchBgModel

This function performs the background model matching based on CodeBook.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the strides of the output components must be the same.
- Input and output data formats:
  - The input is the current gray image (8-bit single component).
  - The input is the foreground status flag (8-bit single component), as shown in Figure 9-4.
  - The input is 24-byte model data.
  - The output is the background differential foreground image (8-bit single component).
  - The output is the frame differential images (8-bit single component)
  - The output is the forehead status flag (8-bit single component), as shown in Figure 9-4.
  - The output is the 24-byte model data.
  - The output is a 64-bit statistical value.

UpdateBgModel

This function performs the background model refresh based on CodeBook.

- Resolution: 64 x 64 to 1920 x 1080
- Address alignment mode: The input and output addresses and strides must be 16-byte-aligned, and the strides of the output components must be the same.
- Input and output data formats:
  - The input is the foreground status flag (8-bit single component), as shown in Figure 9-4.
  - The input is the 24-byte model data.
  - The output is the background differential foreground image (8-bit single component).
  - The output is a background gray image (8-bit single component)
  - The output is a gray image in the change state (8-bit single component)

- The output is a foreground image in the change state (8-bit single component), as shown in Figure 9-4.
- The output is the pixel life period in the change state (16-bit single component), as shown in Figure 9-7.
- The output is the 24-byte model data.
- The output is a 64-bit statistical value.

SAD

This function calculates the accumulated sum of the absolute pixel differences corresponding to two images by block.

- The resolution ranges from 64 x 64 to 1920 x 1080. The width and height of the image must be an integral multiple of the block size.
- Address alignment mode: The input and output addresses and strides must be byte-aligned.
- Input and output data formats:
  - The inputs are two 8-bit single-component images with the same resolution, as shown in Figure 9-4.
  - The results of output depend on the configured value of out_fmt:

    In multiplexed 16-bit SAD output mode, the 16-bit SAD image is output based on the specified block size and the 8-bit SAD binary image after thresh processing is output, as shown in Figure 9-7 and Figure 9-4 respectively.

    In multiplexed 8-bit SAD output mode, the 8-bit SAD image is output based on the specified block size and the 8-bit SAD binary image after thresh processing is output, as shown in Figure 9-4.

    In single 16-bit SAD output mode, the 16-bit SAD image is output based on the specified block size, as shown in Figure 9-7.

    In single 8-bit SAD output mode, the 8-bit SAD image is output based on the specified block size, as shown in Figure 9-4.

    In single binary image SAD output mode, the 8-bit SAD binary image after thresh processing is output based on the specified block size, as shown in Figure 9-4.

9.4 Register Summary

Table 9-1 describes IVE registers.

Table 9-1 Summary of IVE registers (base address: 0x1306_0000)

Offset Address	Register	Description
0x0000	IVE_START	IVE start configuration register
0x0004	INT_EN	IVE interrupt enable register
0x0008	INT_RW	IVE clear interrupt register
0x000C	INT_STATUS	IVE interrupt status register

Offset Address	Register	Description
0x0010	LIST_POINTER	Linked list start address register
0x0014	IVE_STATUS	IVE working status register
0x0018	IVE_TASK_ID	ID register for the tasks processed by the IVE at the previous time
0x0030	NODE_CLK_VALUE	Register for the number of cycles consumed by the preceding node
0x0034	CLK_GT_EN	Clock gating of the IVE internal module
0x0040	NODE_DONE_CNT	Register for the number of processed nodes
0x0044	LIST_DONE_CNT	Register for the number of processed linked lists
0x0048	INT_DONE_CNT	Count register for the node interrupts reported by the current linked list
0x004C	INT_RD_CNT	Count register for the interrupts that have been successfully read by the current linked list
0x0050	INT_WR_CNT	Count register for the interrupts that have been cleared by writing the current linked list
0x0054	AXI_INFO	Read and write outstanding number register
0x0060	IVE_OVER_TIME_THR	Overtime interrupt threshold register
0x0064	IVE_OVER_TIME_CNT	Register for the dynamic counting number of the operator working cycle
0x0068	CHAIN_STAT_CLK_VALUE	Register for the number of cycles consumed by the preceding linked list
0x006C	CHAIN_CYCLE_CNT	Register for the counting number of the current linked list cycles

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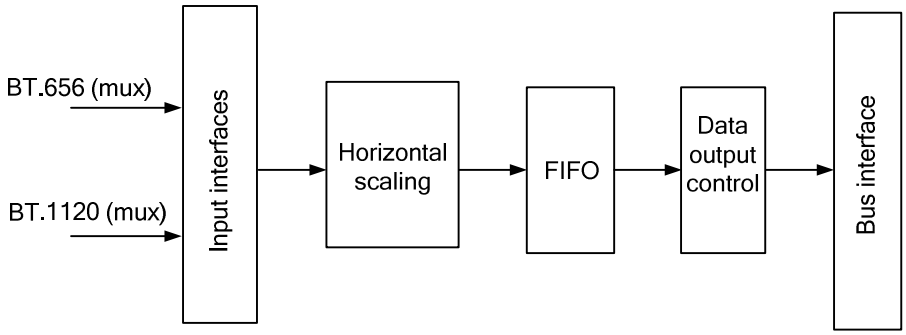
10 Video Interfaces

10.1 VICAP

10.1.1 Overview

The video capture (VICAP) module receives video data over the BT.656 interface (mux) or BT.1120 interface, and stores the data in the specified addresses of the DDR. During this process, the VICAP module performs horizontal scaling on video data (or simple down sampling or scaling based on channels) and outputs multiple video streams. Figure 10-1 shows the functional block diagram of the VICAP module.

Figure 10-1 Functional block diagram of the VICAP module



10.1.2 Features

The VICAP module has the following features:

- Supports the maximum input resolution of 2048 x 1536.
- The Hi3521A Supports four external BT.656 interfaces or two external BT.1120 interfaces.
- The Hi3520D V300 Supports two external BT.656 interfaces or one external BT.1120 interfaces.
- The Hi3521A Internally supports four ports and processes 16-channel videos. Each channel supports interlaced and progressive input modes.

- The Hi3520D V300 Internally supports two ports and processes 8-channel videos. Each channel supports interlaced and progressive input modes.
- Supports dual-edge sampling for the input interfaces.
- Supports BT.656 (mux) and BT.1120 timings.
- Supports SMPTE293M/ITU-R BT.1358 timing (480p/576p), SMPTE 274M/BT.1120 timings (1080i/1080p), and SMPTE 296M timing (720p).
- Supports at most 2x horizontal zoom out for each channel.
- Supports 1/2 vertical line discarding for each channel.
- Supports configurable 2-level bus priorities for each channel.
- Supports the Cover overlaying of four regions for each channel. The color of the Cover region is configurable.
- Obtains data in a specified window for each channel.
- Obtains statistical information about the total luminance of the obtained data.
- Supports mirror and flip.
- Supports the output storage modes of SPYCbCr 4:2:0 and SPYCbCr 4:2:2 for each channel.
- Supports the single-component luminance output mode for each channel.

10.1.3 Function Description

10.1.3.1 Typical Application

The VICAP module captures video data in multiple input timings and stores the captured data in the DDR. By using different function modes configured by the system, the VICAP module can connect to different external VI interfaces, supporting multiple external input devices.

The Hi3521A VICAP uses 36 pins, four clocks, and 32 data lines. It also provides four ports and 16 channels. Each port parses the timings of an interconnected chip, and each channel processes 1-channel video signals. Every two ports correspond to eight channels (pt0 and pt1 correspond to ch0−ch7; pt2 and pt3 correspond to ch8−ch15). The details are as follows:

- Four ports (BT.656) are used to connect four chips with 8-bit data lines.
- Two ports (BT.1120) are used to connect two chips with 16-bit data lines.

Each port can receive 2-channel 720p data, 4-channel D1/960H data, or 1-channel 1080p data in single-edge sampling mode, and receive 4-channel 720p data, 2-channel 1080p data, or 1-channel 3-megapixel data in dual-edge sampling mode.

The Hi3521A VICAP module supports the following typical input modes:

- 16-channel D1/960H (single-edge sampling)
- 8-channel 720p (single-edge sampling)
- 4-channel 1080p (single-edge sampling)
- 16-channel 720p (dual-edge sampling)
- 8-channel 1080p (dual-edge sampling)
- 4-channel 3 megapixels (dual-edge sampling)

The Hi3520D V300 VICAP uses 18 pins, two clocks, and 16 data lines. It also provides two ports and eight channels.

The VICAP module of Hi3520D V300 supports at most two ports (pt0 and pt1), which correspond to ch0−ch7.

The Hi3520D V300 VICAP module supports the following typical input modes:

- 8-channel D1/960H (single-edge sampling)
- 4-channel 720p (single-edge sampling)
- 2-channel 1080p (single-edge sampling)
- 8-channel 720p (dual-edge sampling)
- 4-channel 1080p (dual-edge sampling)

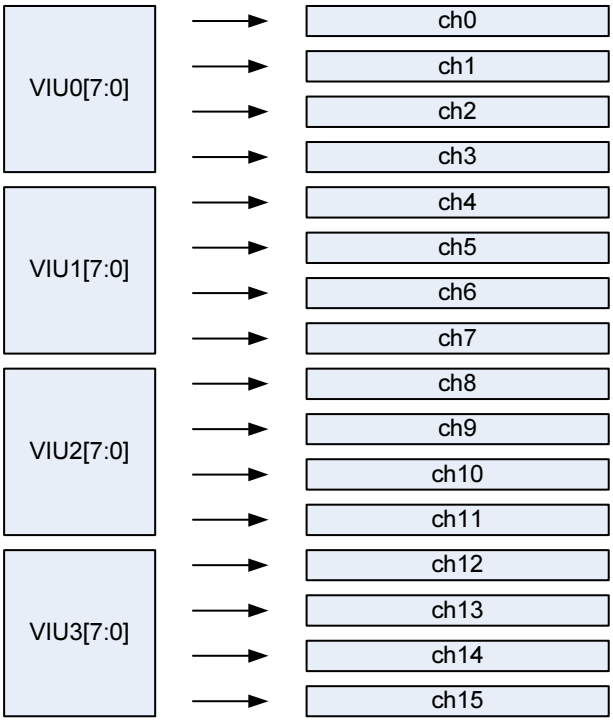
CAUTION

Each 8-bit BT.656 interface (pt0, pt1, pt2, and pt3) has one clock. If two 8-bit interfaces are combined and act as a 16-bit data input, any clock for an 8-bit interface can be used as the clock for the 16-bit interface.

16-Channel D1/960H (Single-Edge Sampling)

Figure 10-2 shows 16-channel D1/960H (single-edge sampling) input application.

Figure 10-2 16-channel D1/960H (single-edge sampling) input application



Each 8-bit pin transfers 4-channel time division multiplexing (TDM) D1/960H (single-edge sampling) data. A total of 32-bit pins are used.

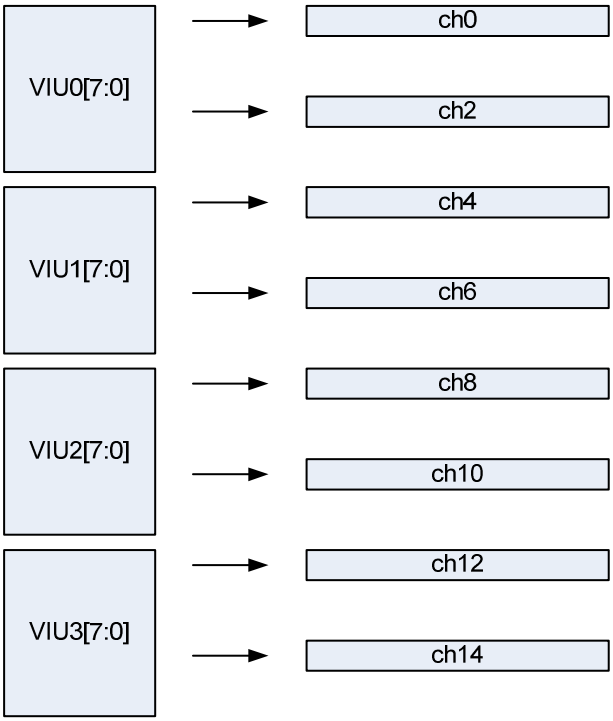
where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- VIU2 indicates the pin corresponding to BT.656 interface 2.
- VIU3 indicates the pin corresponding to BT.656 interface 3.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch15 indicate channel 0 to channel 15 respectively.

8-Channel 720p (Single-Edge Sampling)

Figure 10-3 shows 8-channel 720p (single-edge sampling) input application.

Figure 10-3 8-channel 720p (single-edge sampling) input application



Each 8-bit pin transfers 2-channel 720p (single-edge sampling) data. A total of 32-bit pins are used.

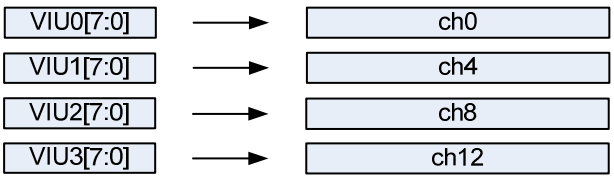
where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- VIU2 indicates the pin corresponding to BT.656 interface 2.
- VIU3 indicates the pin corresponding to BT.656 interface 3.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch7 indicate channel 0 to channel 7 respectively.

4-Channel 1080p (Single-Edge Sampling)

Figure 10-4 shows 4-channel 1080p (single-edge sampling) input application.

Figure 10-4 4-channel 1080p (single-edge sampling) input application



Each 8-bit pin transfers 1-channel 1080p (single-edge sampling) data. A total of 32-bit pins are used.

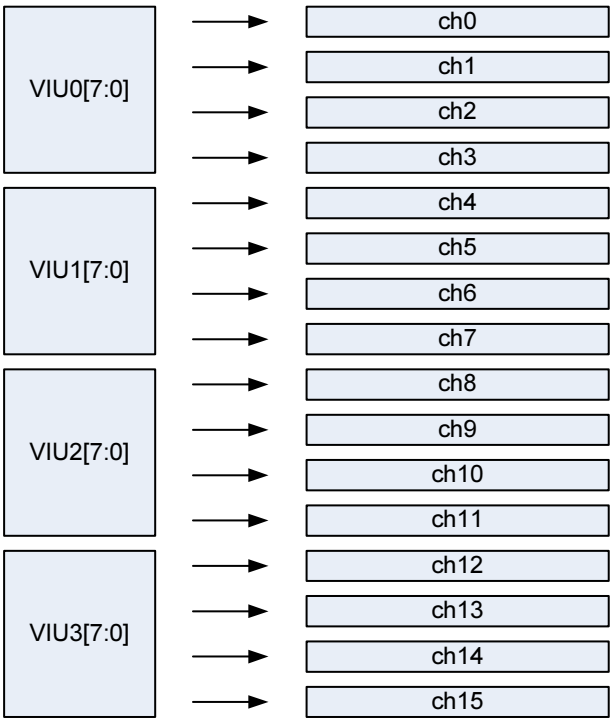
where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- VIU2 indicates the pin corresponding to BT.656 interface 2.
- VIU3 indicates the pin corresponding to BT.656 interface 3.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch7 indicate channel 0 to channel 7 respectively.

16-Channel 720p (Dual-Edge Sampling)

Figure 10-5 shows 16-channel 720p (dual-edge sampling) input application.

Figure 10-5 16-channel 720p (dual-edge sampling) input application



Each 8-bit pin transfers 4-channel TDM 720p (dual-edge sampling) data. A total of 32-bit pins are used.

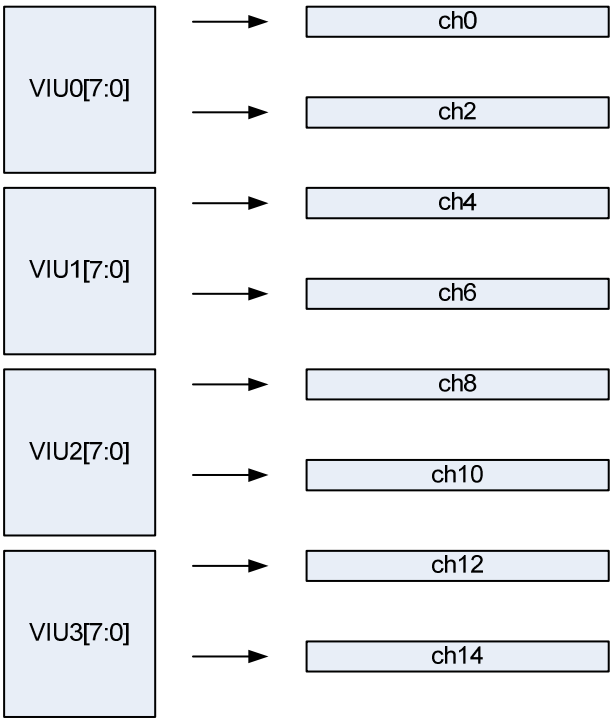
where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- VIU2 indicates the pin corresponding to BT.656 interface 2.
- VIU3 indicates the pin corresponding to BT.656 interface 3.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch15 indicate channel 0 to channel 15 respectively

8-Channel 1080p (Dual-Edge Sampling)

Figure 10-6 shows 8-channel 1080p (dual-edge sampling) input application.

Figure 10-6 8-channel 1080p (dual-edge sampling) input application



Each 8-bit pin transfers 2-channel 1080p (dual-edge sampling) data. A total of 32-bit pins are used.

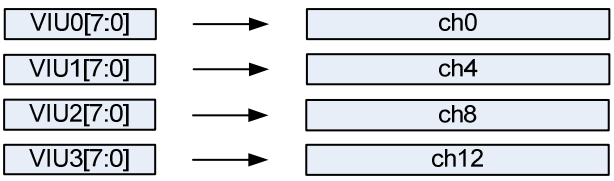
where

- VIU0 indicates the pin corresponding to BT.656interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- VIU2 indicates the pin corresponding to BT.656interface 2.
- VIU3 indicates the pin corresponding to BT.656 interface 3.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch7 indicate channel 0 to channel 7 respectively.

4-Channel 3 Megapixels (Dual-Edge Sampling)

Figure 10-7 shows 4-channel 3 megapixels (dual-edge sampling) input application.

Figure 10-7 4-channel 3 megapixels (dual-edge sampling) input application



Each 8-bit pin transfers 1-channel 3 megapixels (dual-edge sampling) data. A total of 32-bit pins are used.

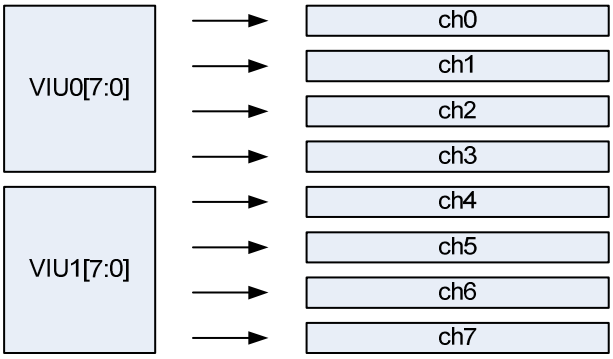
where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- VIU2 indicates the pin corresponding to BT.656 interface 2.
- VIU3 indicates the pin corresponding to BT.656 interface 3.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch7 indicate channel 0 to channel 7 respectively.

8-Channel D1/960H (Single-Edge Sampling)

Figure 10-2 shows 8-channel D1/960H (single-edge sampling) input application.

Figure 10-8 8-channel D1/960H (single-edge sampling) input application



Each 8-bit pin transfers 4-channel time division multiplexing (TDM) D1/960H (single-edge sampling) data. A total of 16-bit pins are used.

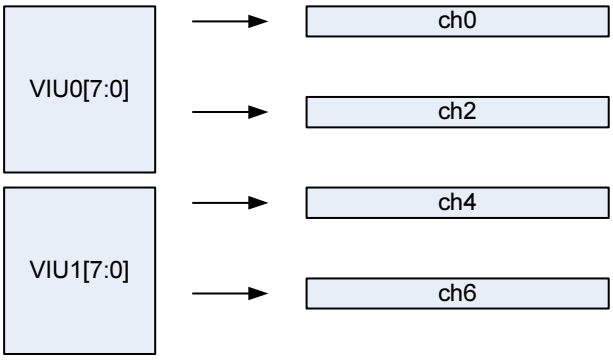
where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch7 indicate channel 0 to channel 7 respectively.

4-Channel 720p (Single-Edge Sampling)

Figure 10-3 shows 4-channel 720p (single-edge sampling) input application.

Figure 10-9 4-channel 720p (single-edge sampling) input application



Each 8-bit pin transfers 2-channel 720p (single-edge sampling) data. A total of 16-bit pins are used.

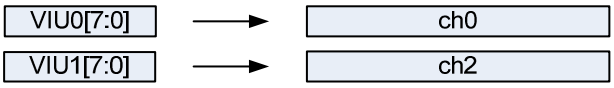
where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch7 indicate channel 0 to channel 7 respectively.

2-Channel 1080p (Single-Edge Sampling)

Figure 10-4 shows 2-channel 1080p (single-edge sampling) input application.

Figure 10-10 2-channel 1080p (single-edge sampling) input application



Each 8-bit pin transfers 1-channel 1080p (single-edge sampling) data. A total of 16-bit pins are used.

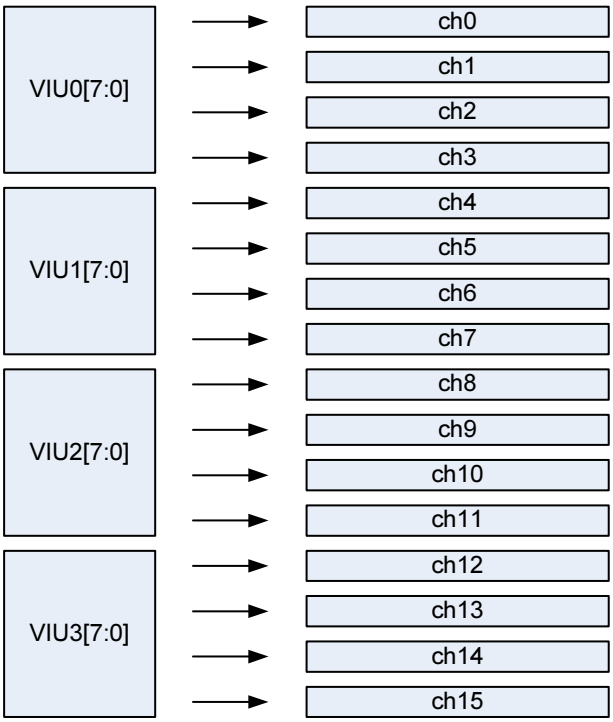
where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch7 indicate channel 0 to channel 7 respectively.

16-Channel 720p (Dual-Edge Sampling)

Figure 10-5 shows 16-channel 720p (dual-edge sampling) input application.

Figure 10-11 16-channel 720p (dual-edge sampling) input application



Each 8-bit pin transfers 4-channel TDM 720p (dual-edge sampling) data. A total of 32-bit pins are used.

where

- VIU0 indicates the pin corresponding to BT.656 interface 0.
- VIU1 indicates the pin corresponding to BT.656 interface 1.
- VIU2 indicates the pin corresponding to BT.656 interface 2.
- VIU3 indicates the pin corresponding to BT.656 interface 3.
- [7:0] indicates bit 7 to bit 0.
- ch0 to ch15 indicate channel 0 to channel 15 respectively

Mixed Timing Input

The interconnected chips are independent of each other, and they can work together in any combination. For example, pt0 supports one HD interleave input, and pt1 supports four D1 inputs.

10.1.3.2 Function Principle

ITU-R BT. 656 YCbCr4:2:2

1. Horizontal timing

Based on the ITU-R BT.656 protocol, sync signals are included in data streams. The special bytes start of active video (SAV) and end of active video (EAV) indicate the start and end of active line data respectively. In video streams, the header of the timing reference code

indicates that the following byte is SAV or EAV. The timing reference code consists of FF 00 00. FF and 00 indicate the reserved bytes of the image encoding data, that is, non-image data. Table 10-1 shows the format of the ITU-R BT.656 line data.

Table 10-1 Format of the ITU-R BT.656 YCbCr 4:2:2 line data

Timing Reference Code				Line Blanking Area					Timing Reference Code				YCbCr 4:2:2 with 720 Valid Pixels						
FF	00	00	EAV	80	10	…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	…	Cr718	Y719

The difference between SAV and EAV depends on the special bit H. Both SAV and EAV include vertical blanking bit V and field indicator bit F. Table 10-2 describes the formats of SAV and EAV.

Table 10-2 Formats of SAV and EAV

Bit7	Bit6 (F)	Bit5 (V)	Bit4 (H)	Bit[3:0] (P3–P0)
Fixed value 1	Field indicator bit 1st field: F = 0 2nd field: F = 1	Vertical blanking bit VBI: V = 1 Active video: V = 0	SAV: H = 0 EAV: H = 1	Check bits

The ITU-R BT.656 protocol defines valid SAV and EAV by using eight valid reserved bits. Four check bits are used to correct 1-bit error and detect 2-bit errors. Table 10-3 describes the valid SAV and EAV values.

Table 10-3 Valid SAV and EAV values

Code	Binary Value	Field Number	Vertical Blanking Interval or Not
SAV	10000000	1	No
EAV	10011101	1	No
SAV	10101011	1	Yes
EAV	10110110	1	Yes
SAV	11000111	2	No
EAV	11011010	2	No
SAV	11101100	2	Yes
EAV	11110001	2	Yes

The four valid reserved bits including P0, P1, P2, and P3 provide the error correction function. They are determined by the F, V, and H bits, as shown in Table 10-4.

Table 10-4 ITU-R BT.656 correction codes

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

NOTE

- P0 = F^V^H
- P1 = F^V
- P2 = F^H
- P3 = V^H

2. Vertical timing

The positions of the vertical timings are determined by bit F and bit V of the timing reference codes SAV and EAV. Figure 10-12 shows the vertical timing of the 525-line 60 field/s video system and Figure 10-13 shows the vertical timing of the 625-line 50 field/s video system.

Figure 10-12 Vertical timing of the 525-line 60 fields/s video system

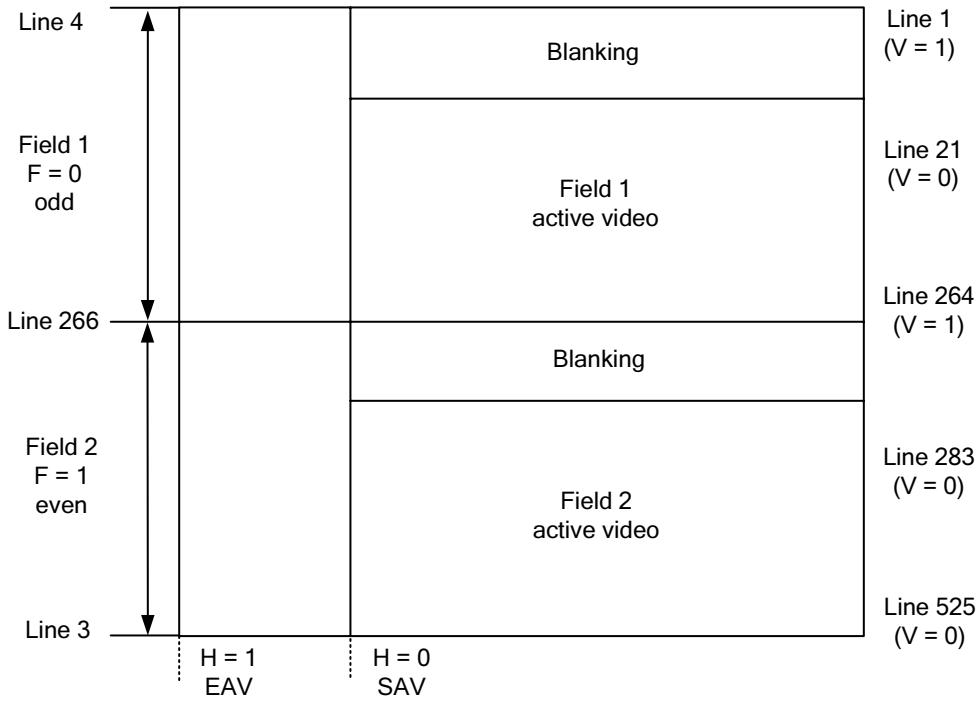
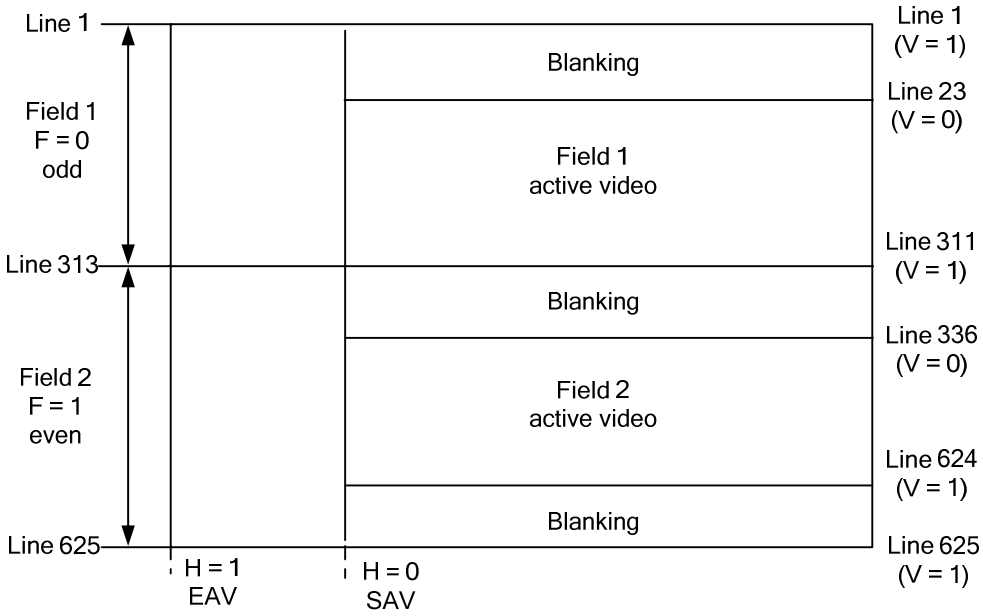


Figure 10-13 Vertical timing of the 625-line 50 fields/s video system

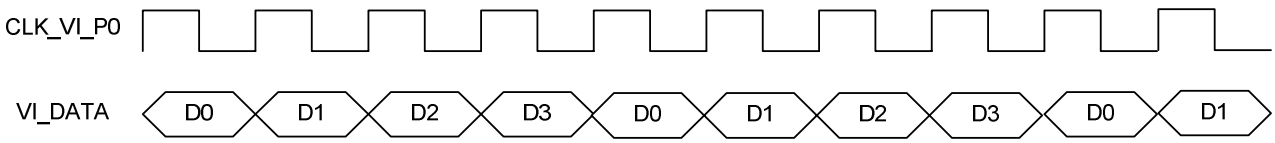


The VICAP module identifies vertical timings based on SAV and EAV regardless of the lines.

Multi-Channel BT.656 (MUX) Timing

The VICAP supports 2-channel and 4-channel BT.656 (mux) timings. The data from multiple channels shares a BT.656 interface in TDM mode. The data from each channel is transferred in the BT.656 timing independently. Figure 10-14 shows the 4-channel BT.656 (mux) timing. D0 to D3 represent the data in BT.656 timing and from four channels.

Figure 10-14 4-channel BT.656 (mux) timing



BT.1120 (HD) Interface Timings

The VICAP module supports the high-definition (HD) interface timings with Y/C separation inputs. In this case, two ports are required. One is used to transfer luminance and the other is used to transfer chrominance, as shown in Figure 10-15 and Figure 10-16.

Figure 10-15 Horizontal input timing of the HD interface

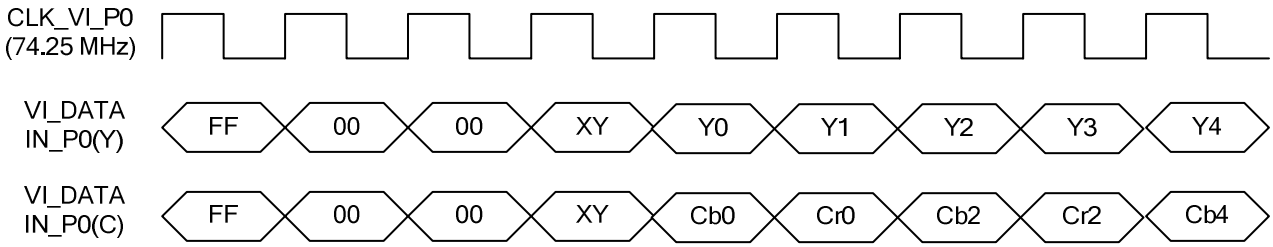
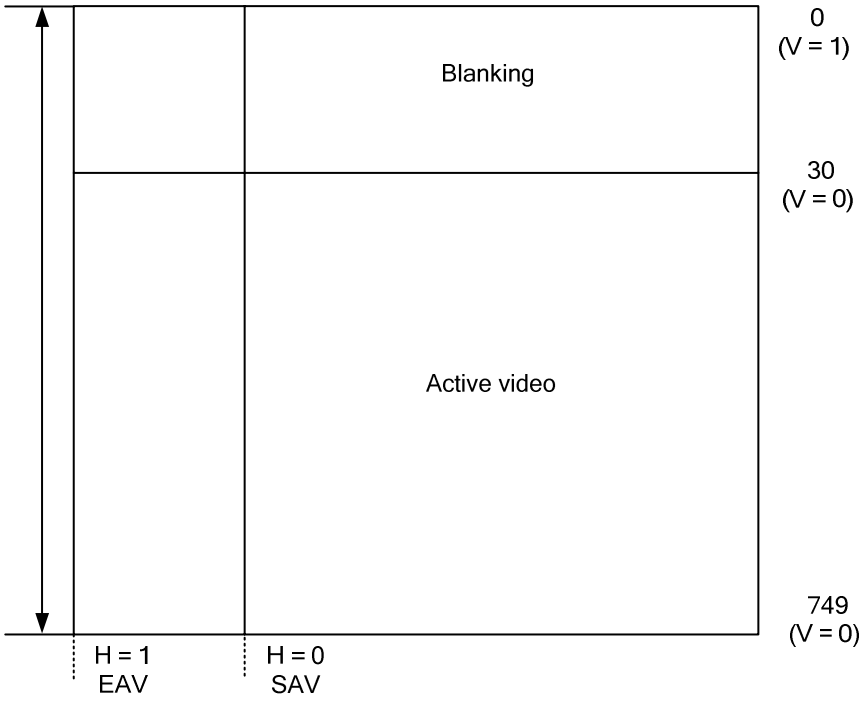


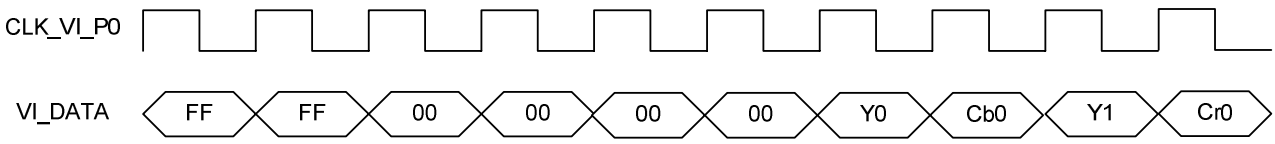
Figure 10-16 Vertical input timing of the HD interface



BT.1120 Y/C (INTERLEAVE) Timing

The VICAP supports the BT.1120 Y/C (interleave) timing, which has the same features as the BT.1120 timing except that the 8-bit interface in TDM mode is used for the BT.1120 Y/C timing, as shown in Figure 10-17.

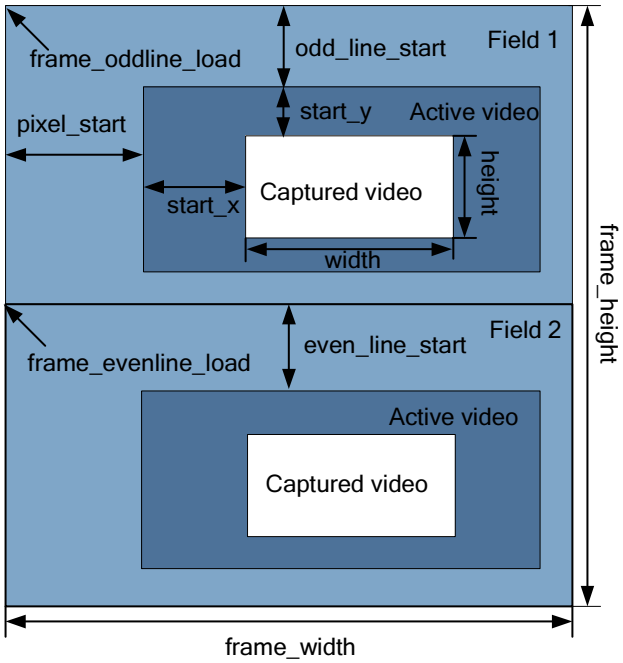
Figure 10-17 BT.1120 Y/C (interleave) timing



10.1.3.3 Picture Cropping

The active video is shown in Figure 10-18, the actual view range, however, is within the active video range. That is, compared with the boundary of the active video, the boundary of the actual view is shrunk, which avoids the boundary effect.

Figure 10-18 Relationships between the active video area and the horizontal/vertical blanking areas



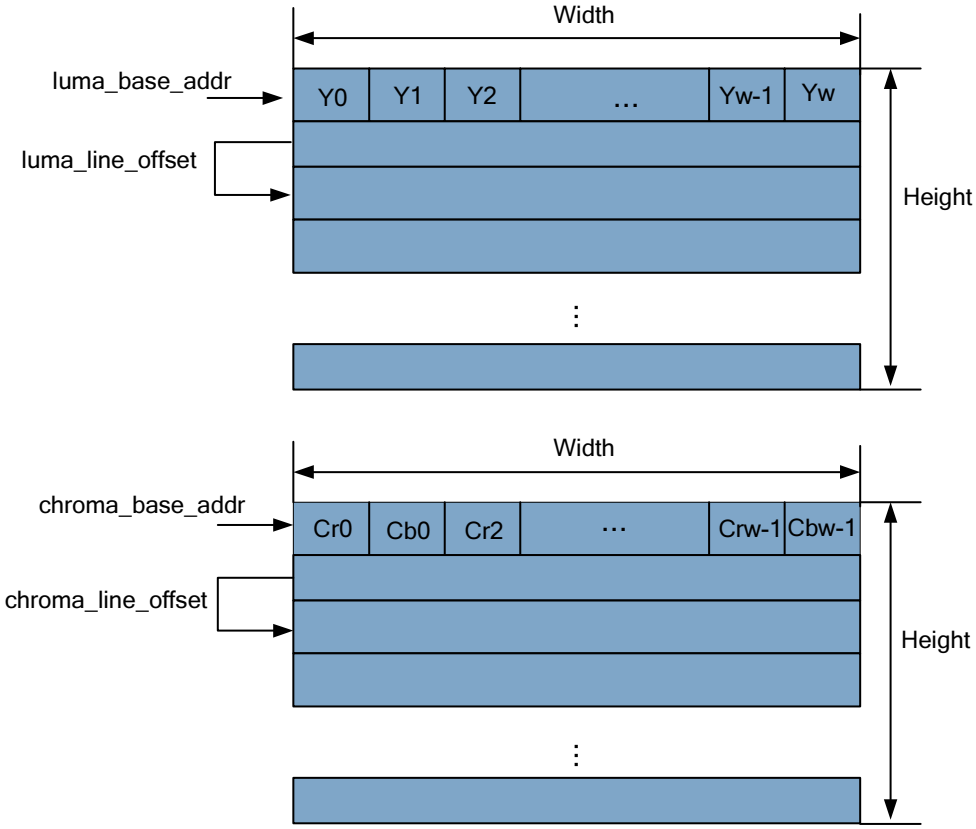
10.1.3.4 Picture Storage Modes

The picture storage modes are as follows:

- Semi-planar YCbCr storage mode

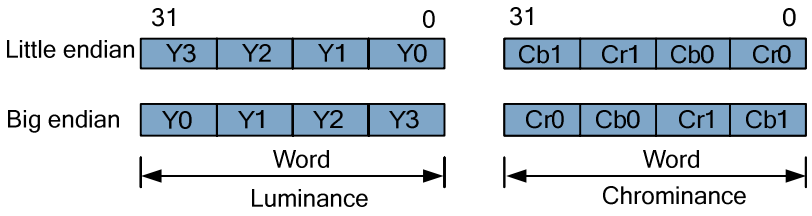
  After setting a view area, the system stores the read data in semi-planar mode. That is, the luminance component and the chrominance component are stored in the luminance space and chrominance space of the DDR respectively.
- For one line, the luminance component and chrominance component are stored separately and consecutively.
- For two consecutive lines, the components are stored based on the offset parameter. This parameter defines the storage stride between the start of two lines. The storage locations in the DDR of the luminance component and chrominance component are specified by the start address base_addr. Figure 10-19 shows the mode of storing the YCbCr4:2:2 data captured by the VICAP module.

Figure 10-19 YCbCr4:2:2 storage mode



In the DDR, data is stored by word (32 bits). Four 8-bit pixels constitute a 32-bit word in big endian mode or little endian mode. Figure 10-20 shows how to store the luminance components and chrominance component in big endian mode and little endian mode.

Figure 10-20 Big endian and little endian storage modes



The VICAP module supports only the DDR that stores data in little endian mode.

10.1.3.5 Mirror and Flip

When the pictures captures by the lens are reversed horizontal and vertically due to the reserve installation of the sensor, you can rectify this problem by using the mirror and flip functions of the VICAP module. The functions are implemented by writing reverse DDR addresses. Note that the start addresses of frames must be 128-bit-aligned.

10.1.4 Operating Mode

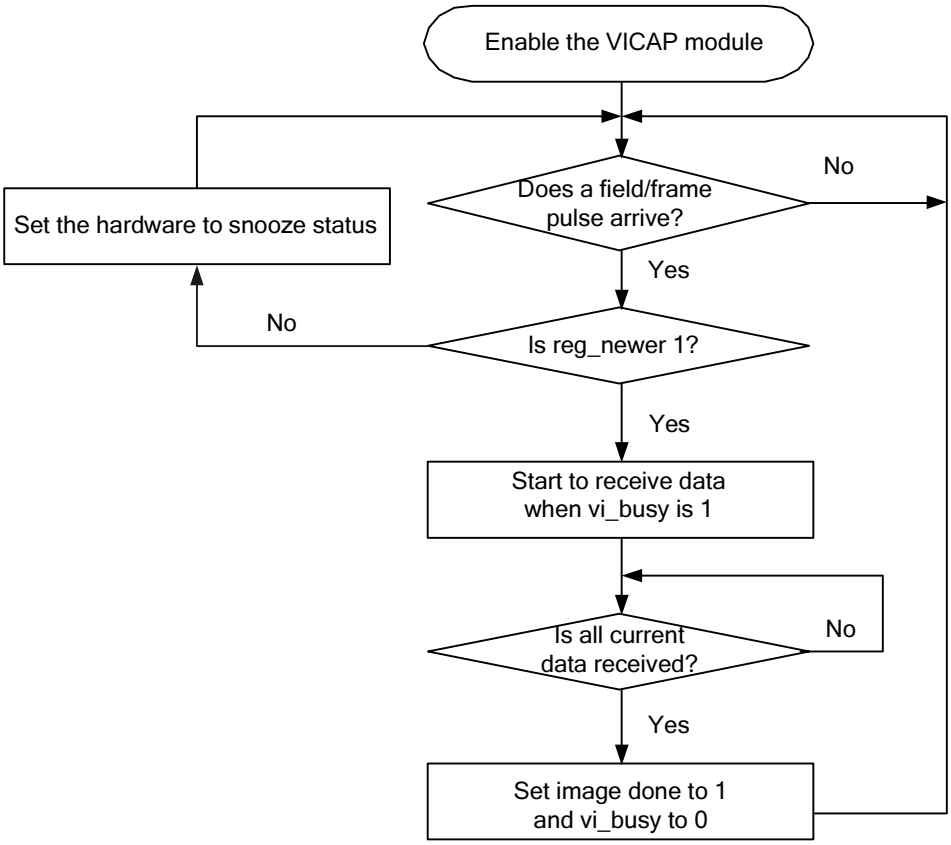
10.1.4.1 reg_newer Function of the VICAP Module

- Before enabling a channel of the VICAP module, the software must perform the following operations:
  - Configure the VICAP attribute register.
  - Write 1 to the reg_newer bit to inform the VICAP module that the current register is ready.
- After the VICAP module is enabled, the VICAP logic starts to work. When a field or a frame arrives:
  - If reg_newer is 0, the VICAP module does not receive data. However, it sets the hardware status to snooze and waits for the next field or frame.
  - If reg_newer is 1, the VICAP module starts to receive data, generates the register update interrupt reg_update_int, and sets the hardware status to busy.
- After all the current data is received, the busy status of the hardware is cleared. When the next field or frame arrives:
  - If reg_newer is 0, the data of the next field or frame is not received.
  - If reg_newer is 1, the data of the next field or frame is received.

10.1.4.2 VICAP Hardware Workflow

Figure 10-21 shows the VICAP hardware workflow.

Figure 10-21 VICAP hardware workflow

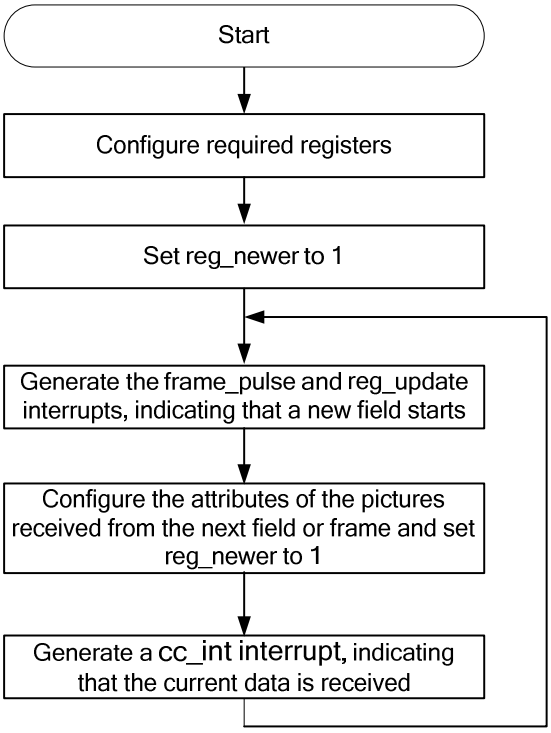


After the data of a specified field or frame is received, the VICAP module checks the reg_newer bit when the next field or frame arrives. If reg_newer is 1, it indicates that software updates or confirms corresponding VICAP registers. In this case, the VICAP module automatically loads the register values configured by the software to the working register (this register is inaccessible to software), clears reg_newer, and starts to receive the data of the next field or frame. If reg_newer is 0, the VICAP module starts to receive data only when reg_newer is 1 and a new field or frame arrives.

10.1.4.3 Software Configuration Workflow

Figure 10-22 shows the software configuration process in interrupt mode.

Figure 10-22 Software configuration workflow



In BT.656 or BT.1120 mode, the timing registers can be ignored.

10.1.5 Register Summary

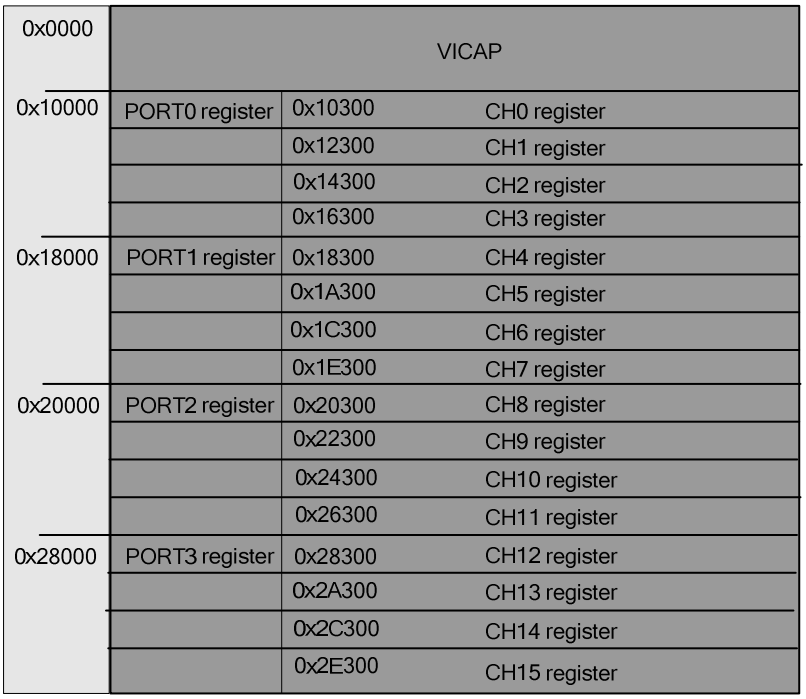
Figure 10-23 shows the space allocation of VICAP registers.

CAUTION

Hi3520D V300 supports at most two external ports, and the registers with the prefix "PT_" in Table 10-5 exist only in channel 0 and channel 4. The register whose offset addresses range from 0x0000 to 0x0200 are system registers.

- Port 0 can be connected to any channel of channel 0–channel 3.
- Port 1 can be connected to any channel of channel 4–channel 7.

Figure 10-23 Space allocation of VICAP registers



NOTE

In Figure 10-23, the addresses starting with 0x0 indicate the offset addresses.

Table 10-5 describes the VICAP registers.

NOTE

The register description in section 10.1.6 "Register Description" is applicable to PORT0 and CH0.

- PORT0 is used as an example to introduce PT-XXX in Table 10-5. PORT1−PORT3 registers and the PORT0 register have the same features except that their offset addresses are different.
- CH0 is used as an example to introduce CH_XXX in Table 10-5. CH1−CH15 registers and the CH0 register have the same features except that their offset addresses are different.

Table 10-5 Summary of the VICAP registers (base address: 0x130C_0000)

Offset Address	Register	Description	Page
0x0000	WK_MODE	Global working configuration register	10-24
0x0010	AXI_CFG	Bus configuration register	10-24
0x0014	MAC_CFG	MAC priority configuration register	10-25
0x0020	CPC_SEL0	Channel port select register 0	10-27
0x0024	CPC_SEL1	Channel port select register 1	10-29
0x0060	CH_RST_REQ	Channel soft reset request register	10-32
0x00E0	APB_TIMEOUT	APB timeout register	10-34

Offset Address	Register	Description	Page
0x00F0	VICAP_INT	Interrupt indicator register	10-34
0x00F8	VICAP_INT_MASK	Interrupt enable register	10-36
0x10000	PT_INTF_MOD	Interface mode register	10-38
0x10010	PT_INTF_OFFSET	Interface offset register	10-39
0x10050	PT_ID_STATUS	Interface ID status register	10-40
0x10300	CH_IPI_INTF_MOD	Interface mode register	10-40
0x10310	CH_IPI_OFFSET0	Component 0 offset register	10-41
0x10314	CH_IPI_OFFSET1	Component 1 offset register	10-42
0x10318	CH_IPI_OFFSET2	Component 2 offset register	10-42
0x10320	CH_IPI_BT656_CFG	BT.656 configuration register	10-43
0x10330	CH_IPI_UNIFY_TIMING_CFG	Timing configuration register	10-44
0x10334	CH_IPI_GEN_TIMING_CFG	Timing recovery module configuration register	10-46
0x10340	CH_IPI_UNIFY_DATA_CFG	Data configuration register	10-47
0x10350	CH_IPI_YUV444_CFG	YUV444 configuration register	10-47
0x10380	CH_IPI_INTF_HFB	Horizontal front blanking region width register	10-48
0x10384	CH_IPI_INTF_HACT	Horizontal valid region width register	10-48
0x10388	CH_IPI_INTF_HBB	Horizontal back blanking region width register	10-49
0x1038C	CH_IPI_INTF_VFB	Vertical front blanking region width register	10-49
0x10390	CH_IPI_INTF_VACT	Vertical valid region width register	10-50
0x10394	CH_IPI_INTF_VBB	Vertical back blanking region width register	10-50
0x10398	CH_IPI_INTF_VBFB	Vertical bottom field front blanking region width register	10-50
0x1039C	CH_IPI_INTF_VBACT	Vertical bottom field valid region width register	10-51
0x103A0	CH_IPI_INTF_VBBB	Vertical bottom field back blanking region width register	10-51
0x103E0	CH_IPI_STATUS	Interface status register	10-51

Offset Address	Register	Description	Page
0x103E4	CH_IPI_BT656_STATUS	BT.656 status register	10-52
0x103EC	CH_IPI_SIZE	Input picture size register	10-52
0x10500	CH_CTRL	Channel control register	10-53
0x10504	CH_REG_NEWER	Capture control register	10-53
0x10520	CH_SUM_Y	Input picture luminance statistics register	10-54
0x10530	CH_COUNT	Channel input picture counter register	10-54
0x10534	CH_DLY_CFG	Channel input picture start interrupt delay configuration register	10-55
0x10580	CH_WCH_Y_CFG	Y component configuration register for the WCH module	10-55
0x10584	CH_WCH_Y_SIZE	Y component storage size register for the WCH module	10-56
0x10590	CH_WCH_Y_FADDR	Y component storage base address register for the WCH module	10-56
0x10598	CH_WCH_Y_STRIDE	Y component line offset register for the WCH module	10-57
0x105A0	CH_WCH_C_CFG	C component configuration register for the WCH module	10-57
0x105A4	CH_WCH_C_SIZE	C component storage size register for the WCH module	10-58
0x105B0	CH_WCH_C_FADDR	C component storage base address register for the WCH module	10-59
0x105B8	CH_WCH_C_STRIDE	C component line offset register for the WCH module	10-59
0x105F0	CH_INT	Channel raw interrupt register	10-60
0x105F8	CH_INT_MASK	Channel interrupt mask register	10-61
0x10700	CH_MSC_CFG	Block mask configuration register	10-63
0x10710	CH_BLOCK0_START	Mask start position register for block 0	10-63
0x10714	CH_BLOCK1_START	Mask start position register for block 1	10-64
0x10718	CH_BLOCK2_START	Mask start position register for block 2	10-64
0x1071C	CH_BLOCK3_START	Mask start position register for block 3	10-65
0x10720	CH_BLOCK0_SIZE	Mask size register for block 0	10-65
0x10724	CH_BLOCK1_SIZE	Mask size register for block 1	10-66

Offset Address	Register	Description	Page
0x10728	CH_BLOCK2_SIZE	Mask size register for block 2	10-66
0x1072C	CH_BLOCK3_SIZE	Mask size register for block 3	10-67
0x10730	CH_BLOCK0_COLOR	Mask color register for block 0	10-67
0x10734	CH_BLOCK1_COLOR	Mask color register for block 1	10-68
0x10738	CH_BLOCK2_COLOR	Mask color register for block 2	10-68
0x1073C	CH_BLOCK3_COLOR	Mask color register for block 3	10-69
0x10800	CH_CROP_CFG	Crop enable register	10-69
0x10810	CH_CROP0_START	Crop start position register for region 0	10-70
0x10814	CH_CROP0_SIZE	Crop size configuration register for region 0	10-70
0x10900	CH_SKIP_Y_CFG	Y component skip configuration register	10-71
0x10910	CH_SKIP_C_CFG	C component skip configuration register	10-71
0x10A00	CH_LHFIR_SPH	Horizontal luminance scaling parameter configuration register	10-72
0x10A04	CH_CHFIR_SPH	Horizontal chrominance scaling parameter configuration register	10-72
0x10A10	CH_LHFIR_IN_SIZE	Horizontal luminance scaling input size configuration register	10-73
0x10A14	CH_CHFIR_IN_SIZE	Horizontal chrominance scaling input size configuration register	10-73
0x10A18	CH_LHFIR_OUT_SIZE	Horizontal luminance scaling output size configuration register	10-74
0x10A1C	CH_CHFIR_OUT_SIZE	Horizontal chrominance scaling output size configuration register	10-74
0x10A30	CH_LHFIR_COEF0	Horizontal luminance scaling coefficient register 0	10-75
0x10A34	CH_LHFIR_COEF1	Horizontal luminance scaling coefficient register 1	10-75
0x10A38	CH_LHFIR_COEF2	Horizontal luminance scaling coefficient register 2	10-76
0x10A40	CH_CHFIR_COEF0	Horizontal chrominance scaling coefficient register 0	10-76
0x10A44	CH_CHFIR_COEF1	Horizontal chrominance scaling coefficient register 1	10-77

Offset Address	Register	Description	Page
0x10A48	CH_CHFIR_COEF2	Horizontal chrominance scaling coefficient register 2	10-77
0x10B00	CH_VCDS_CFG	Vertical chrominance down sampling configuration register for large streams	10-78
0x10B04	CH_VCDS_COEF	Vertical chrominance down sampling coefficient register for large streams	10-78
0x10B08	CH_VCDS_IN_SIZE	Vertical chrominance down sampling input size configuration register	10-79
0x10C00	CH_CLIP_Y_CFG	Luminance clamp configuration register	10-79
0x10C04	CH_CLIP_C_CFG	Chrominance clamp configuration register	10-80

10.1.6 Register Description

WK_MODE

WK_MODE is a global working configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	WK_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								power_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	power_mode	Clock mode 0: The low-power mode is disabled. 1: The low-power mode is enabled.

AXI_CFG

AXI_CFG is a bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	AXI_CFG	0x0010_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								w_outstanding				reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	w_outstanding	Number of write request outstandings Value range: [1, 8]
[3:0]	RO	reserved	Reserved

MAC_CFG

MAC_CFG is a MAC priority configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	MAC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ch15_c_pro	ch15_y_pro	ch14_c_pro	ch14_y_pro	ch13_c_pro	ch13_y_pro	ch12_c_pro	ch12_y_pro	ch11_c_pro	ch11_y_pro	ch10_c_pro	ch10_y_pro	ch9_c_pro	ch9_y_pro	ch8_c_pro	ch8_y_pro	ch7_c_pro	ch7_y_pro	ch6_c_pro	ch6_y_pro	ch5_c_pro	ch5_y_pro	ch4_c_pro	ch4_y_pro	ch3_c_pro	ch3_y_pro	ch2_c_pro	ch2_y_pro	ch1_c_pro	ch1_y_pro	ch0_c_pro	ch0_y_pro
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	ch15_c_pro	Chrominance priority of channel 15. The value 0 indicates the highest priority.
[30]	RW	ch15_y_pro	Luminance priority of channel 15. The value 0 indicates the highest priority.
[29]	RW	ch14_c_pro	Chrominance priority of channel 14. The value 0 indicates the highest priority.
[28]	RW	ch14_y_pro	Luminance priority of channel 14. The value 0 indicates the highest priority.
[27]	RW	ch13_c_pro	Chrominance priority of channel 13. The value 0 indicates the highest priority.
[26]	RW	ch13_y_pro	Luminance priority of channel 13. The value 0 indicates the highest priority.

[25]	RW	ch12_c_pro	Chrominance priority of channel 12. The value 0 indicates the highest priority.
[24]	RW	ch12_y_pro	Luminance priority of channel 12. The value 0 indicates the highest priority.
[23]	RW	ch11_c_pro	Chrominance priority of channel 11. The value 0 indicates the highest priority.
[22]	RW	ch11_y_pro	Luminance priority of channel 11. The value 0 indicates the highest priority.
[21]	RW	ch10_c_pro	Chrominance priority of channel 10. The value 0 indicates the highest priority.
[20]	RW	ch10_y_pro	Luminance priority of channel 10. The value 0 indicates the highest priority.
[19]	RW	ch9_c_pro	Chrominance priority of channel 9. The value 0 indicates the highest priority.
[18]	RW	ch9_y_pro	Luminance priority of channel 9. The value 0 indicates the highest priority.
[17]	RW	ch8_c_pro	Chrominance priority of channel 8. The value 0 indicates the highest priority.
[16]	RW	ch8_y_pro	Luminance priority of channel 8. The value 0 indicates the highest priority.
[15]	RW	ch7_c_pro	Chrominance priority of channel 7. The value 0 indicates the highest priority.
[14]	RW	ch7_y_pro	Luminance priority of channel 7. The value 0 indicates the highest priority.
[13]	RW	ch6_c_pro	Chrominance priority of channel 6. The value 0 indicates the highest priority.
[12]	RW	ch6_y_pro	Luminance priority of channel 6. The value 0 indicates the highest priority.
[11]	RW	ch5_c_pro	Chrominance priority of channel 5. The value 0 indicates the highest priority.
[10]	RW	ch5_y_pro	Luminance priority of channel 5. The value 0 indicates the highest priority.
[9]	RW	ch4_c_pro	Chrominance priority of channel 4. The value 0 indicates the highest priority.
[8]	RW	ch4_y_pro	Luminance priority of channel 4. The value 0 indicates the highest priority.
[7]	RW	ch3_c_pro	Chrominance priority of channel 3. The value 0 indicates the highest priority.
[6]	RW	ch3_y_pro	Luminance priority of channel 3. The value 0 indicates the highest priority.

[5]	RW	ch2_c_pro	Chrominance priority of channel 2. The value 0 indicates the highest priority.
[4]	RW	ch2_y_pro	Luminance priority of channel 2. The value 0 indicates the highest priority.
[3]	RW	ch1_c_pro	Chrominance priority of channel 1. The value 0 indicates the highest priority.
[2]	RW	ch1_y_pro	Luminance priority of channel 1. The value 0 indicates the highest priority.
[1]	RW	ch0_c_pro	Chrominance priority of channel 0. The value 0 indicates the highest priority.
[0]	RW	ch0_y_pro	Luminance priority of channel 0. The value 0 indicates the highest priority.

CPC_SEL0

CPC_SEL0 is channel port select register 0.

Offset Address	Register Name	Total Reset Value
0x0020	CPC_SEL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ch7_sel			reserved	ch6_sel			reserved	ch5_sel			reserved	ch4_sel			reserved	ch3_sel			reserved	ch2_sel			reserved	ch1_sel			reserved	ch0_sel		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	ch7_sel	Channel 7 port select 000: port 0 data with the ID of 0 001: port 0 data with the ID of 1 010: port 0 data with the ID of 2 011: port 0 data with the ID of 3 100: port 1 data with the ID of 0 101: port 1 data with the ID of 1 110: port 1 data with the ID of 2 111: port 1 data with the ID of 3
[27]	RO	reserved	Reserved

[26:24]	RW	ch6_sel	Channel 6 port select 000: port 0 data with the ID of 0 001: port 0 data with the ID of 1 010: port 0 data with the ID of 2 011: port 0 data with the ID of 3 100: port 1 data with the ID of 0 101: port 1 data with the ID of 1 110: port 1 data with the ID of 2 111: port 1 data with the ID of 3
[23]	RO	reserved	Reserved
[22:20]	RW	ch5_sel	Channel 5 port select 000: port 0 data with the ID of 0 001: port 0 data with the ID of 1 010: port 0 data with the ID of 2 011: port 0 data with the ID of 3 100: port 1 data with the ID of 0 101: port 1 data with the ID of 1 110: port 1 data with the ID of 2 111: port 1 data with the ID of 3
[19]	RO	reserved	Reserved
[18:16]	RW	ch4_sel	Channel 4 port select 000: port 0 data with the ID of 0 001: port 0 data with the ID of 1 010: port 0 data with the ID of 2 011: port 0 data with the ID of 3 100: port 1 data with the ID of 0 101: port 1 data with the ID of 1 110: port 1 data with the ID of 2 111: port 1 data with the ID of 3
[15]	RO	reserved	Reserved
[14:12]	RW	ch3_sel	Channel 3 port select 000: port 0 data with the ID of 0 001: port 0 data with the ID of 1 010: port 0 data with the ID of 2 011: port 0 data with the ID of 3 100: port 1 data with the ID of 0 101: port 1 data with the ID of 1 110: port 1 data with the ID of 2 111: port 1 data with the ID of 3

[11]	RO	reserved	Reserved
[10:8]	RW	ch2_sel	Channel 2 port select 000: port 0 data with the ID of 0 001: port 0 data with the ID of 1 010: port 0 data with the ID of 2 011: port 0 data with the ID of 3 100: port 1 data with the ID of 0 101: port 1 data with the ID of 1 110: port 1 data with the ID of 2 111: port 1 data with the ID of 3
[7]	RO	reserved	Reserved
[6:4]	RW	ch1_sel	Channel 1 port select 000: port 0 data with the ID of 0 001: port 0 data with the ID of 1 010: port 0 data with the ID of 2 011: port 0 data with the ID of 3 100: port 1 data with the ID of 0 101: port 1 data with the ID of 1 110: port 1 data with the ID of 2 111: port 1 data with the ID of 3
[3]	RO	reserved	Reserved
[2:0]	RW	ch0_sel	Channel 0 port select 000: port 0 data with the ID of 0 001: port 0 data with the ID of 1 010: port 0 data with the ID of 2 011: port 0 data with the ID of 3 100: port 1 data with the ID of 0 101: port 1 data with the ID of 1 110: port 1 data with the ID of 2 111: port 1 data with the ID of 3

CPC_SEL1

CPC_SEL1 is channel port select register 1.

Offset Address	Register Name	Total Reset Value
0x0024	CPC_SEL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ch15_sel			reserved	ch14_sel			reserved	ch13_sel			reserved	ch12_sel			reserved	ch11_sel			reserved	ch10_sel			reserved	ch9_sel			reserved	ch8_sel		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	ch15_sel	Channel 15 port select 000: port 2 data with the ID of 0 001: port 2 data with the ID of 1 010: port 2 data with the ID of 2 011: port 2 data with the ID of 3 100: port 3 data with the ID of 0 101: port 3 data with the ID of 1 110: port 3 data with the ID of 2 111: port 3 data with the ID of 3
[27]	RO	reserved	Reserved
[26:24]	RW	ch14_sel	Channel 14 port select 000: port 2 data with the ID of 0 001: port 2 data with the ID of 1 010: port 2 data with the ID of 2 011: port 2 data with the ID of 3 100: port 3 data with the ID of 0 101: port 3 data with the ID of 1 110: port 3 data with the ID of 2 111: port 3 data with the ID of 3
[23]	RO	reserved	Reserved
[22:20]	RW	ch13_sel	Channel 13 port select 000: port 2 data with the ID of 0 001: port 2 data with the ID of 1 010: port 2 data with the ID of 2 011: port 2 data with the ID of 3 100: port 3 data with the ID of 0 101: port 3 data with the ID of 1 110: port 3 data with the ID of 2 111: port 3 data with the ID of 3

[19]	RO	reserved	Reserved
[18:16]	RW	ch12_sel	Channel 12 port select 000: port 2 data with the ID of 0 001: port 2 data with the ID of 1 010: port 2 data with the ID of 2 011: port 2 data with the ID of 3 100: port 3 data with the ID of 0 101: port 3 data with the ID of 1 110: port 3 data with the ID of 2 111: port 3 data with the ID of 3
[15]	RO	reserved	Reserved
[14:12]	RW	ch11_sel	Channel 11 port select 000: port 2 data with the ID of 0 001: port 2 data with the ID of 1 010: port 2 data with the ID of 2 011: port 2 data with the ID of 3 100: port 3 data with the ID of 0 101: port 3 data with the ID of 1 110: port 3 data with the ID of 2 111: port 3 data with the ID of 3
[11]	RO	reserved	Reserved
[10:8]	RW	ch10_sel	Channel 10 port select 000: port 2 data with the ID of 0 001: port 2 data with the ID of 1 010: port 2 data with the ID of 2 011: port 2 data with the ID of 3 100: port 3 data with the ID of 0 101: port 3 data with the ID of 1 110: port 3 data with the ID of 2 111: port 3 data with the ID of 3
[7]	RO	reserved	Reserved

[6:4]	RW	ch9_sel	Channel 9 port select 000: port 2 data with the ID of 0 001: port 2 data with the ID of 1 010: port 2 data with the ID of 2 011: port 2 data with the ID of 3 100: port 3 data with the ID of 0 101: port 3 data with the ID of 1 110: port 3 data with the ID of 2 111: port 3 data with the ID of 3
[3]	RO	reserved	Reserved
[2:0]	RW	ch8_sel	Channel 8 port select 000: port 2 data with the ID of 0 001: port 2 data with the ID of 1 010: port 2 data with the ID of 2 011: port 2 data with the ID of 3 100: port 3 data with the ID of 0 101: port 3 data with the ID of 1 110: port 3 data with the ID of 2 111: port 3 data with the ID of 3

CH_RST_REQ

CH_RST_REQ is a channel soft reset request register.

Offset Address	Register Name	Total Reset Value
0x0060	CH_RST_REQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch15_srst_req	ch14_srst_req	ch13_srst_req	ch12_srst_req	ch11_srst_req	ch10_srst_req	ch9_srst_req	ch8_srst_req	ch7_srst_req	ch6_srst_req	ch5_srst_req	ch4_srst_req	ch3_srst_req	ch2_srst_req	ch1_srst_req	ch0_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	ch15_srst_req	Soft reset request of channel 15 0: deassert soft reset 1: enable soft reset

[14]	RW	ch14_srst_req	Soft reset request of channel 14 0: deassert soft reset 1: enable soft reset
[13]	RW	ch13_srst_req	Soft reset request of channel 13 0: deassert soft reset 1: enable soft reset
[12]	RW	ch12_srst_req	Soft reset request of channel 12 0: deassert soft reset 1: enable soft reset
[11]	RW	ch11_srst_req	Soft reset request of channel 11 0: deassert soft reset 1: enable soft reset
[10]	RW	ch10_srst_req	Soft reset request of channel 10 0: deassert soft reset 1: enable soft reset
[9]	RW	ch8_srst_req	Soft reset request of channel 9 0: deassert soft reset 1: enable soft reset
[8]	RW	ch8_srst_req	Soft reset request of channel 8 0: deassert soft reset 1: enable soft reset
[7]	RW	ch7_srst_req	Soft reset request of channel 7 0: deassert soft reset 1: enable soft reset
[6]	RW	ch6_srst_req	Soft reset request of channel 6 0: deassert soft reset 1: enable soft reset
[5]	RW	ch5_srst_req	Soft reset request of channel 5 0: deassert soft reset 1: enable soft reset
[4]	RW	ch4_srst_req	Soft reset request of channel 4 0: deassert soft reset 1: enable soft reset
[3]	RW	ch3_srst_req	Soft reset request of channel 3 0: deassert soft reset 1: enable soft reset

[2]	RW	ch2_srst_req	Soft reset request of channel 2 0: deassert soft reset 1: enable soft reset
[1]	RW	ch1_srst_req	Soft reset request of channel 1 0: deassert soft reset 1: enable soft reset
[0]	RW	ch0_srst_req	Soft reset request of channel 0 0: deassert soft reset 1: enable soft reset

APB_TIMEOUT

APB_TIMEOUT is an APB timeout register.

Offset Address	Register Name	Total Reset Value
0x00E0	APB_TIMEOUT	0x8000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved															timeout															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Timeout enable 0: disabled 1: enabled
[30:16]	RO	reserved	Reserved
[15:0]	RW	timeout	Timeout threshold (in APB clock)

VICAP_INT

VICAP_INT is an interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x00F0	VICAP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ch15	int_ch14	int_ch13	int_ch12	int_ch11	int_ch10	int_ch9	int_ch8	int_ch7	int_ch6	int_ch5	int_ch4	int_ch3	int_ch2	int_ch1	int_ch0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RO	int_ch15	Interrupt indicator of channel 15 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RO	int_ch14	Interrupt indicator of channel 14 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RO	int_ch13	Interrupt indicator of channel 13 0: No interrupt is generated. 1: An interrupt is generated.
[12]	RO	int_ch12	Interrupt indicator of channel 12 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	int_ch11	Interrupt indicator of channel 11 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	int_ch10	Interrupt indicator of channel 10 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	int_ch9	Interrupt indicator of channel 9 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	int_ch8	Interrupt indicator of channel 8 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	int_ch7	Interrupt indicator of channel 7 0: No interrupt is generated. 1: An interrupt is generated.

[6]	RO	int_ch6	Interrupt indicator of channel 6 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	int_ch5	Interrupt indicator of channel 5 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	int_ch4	Interrupt indicator of channel 4 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	int_ch3	Interrupt indicator of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	int_ch2	Interrupt indicator of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_ch1	Interrupt indicator of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_ch0	Interrupt indicator of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

VICAP_INT_MASK

VICAP_INT_MASK is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x00F8	VICAP_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ch15	int_ch14	int_ch13	int_ch12	int_ch11	int_ch10	int_ch9	int_ch8	int_ch7	int_ch6	int_ch5	int_ch4	int_ch3	int_ch2	int_ch1	int_ch0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15]	RW	int_ch15	Channel 15 interrupt enable 0: masked 1: enabled
[14]	RW	int_ch14	Channel 14 interrupt enable 0: masked 1: enabled
[13]	RW	int_ch13	Channel 13 interrupt enable 0: masked 1: enabled
[12]	RW	int_ch12	Channel 12 interrupt enable 0: masked 1: enabled
[11]	RW	int_ch11	Channel 11 interrupt enable 0: masked 1: enabled
[10]	RW	int_ch10	Channel 10 interrupt enable 0: masked 1: enabled
[9]	RW	int_ch9	Channel 9 interrupt enable 0: masked 1: enabled
[8]	RW	int_ch8	Channel 8 interrupt enable 0: masked 1: enabled
[7]	RW	int_ch7	Channel 7 interrupt enable 0: masked 1: enabled
[6]	RW	int_ch6	Channel 6 interrupt enable 0: masked 1: enabled
[5]	RW	int_ch5	Channel 5 interrupt enable 0: masked 1: enabled
[4]	RW	int_ch4	Channel 4 interrupt enable 0: masked 1: enabled

[3]	RW	int_ch3	Channel 3 interrupt enable 0: masked 1: enabled
[2]	RW	int_ch2	Channel 2 interrupt enable 0: masked 1: enabled
[1]	RW	int_ch1	Channel 1 interrupt enable 0: masked 1: enabled
[0]	RW	int_ch0	Channel 0 interrupt enable 0: masked 1: enabled

PT_INTF_MOD

PT_INTF_MOD is an interface mode register.

Offset Address	Register Name	Total Reset Value
0x10000	PT_INTF_MOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved						interleave_seq	ch3_id_en	ch2_id_en	ch1_id_en	ch0_id_en	reserved										port_mux_mode	reserved								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Port register. Four ports are supported. 0x10000−0x100FF: offset addresses of port 0 0x18000−0x180FF: offset addresses of port 1 0x20000−0x200FF: offset addresses of port 2 0x28000−0x280FF: offset addresses of port 3 In the following register description, only the offset addresses of port 0 are provided. The register descriptions of other ports are similar. Port enable 0: disabled 1: enabled

[30:25]	RO	reserved	Reserved
[24]	RW	interleave_seq	Y/C sequence during interleaving 0: The C component is before the Y component. 1: The Y component is before the C component.
[23]	RW	ch3_id_en	Channel 3 ID enable 0: The channel ID is not checked. 1: The data channel is selected based on the channel ID.
[22]	RW	ch2_id_en	Channel 2 ID enable 0: The channel ID is not checked. 1: The data channel is selected based on the channel ID.
[21]	RW	ch1_id_en	Channel 1 ID enable 0: The channel ID is not checked. 1: The data channel is selected based on the channel ID.
[20]	RW	ch0_id_en	Channel 0 ID enable 0: The channel ID is not checked. 1: The data channel is selected based on the channel ID.
[19:10]	RW	reserved	Reserved
[9:8]	RW	port_mux_mode	Multiplexed timing mode 0: non-multiplexed mode 1: 2-channel BT.656 multiplexed mode 2: 4-channel BT.656 multiplexed mode 3: BT.1120 Y/C interleaved mode
[7:0]	RO	reserved	Reserved

PT_INTF_OFFSET

PT_INTF_OFFSET is an interface offset register.

Offset Address	Register Name	Total Reset Value
0x10010	PT_INTF_OFFSET	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 0 mask

[15]	RW	rev	Whether the data line is reversed 0: The data line is not reversed. 1: The data line is reversed.
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 0 offset

PT_ID_STATUS

PT_ID_STATUS is an interface ID status register.

Offset Address	Register Name	Total Reset Value
0x10050	PT_ID_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												id3	id2	id1	id0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	id3	Data with the ID of 3 is detected in channel 3.
[2]	RO	id2	Data with the ID of 2 is detected in channel 2.
[1]	RO	id1	Data with the ID of 1 is detected in channel 1.
[0]	RO	id0	Data with the ID of 0 is detected in channel 0.

CH_IPI_INTF_MOD

CH_IPI_INTF_MOD is an interface mode register.

Offset Address	Register Name	Total Reset Value
0x10300	CH_IPI_INTF_MOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Channel. A maximum of 16 channels are supported. 0x10300−0x113FF: offset addresses of channel 0 0x12300−0x133FF: offset addresses of channel 1 0x14300−0x153FF: offset addresses of channel 2 0x16300−0x173FF: offset addresses of channel 3 0x18300−0x193FF: offset addresses of channel 4 0x1A300−0x1B3FF: offset addresses of channel 5 0x1C300−0x1D3FF: offset addresses of channel 6 0x1E300−0x1F3FF: offset addresses of channel 7 0x20300−0x213FF: offset addresses of channel 8 0x22300−0x233FF: offset addresses of channel 9 0x24300−0x253FF: offset addresses of channel 10 0x26300−0x273FF: offset addresses of channel 11 0x28300−0x293FF: offset addresses of channel 12 0x2a300−0x2b3FF: offset addresses of channel 13 0x2c300−0x2d3FF: offset addresses of channel 14 0x2e300−0x2f3FF: offset addresses of channel 15 Port enable 0: disabled 1: enabled
[30:1]	RO	reserved	Reserved
[0]	RW	mode	Timing mode 0: external synchronous mode 1: BT656 timing mode

CH_IPI_OFFSET0

CH_IPI_OFFSET0 is a component 0 offset register.

Offset Address	Register Name	Total Reset Value
0x10310	CH_IPI_OFFSET0	0xFF00_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 0 mask
[15]	RW	rev	Whether the data line is reversed 0: The data line is not reversed. 1: The data line is reversed.
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 0 offset

CH_IPI_OFFSET1

CH_IPI_OFFSET1 is a component 1 offset register.

Offset Address	Register Name	Total Reset Value
0x10314	CH_IPI_OFFSET1	0xFF00_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 1 mask
[15]	RW	rev	Whether the data line is reversed 0: The data line is not reversed. 1: The data line is reversed.
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 1 offset

CH_IPI_OFFSET2

CH_IPI_OFFSET2 is a component 2 offset register.

Offset Address	Register Name	Total Reset Value
0x10318	CH_IPI_OFFSET2	0xFF00_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 2 mask
[15]	RW	rev	Whether the data line is reversed 0: The data line is not reversed. 1: The data line is reversed.
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 2 offset

CH_IPI_BT656_CFG

CH_IPI_BT656_CFG is a BT.656 configuration register.

Offset Address	Register Name	Total Reset Value
0x10320	CH_IPI_BT656_CFG	0x0000_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																				field_inv	vsync_inv	hsync_inv	reserved				mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31]	RW	enable	BT.656 enable 0: disabled 1: enabled
[30:11]	RO	reserved	Reserved
[10]	RW	field_inv	Reverse control 0: not reversed 1: reversed
[9]	RW	vsync_inv	vsync reverse control 0: not reversed 1: reversed

[8]	RW	hsync_inv	hsync reverse control 0: not reversed 1: reversed
[7:4]	RO	reserved	Reserved
[3:0]	RW	mode	Mode select mode[0] 0: hsync is not an active signal. 1: hsync is an active signal. mode[1] 0: The hsync output is active low. 1: The hsync output is active high. mode[3:2] 00: Component 0 is parsed. 01: Component 1 is parsed. 10: Component 2 is parsed. 11: reserved

CH_IPI_UNIFY_TIMING_CFG

CH_IPI_UNIFY_TIMING_CFG is a timing configuration register.

Offset Address	Register Name	Total Reset Value
0x10330	CH_IPI_UNIFY_TIMING_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					field_inv	field_sel		reserved				vsync_mode		vsync_inv	vsync_sel	reserved		hsync_mode		hsync_and		hsync_inv	hsync_sel	reserved					de_inv	de_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RW	field_inv	Field reverse (level-1 field processing) 0: not reversed 1: reversed

[25:24]	RW	field_sel	Field source select (level-0 field processing) 00: input field 01: input vsync 10: detected based on the relationship between vsync and hsync 11: fixed at 0
[23:21]	RO	reserved	Reserved
[20:19]	RW	vsync_mode	Vsync processing mode (level-2 vsync processing) 00: not processed 01: detect the rising edge 10: detect the rising edge and falling edge 11: reserved
[18]	RW	vsync_inv	vsync reverse (level-1 vsync processing) 0: not reversed 1: reversed
[17:16]	RW	vsync_sel	vsync source select (level-0 vsync processing) 00: input vsync 01: input field 10: fixed at 0 11: reserved
[15]	RO	reserved	Reserved
[14:13]	RW	hsync_mode	hsync processing mode (level-3 hsync processing) 0: not processed 1: detect the rising edge
[12:11]	RW	hsync_and	Whether hsync is operated with the result of level-1 vsync processing (level-2 hsync processing) 00: not processed 01: ANDed 10: exclusive ORed 11: reserved
[10]	RW	hsync_inv	hsync reverse (level-1 hsync processing) 0: not reversed 1: reversed
[9:8]	RW	hsync_sel	hsync source select (level-1 hsync processing) 00: input hsync 01: input de 10: fixed at 0 11: reserved
[7:3]	RO	reserved	Reserved

[2]	RW	de_inv	de reverse (level-1 de processing) 0: not reversed 1: reversed
[1:0]	RW	de_sel	de source select (level-0 de processing) 00: input de 01: result of level-2 hsync processing 10: fixed at 1 11: fixed at 0

CH_IPI_GEN_TIMING_CFG

CH_IPI_GEN_TIMING_CFG is a timing recovery module configuration register.

Offset Address	Register Name	Total Reset Value
0x10334	CH_IPI_GEN_TIMING_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	mode	reserved																											vsync_mode	hsync_mode	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Timing recovery enable (timings are recovered based on timing parameters) 0: disabled 1: enabled
[30]	RW	mode	Timing recovery mode (timings are recovered based on timing parameters) 0: Timings are generated based on the input valid signal of PT. 1: Timings are automatically calculated and generated internally.
[29:3]	RO	reserved	Reserved
[2]	RW	vsync_mode	vsync recovery 0: not recovered 1: recovered
[1]	RW	hsync_mode	hsync recovery 0: not recovered 1: recovered
[0]	RO	reserved	Reserved

CH_IPI_UNIFY_DATA_CFG

CH_IPI_UNIFY_DATA_CFG is a data configuration register.

Offset Address	Register Name	Total Reset Value
0x10340	CH_IPI_UNIFY_DATA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																											uv_seq	yc_seq	comp_num		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Data separation enable 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved
[3]	RW	uv_seq	Cb/Cr sequence 0: CbCr 1: CrCb
[2]	RW	yc_seq	Y/C sequence 0: CY 1: YC
[1:0]	RW	comp_num	Data component select 00: component 1 01: component 2 10: component 3 11: reserved

CH_IPI_YUV444_CFG

CH_IPI_YUV444_CFG is a YUV444 configuration register.

Offset Address	Register Name	Total Reset Value
0x10350	CH_IPI_YUV444_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	YUV enable for converting YUV422 signals into YUV444 signals 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

CH_IPI_INTF_HFB

CH_IPI_INTF_HFB is a horizontal front blanking region width register.

Offset Address	Register Name	Total Reset Value
0x10380	CH_IPI_INTF_HFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hfb	Horizontal front blanking region width

CH_IPI_INTF_HACT

CH_IPI_INTF_HACT is a horizontal valid region width register.

Offset Address	Register Name	Total Reset Value
0x10384	CH_IPI_INTF_HACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hact																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hact	Horizontal valid region width (in clock cycle)

CH_IPI_INTF_HBB

CH_IPI_INTF_HBB is a horizontal back blanking region width register.

Offset Address	Register Name	Total Reset Value
0x10388	CH_IPI_INTF_HBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hbb	Horizontal back blanking region width

CH_IPI_INTF_VFB

CH_IPI_INTF_VFB is a vertical front blanking region width register.

Offset Address	Register Name	Total Reset Value
0x1038C	CH_IPI_INTF_VFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vfb	Vertical front blanking region width

CH_IPI_INTF_VACT

CH_IPI_INTF_VACT is a vertical valid region width register.

Offset Address	Register Name	Total Reset Value
0x10390	CH_IPI_INTF_VACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vact	Vertical valid region width

CH_IPI_INTF_VBB

CH_IPI_INTF_VBB is a vertical back blanking region width register.

Offset Address	Register Name	Total Reset Value
0x10394	CH_IPI_INTF_VBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbb	Vertical back blanking region width

CH_IPI_INTF_VBFB

CH_IPI_INTF_VBFB is a vertical bottom field front blanking region width register.

Offset Address	Register Name	Total Reset Value
0x10398	CH_IPI_INTF_VBFB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	vbfb	Vertical bottom field front blanking region width

CH_IPI_INTF_VBACT

CH_IPI_INTF_VBACT is a vertical bottom field valid region width register.

Offset Address	Register Name	Total Reset Value
0x1039C	CH_IPI_INTF_VBACT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbact	Vertical bottom field valid region width

CH_IPI_INTF_VBBB

CH_IPI_INTF_VBBB is a vertical bottom field back blanking region width register.

Offset Address	Register Name	Total Reset Value
0x103A0	CH_IPI_INTF_VBBB	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbbb	Vertical bottom field back blanking region width

CH_IPI_STATUS

CH_IPI_STATUS is an interface status register.

Offset Address	Register Name	Total Reset Value
0x103E0	CH_IPI_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										id		field	vysnc	hsync	de
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RO	id	Port output ID
[3]	RO	field	Field output over the port
[2]	RO	vysnc	vysnc signal output over the port
[1]	RO	hsync	hsync signal output over the port
[0]	RO	de	de signal output over the port

CH_IPI_BT656_STATUS

CH_IPI_BT656_STATUS is a BT.656 status register.

Offset Address	Register Name	Total Reset Value
0x103E4	CH_IPI_BT656_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																seav								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RO	seav	Synchronization code
[7:0]	RO	reserved	Reserved

CH_IPI_SIZE

CH_IPI_SIZE is an input picture size register.

Offset Address	Register Name	Total Reset Value
0x103EC	CH_IPI_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Picture height
[15:0]	RO	width	Picture width

CH_CTRL

CH_CTRL is a channel control register.

Offset Address	Register Name	Total Reset Value
0x10500	CH_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Channel enable 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

CH_REG_NEWER

CH_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x10504	CH_REG_NEWER	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							reg_newer
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	reg_newer	Channel update. This bit is automatically cleared for each frame.

CH_SUM_Y

CH_SUM_Y is an input picture luminance statistics register.

Offset Address	Register Name	Total Reset Value
0x10520	CH_SUM_Y	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	sum_y							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	sum_y	Luminance statistics

CH_COUNT

CH_COUNT is a channel input picture counter register.

Offset Address	Register Name	Total Reset Value
0x10530	CH_COUNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	v_count				reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	v_count	Counter for the number of vertical lines.This bit is automatically cleared for each frame.

[15:0]	RO	reserved	Reserved

CH_DLY_CFG

CH_DLY_CFG is a channel input picture start interrupt delay configuration register.

Offset Address	Register Name	Total Reset Value
0x10534	CH_DLY_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_dly_cfg																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	v_dly_cfg	Vertical line number delay
[15:0]	RO	reserved	Reserved

CH_WCH_Y_CFG

CH_WCH_Y_CFG is a Y component configuration register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10580	CH_WCH_Y_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved											interleave	bfield	reserved		reserved								flip	mirror	reserved					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	CH write channel enable 0: disabled 1: enabled
[30:20]	RO	reserved	Reserved
[19]	RW	interleave	Progressive/Interlaced flag 0: The output data is progressive or interlaced and does not need to be interleaved as frames for storage. 1: The output data is interlaced and needs to be interleaved as frames for storage.

[18]	RW	bfield	Top/Bottom field flag. This field is used when the output data is interlaced and needs to be interleaved as frames for storage. 0: top field 1: bottom field
[17:16]	RO	reserved	Reserved
[15:5]	RO	reserved	Reserved
[4]	RW	flip	Channel flip enable 0: disabled 1: enabled
[3]	RW	mirror	Channel mirror enable 0: disabled 1: enabled
[2:0]	RW	reserved	Reserved

CH_WCH_Y_SIZE

CH_WCH_Y_SIZE is a Y component storage size register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10584	CH_WCH_Y_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the stored picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the stored picture. The configured value is the actual value minus 1.

CH_WCH_Y_FADDR

CH_WCH_Y_FADDR is a Y component storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10590	CH_WCH_Y_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the Y component

CH_WCH_Y_STRIDE

CH_WCH_Y_STRIDE is a Y component line offset register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10598	CH_WCH_Y_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Stride (in byte) for storing the Y component

CH_WCH_C_CFG

CH_WCH_C_CFG is a C component configuration register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x105A0	CH_WCH_C_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved											interleave	bfield	reserved		reserved											flip	mirror	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	CH write channel enable 0: disabled 1: enabled
[30:20]	RO	reserved	Reserved
[19]	RW	interleave	Progressive/Interlaced flag 0: The output data is progressive or interlaced and does not need to be interleaved as frames for storage. 1: The output data is interlaced and needs to be interleaved as frames for storage.
[18]	RW	bfield	Top/Bottom field flag. This field is used when the output data is interlaced and needs to be interleaved as frames for storage. 0: top field 1: bottom field
[17:16]	RO	reserved	Reserved
[15:5]	RO	reserved	Reserved
[4]	RW	flip	Channel flip enable 0: disabled 1: enabled
[3]	RW	mirror	Channel mirror enable 0: disabled 1: enabled
[2:0]	RW	reserved	Reserved

CH_WCH_C_SIZE

CH_WCH_C_SIZE is a C component storage size register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x105A4	CH_WCH_C_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the stored picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the stored picture. The configured value is the actual value minus 1.

CH_WCH_C_FADDR

CH_WCH_C_FADDR is a C component storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x105B0	CH_WCH_C_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the C component

CH_WCH_C_STRIDE

CH_WCH_C_STRIDE is a C component line offset register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x105B8	CH_WCH_C_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Stride (in byte) for storing the C component

CH_INT

CH_INT is a channel raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x105F0	CH_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fstart_dly	reserved							timer_out	height_err	width_err	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	WC	fstart_dly	Status of the delayed field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[14:8]	RO	reserved	Reserved
[7]	WC	timer_out	Status of the timing loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[6]	WC	height_err	Status of the picture height change interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

[5]	WC	width_err	Status of the picture width change interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	update_cfg	Status of the register updated interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the field/frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the field/frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

CH_INT_MASK

CH_INT_MASK is a channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x105F8	CH_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fstart_dly	reserved							timer_out	height_err	width_err	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	fstart_dly	Delayed field/frame start interrupt enable 0: masked 1: enabled
[14:8]	RO	reserved	Reserved
[7]	WC	timer_out	Timing loss interrupt status enable 0: masked 1: enabled
[6]	RW	height_err	Picture height change interrupt status enable 0: masked 1: enabled
[5]	RW	width_err	Picture width change interrupt status enable 0: masked 1: enabled
[4]	RW	update_cfg	Register update interrupt enable 0: masked 1: enabled
[3]	RW	field_throw	Field/Frame loss interrupt enable 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable 0: masked 1: enabled

[0]	RW	fstart	Field/Frame start interrupt enable 0: masked 1: enabled

CH_MSC_CFG

CH_MSC_CFG is a block mask configuration register.

Offset Address	Register Name	Total Reset Value
0x10700	CH_MSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												msc3_en	msc2_en	msc1_en	msc0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	msc3_en	Block 3 enable 0: disabled 1: enabled
[2]	RW	msc2_en	Block 2 enable 0: disabled 1: enabled
[1]	RW	msc1_en	Block 1 enable 0: disabled 1: enabled
[0]	RW	msc0_en	Block 0 enable 0: disabled 1: enabled

CH_BLOCK0_START

CH_BLOCK0_START is a mask start position register for block 0.

Offset Address	Register Name	Total Reset Value
0x10710	CH_BLOCK0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	y_start	Vertical start point of block 0
[15:12]	RO	reserved	Reserved
[11:0]	RW	x_start	Horizontal start point of block 0

CH_BLOCK1_START

CH_BLOCK1_START is a mask start position register for block 1.

Offset Address	Register Name	Total Reset Value
0x10714	CH_BLOCK1_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	y_start	Vertical start point of block 1
[15:12]	RO	reserved	Reserved
[11:0]	RW	x_start	Horizontal start point of block 1

CH_BLOCK2_START

CH_BLOCK2_START is a mask start position register for block 2.

Offset Address	Register Name	Total Reset Value
0x10718	CH_BLOCK2_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	y_start	Vertical start point of block 2
[15:12]	RO	reserved	Reserved
[11:0]	RW	x_start	Horizontal start point of block 2

CH_BLOCK3_START

CH_BLOCK3_START is a mask start position register for block 3.

Offset Address	Register Name	Total Reset Value
0x1071C	CH_BLOCK3_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	y_start	Vertical start point of block 3
[15:12]	RO	reserved	Reserved
[11:0]	RW	x_start	Horizontal start point of block 3

CH_BLOCK0_SIZE

CH_BLOCK0_SIZE is a mask size register for block 0.

Offset Address	Register Name	Total Reset Value
0x10720	CH_BLOCK0_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	blk_height			reserved	blk_width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	blk_height	Vertical height of block 0 minus 1
[15:12]	RO	reserved	Reserved
[11:0]	RW	blk_width	Horizontal width of block 0 minus 1

CH_BLOCK1_SIZE

CH_BLOCK1_SIZE is a mask size register for block 1.

Offset Address	Register Name	Total Reset Value
0x10724	CH_BLOCK1_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	blk_height			reserved	blk_width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	blk_height	Vertical height of block 1 minus 1
[15:12]	RO	reserved	Reserved
[11:0]	RW	blk_width	Horizontal width of block 1 minus 1

CH_BLOCK2_SIZE

CH_BLOCK2_SIZE is a mask size register for block 2.

Offset Address	Register Name	Total Reset Value
0x10728	CH_BLOCK2_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	blk_height			reserved	blk_width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	blk_height	Vertical height of block 2 minus 1
[15:12]	RO	reserved	Reserved
[11:0]	RW	blk_width	Horizontal width of block 2 minus 1

CH_BLOCK3_SIZE

CH_BLOCK3_SIZE is a mask size register for block 3.

Offset Address	Register Name	Total Reset Value
0x1072C	CH_BLOCK3_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	blk_height			reserved	blk_width		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	blk_height	Vertical height of block 3 minus 1
[15:12]	RO	reserved	Reserved
[11:0]	RW	blk_width	Horizontal width of block 3 minus 1

CH_BLOCK0_COLOR

CH_BLOCK0_COLOR is a mask color register for block 0.

Offset Address	Register Name	Total Reset Value
0x10730	CH_BLOCK0_COLOR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		blk_cr		blk_cb		blk_y	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	blk_cr	Cr component of the filling color for block 0
[15:8]	RW	blk_cb	Cb component of the filling color for block 0
[7:0]	RW	blk_y	Y component of the filling color for block 0

CH_BLOCK1_COLOR

CH_BLOCK1_COLOR is a mask color register for block 1.

Offset Address	Register Name	Total Reset Value
0x10734	CH_BLOCK1_COLOR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		blk_cr		blk_cb		blk_y	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	blk_cr	Cr component of the filling color for block 1
[15:8]	RW	blk_cb	Cb component of the filling color for block 1
[7:0]	RW	blk_y	Y component of the filling color for block 1

CH_BLOCK2_COLOR

CH_BLOCK2_COLOR is a mask color register for block 2.

Offset Address	Register Name	Total Reset Value
0x10738	CH_BLOCK2_COLOR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		blk_cr		blk_cb		blk_y	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	blk_cr	Cr component of the filling color for block 2
[15:8]	RW	blk_cb	Cb component of the filling color for block 2
[7:0]	RW	blk_y	Y component of the filling color for block 2

CH_BLOCK3_COLOR

CH_BLOCK3_COLOR is a mask color register for block 3.

Offset Address	Register Name	Total Reset Value
0x1073C	CH_BLOCK3_COLOR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		blk_cr		blk_cb		blk_y	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	blk_cr	Cr component of the filling color for block 3
[15:8]	RW	blk_cb	Cb component of the filling color for block 3
[7:0]	RW	blk_y	Y component of the filling color for block 3

CH_CROP_CFG

CH_CROP_CFG is a crop enable register.

Offset Address	Register Name	Total Reset Value
0x10800	CH_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	Enable for crop region 0 0: disabled 1: enabled

CH_CROP0_START

CH_CROP0_START is a crop start position register for region 0.

Offset Address	Register Name	Total Reset Value
0x10810	CH_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which the picture starts to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which the picture starts to be captured

CH_CROP0_SIZE

CH_CROP0_SIZE is a crop size configuration register for region 0.

Offset Address	Register Name	Total Reset Value
0x10814	CH_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained picture. The configured value is the actual value minus 1.

CH_SKIP_Y_CFG

CH_SKIP_Y_CFG is a Y component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x10900	CH_SKIP_Y_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration of the Y component

CH_SKIP_C_CFG

CH_SKIP_C_CFG is a C component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x10910	CH_SKIP_C_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration of the C component

CH_LHFIR_SPH

CH_LHFIR_SPH is a horizontal luminance scaling parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x10A00	CH_LHFIR_SPH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hlmsc_en	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hlmsc_en	Horizontal luminance scaling enable 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

CH_CHFIR_SPH

CH_CHFIR_SPH is a horizontal chrominance scaling parameter configuration register.

Offset Address	Register Name	Total Reset Value
0x10A04	CH_CHFIR_SPH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hchmsc_en	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hchmsc_en	Horizontal chrominance scaling enable 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

CH_LHFIR_IN_SIZE

CH_LHFIR_IN_SIZE is a horizontal luminance scaling input size configuration register.

Offset Address	Register Name	Total Reset Value
0x10A10	CH_LHFIR_IN_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width (in pixel). The configured value is the actual value minus 1.

CH_CHFIR_IN_SIZE

CH_CHFIR_IN_SIZE is a horizontal chrominance scaling input size configuration register.

Offset Address	Register Name	Total Reset Value
0x10A14	CH_CHFIR_IN_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width (in pixel). The configured value is the actual value minus 1. The picture width is set to the sum of the widths of the Cb and Cr chrominance components.

CH_LHFIR_OUT_SIZE

CH_LHFIR_OUT_SIZE is a horizontal luminance scaling output size configuration register.

Offset Address	Register Name	Total Reset Value
0x10A18	CH_LHFIR_OUT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width (in pixel). The configured value is the actual value minus 1.

CH_CHFIR_OUT_SIZE

CH_CHFIR_OUT_SIZE is a horizontal chrominance scaling output size configuration register.

Offset Address	Register Name	Total Reset Value
0x10A1C	CH_CHFIR_OUT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width (in pixel). The configured value is the actual value minus 1. The picture width is set to the sum of the widths of the Cb and Cr chrominance components.

CH_LHFIR_COEF0

CH_LHFIR_COEF0 is horizontal luminance scaling coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x10A30	CH_LHFIR_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		coef2										coef1								coef0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	coef2	Horizontal luminance scaling and filtering coefficient 2
[19:10]	RW	coef1	Horizontal luminance scaling and filtering coefficient 1
[9:0]	RW	coef0	Horizontal luminance scaling and filtering coefficient 0 Only 8-tap horizontal scaling at an integral ratio is supported.

CH_LHFIR_COEF1

CH_LHFIR_COEF1 is horizontal luminance scaling coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x10A34	CH_LHFIR_COEF1	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef5								coef4												coef3							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	coef5	Horizontal luminance scaling and filtering coefficient 5
[19:10]	RW	coef4	Horizontal luminance scaling and filtering coefficient 4
[9:0]	RW	coef3	Horizontal luminance scaling and filtering coefficient 3

CH_LHFIR_COEF2

CH_LHFIR_COEF2 is horizontal luminance scaling coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x10A38	CH_LHFIR_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef7												coef6							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:10]	RW	coef7	Horizontal luminance scaling and filtering coefficient 7
[9:0]	RW	coef6	Horizontal luminance scaling and filtering coefficient 6

CH_CHFIR_COEF0

CH_CHFIR_COEF0 is chrominance horizontal scaling coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x10A40	CH_CHFIR_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef2								coef1												coef0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	coef2	Horizontal chrominance scaling and filtering coefficient 2
[19:10]	RW	coef1	Horizontal chrominance scaling and filtering coefficient 1
[9:0]	RW	coef0	Horizontal chrominance scaling and filtering coefficient 0 Only 8-tap horizontal scaling at an integral ratio is supported.

CH_CHFIR_COEF1

CH_CHFIR_COEF1 is chrominance horizontal scaling coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x10A44	CH_CHFIR_COEF1	0x0000_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef5								coef4												coef3							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	coef5	Horizontal chrominance scaling and filtering coefficient 5
[19:10]	RW	coef4	Horizontal chrominance scaling and filtering coefficient 4
[9:0]	RW	coef3	Horizontal chrominance scaling and filtering coefficient 3

CH_CHFIR_COEF2

CH_CHFIR_COEF2 is chrominance horizontal scaling coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x10A48	CH_CHFIR_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef7										coef6									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:10]	RW	coef7	Horizontal chrominance scaling and filtering coefficient 7
[9:0]	RW	coef6	Horizontal chrominance scaling and filtering coefficient 6

CH_VCDS_CFG

CH_VCDS_CFG is a vertical chrominance down sampling configuration register for large streams.

Offset Address	Register Name	Total Reset Value
0x10B00	CH_VCDS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Down sampling enable 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

CH_VCDS_COEF

CH_VCDS_COEF is a vertical chrominance down sampling coefficient register for large streams.

Offset Address	Register Name	Total Reset Value
0x10B04	CH_VCDS_COEF	0x0000_001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef1				reserved												coef0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:16]	RW	coef1	Down sampling coefficient 1
[15:5]	RO	reserved	Reserved
[4:0]	RW	coef0	Down sampling coefficient 0

CH_VCDS_IN_SIZE

CH_VCDS_IN_SIZE is a vertical chrominance down sampling input size configuration register.

Offset Address	Register Name	Total Reset Value
0x10B08	CH_VCDS_IN_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained picture. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained picture. The configured value is the actual value minus 1. The picture width is set to the width of the Cb/Cr component.

CH_CLIP_Y_CFG

CH_CLIP_Y_CFG is a luminance clamp configuration register.

Offset Address	Register Name	Total Reset Value
0x10C00	CH_CLIP_Y_CFG	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max																min															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	max	Maximum luminance value. When the data bit width is less than 16 bits, the upper bits are valid.
[15:0]	RW	min	Minimum luminance value. When the data bit width is less than 16 bits, the upper bits are valid.

CH_CLIP_C_CFG

CH_CLIP_C_CFG is a chrominance clamp configuration register.

Offset Address	Register Name	Total Reset Value
0x10C04	CH_CLIP_C_CFG	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	max																min															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	max	Maximum chrominance value. When the data bit width is less than 16 bits, the upper bits are valid.
[15:0]	RW	min	Minimum chrominance value. When the data bit width is less than 16 bits, the upper bits are valid.

10.2 VDP

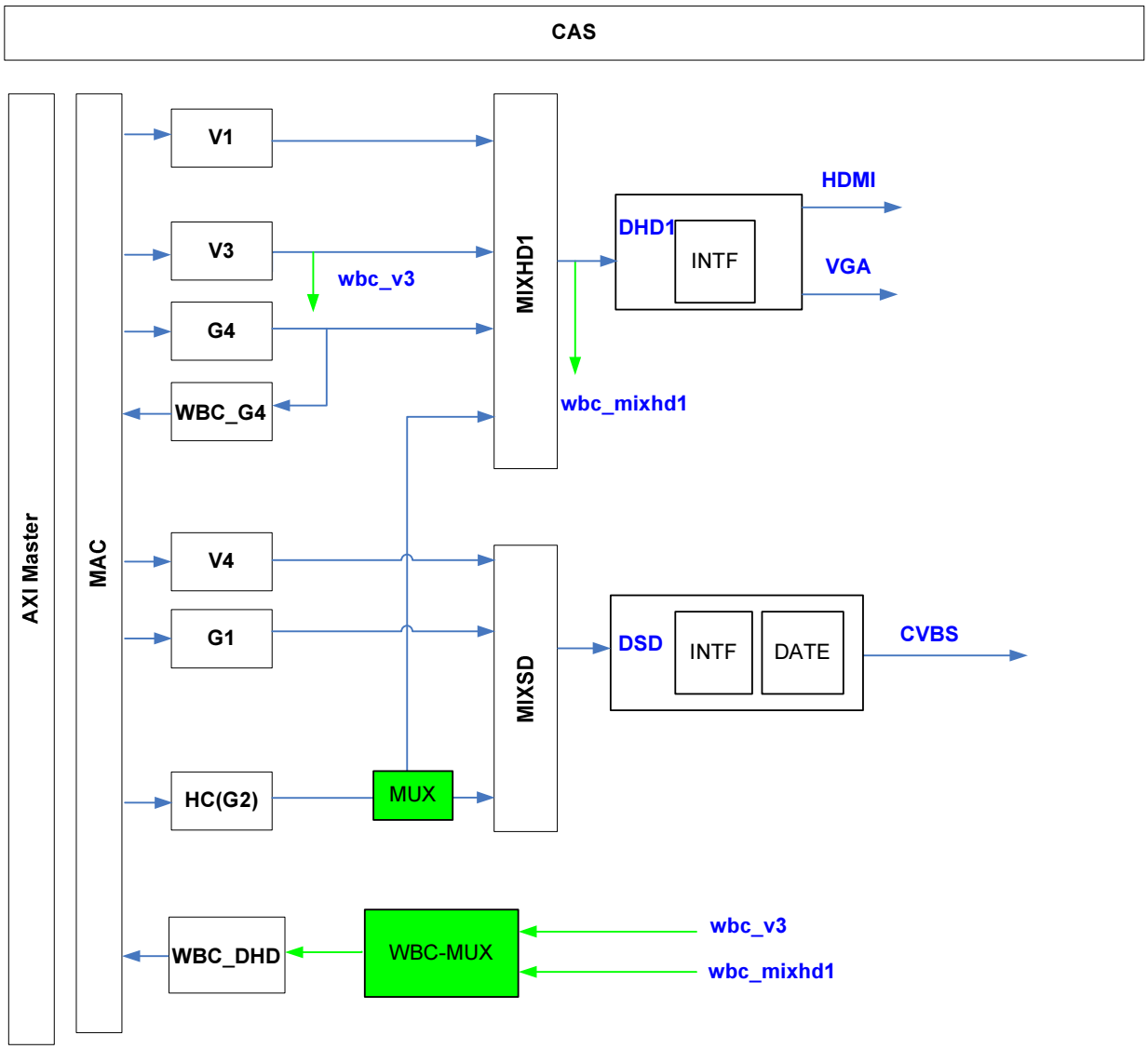
10.2.1 Overview

The video display processor (VDP) module reads video and graphics data from the DDR, overlays the data on the video and graphics layers, and transmits the data through the display channel.

10.2.2 Function Description

Figure 10-24 shows the overall architecture of the VDP module.

Figure 10-24 Overall architecture of the VDP module



- Surfaces: data paths of bus inputs. The surface reads the bus data of a layer and processes data. The surfaces include video layers (V1, V3, and V4), graphics layers (G1, and G4), and cursor layer (G2).
- Display channel: Display channels include high-definition display channels (DHD1) and standard-definition display channels (DSD).
- Mixers: The mixers include MIXHD1, and MIXSD and support overlapping of video layers and graphics layers.
- Parameter (PARA): It updates and loads the channel zoom engine (ZME) coefficients.
- MAC: bus request arbitration module of each layer. Each module reads data from the DDR over the AXI bus. The MAC arbitrates when layers raise requests.
- Control and status (CAS): It configures registers over the APB and reports the status of other modules to the CPU.

The VDP registers are classified into:

- Global registers
  Include the bus configuration register, interrupt register, and version register.
- Surface registers
  Include the video layer configuration register and graphics layer configuration register.
- Display channel registers
  Include the DHD1 and DSD configuration registers.
- Interface registers
  Include the HDMI, VGA, and CVBS configuration registers

The VDP module has the following features:

- AXI_master
  - Configurable value range of 1−15 for the outstanding
  - Multiple IDs. The IDs cannot be dynamically switched.
- Digital output interfaces
  - HDMI outputs for the HD channels DHD1
- Analog output interfaces
  - CVBS outputs for the SD channel DSD
  - VGA outputs for the HD channels DHD1
- Video layer
  - Input pixel formats: semi-planar YCbCr4:2:2 and semi-planar YCbCr4:2:0
  - Global alpha
  - Color space conversion (CSC) and adjustment of luminance, contrast, hue, and saturation
  - Vertical chrominance up sampling
  - Horizontal chrominance up sampling
  - Read/Write on multiple regions (16 regions for V3, and a single region for V1 and V4)
  - At most 16x scaling
- Graphics layer
  - Three graphics layers: graphics layers G1, and G4.
  - One cursor layer: G2
  - Data formats: ARGB8888, ARGB1555
  - Global alpha and pixel alpha
  - Three data extended modes
  - Even width and height
  - CSC and adjustment of luminance, contrast, hue, and saturation
  - Premultiplication
- Overlay
  - 256-level alpha blending of the background layer, video layers, graphics layers, and cursor layer. The priorities of graphics layers and video layers can be set.
  - Adjustment of the size and position of each overlay layer
  - Adjustment of the luminance, contrast, hue, and saturation of overlaid pictures–

- The VDP module has one HD channel and one SD channel. Each channel has a separate vertical timing interrupt (indicating the end of a field/frame), two low bandwidth interrupts, two writeback (WBC) completion interrupts, and four offload interrupts.

10.2.3 Operating Mode

10.2.3.1 Clock Configuration

The VDP module has one HD clock source of VPLL0. For details, see the description of the CRG register PERI_CRG12.

10.2.3.2 Reset

The VDP module supports a hard reset signal and a soft reset signal.

CAUTION

Before soft-resetting the AXI bus, do as follows:

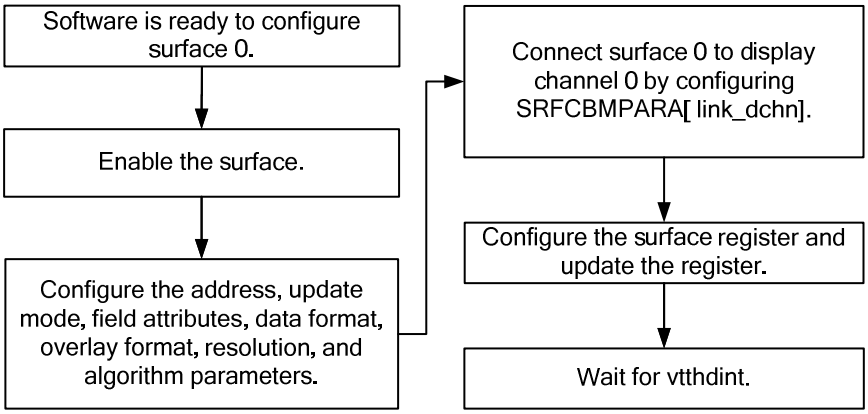
- Disable all layers.
- Configure the bus reset request after the next field/frame interrupt is detected.

10.2.3.3 Updating Registers and Coefficients

Updating Registers

Figure 10-25 shows the recommended process for configuring the surface register.

Figure 10-25 Recommended process for configuring the surface register

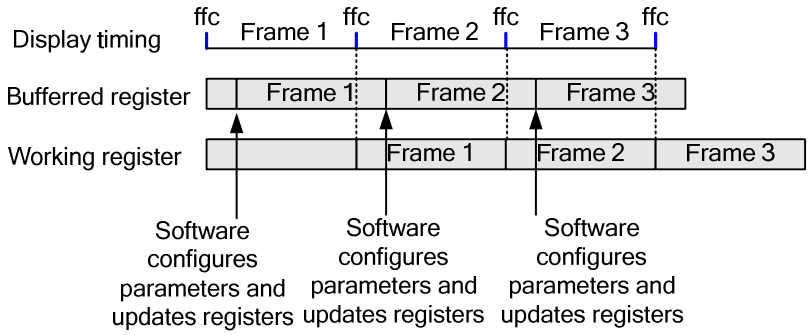


After surface 0 is connected to display channel 0, surface 0 updates its register based on the timing interrupt of display channel 0. Therefore, software needs to check whether the register update time is reached based on the vtthdint interrupt of display channel 0.

There are two sets of surface registers: working registers and buffered registers. The configurations of working registers are used by the current data channels. The register values

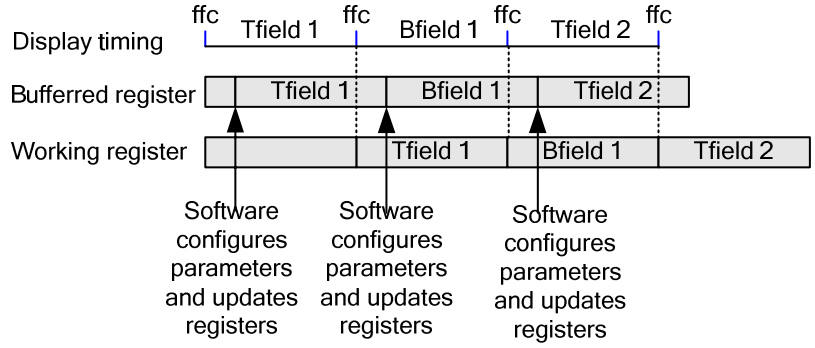
configured by software are buffered in the buffered registers. After the register update time is reached, the register values are imported to the working registers.

Figure 10-26 Surface register update mode (frame update mode)



The video layers support not only the frame update mode, but also the field update mode for the interlaced output, as shown in Figure 10-27. In this case, the interrupt frequency register regup_rate of video layers needs to be set to field update mode. ffc in Figure 10-27 indicates the time point of switching frame and field modes.

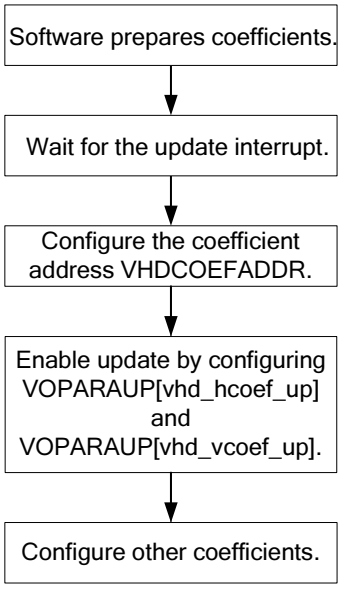
Figure 10-27 Surface register update mode (field update mode)



Storing and Updating On-chip Coefficients

The data amount of on-chip coefficients is large. To avoid additional CPU usage, software does not use the APB slave to configure the coefficients. Before hardware automatically updates the coefficients (reading coefficients by using the AXI master), software needs to configure the coefficient update enable bits and coefficient storage addresses. After that, hardware adds the address and update command to the coefficient update queue. Then the AXI master updates the address and command. Therefore, software can configure multiple coefficient update commands continuously. Figure 10-28 describes the process for updating scaling and filtering coefficients by using channel V3 as an example.

Figure 10-28 Example of updating on-chip coefficients



10.2.3.4 Analog Output Interfaces

The VDP module supports two types of analog output interfaces:

- CVBS interface
- VGA interface

CVBS Interface

- CVBS output interface supported by SD channels
- DSD -> CVBS
- PAL and NTSC standards supported by the CVBS interface

VGA Interface

The VDP module supports VGA interface.

- Output resolution ranging from 800 x 600 to 1920x1080/1600x1200
- Clock frequency ranging from 40 MHz to 162 MHz
- RGB888 output supported by configuring the channel CSC function

Digital Output Interfaces

The VDP module supports two types of digital output interfaces:

- HDMI interface

HDMI Interface

The Hi3521A HDMI interface is a standard HDMI 1.4a interface. Its video source is DHD1.

- Maximum output resolution of 1920x1080/1600x1200

- Clock frequency ranging from 74.25 MHz to 162 MHz
- Interlaced and progressive display
- Output data format of YCbCr444

10.2.3.5 HD Video Layers

V3 supports simultaneous display on a maximum of 16 regions, whereas V1 and V4 support the display on a single region.

Reading Multiple Regions for V3

The VDP module can read multiple regions to display their pictures at the same time. The data sources of regions can be different. The details are as follows:

- Multi-region specifications supported by V3
- Input pixel formats of semi-planar420 and semi-planar422
- A multiple of 2 for the input horizontal resolution, a multiple of 4 for the interlaced 420 vertical resolution, and a multiple of 2 for other vertical resolutions
- A maximum of 16 regions for V3
- User-defined region size, minimum resolution of 32 x 32, and maximum resolution of 1920 x 1080
- Separate enabling for each region
- User-defined display position of each region by configuring the start and end coordinates of the region, anywhere on the screen
- User-defined source start addresses (including luminance and chrominance addresses) of regions, 2-byte-aligned compressed address, and 16-byte-aligned decompressed address
- User-defined source stride addresses (including luminance and chrominance addresses) of regions, 16-byte-aligned
- Interlaced and progressive modes
- When the single region mode of V3 is enabled, only region 0 is available. In this case, V3 is equivalent to V1/V4.

Reading a Single Region for V1

- Input pixel formats of semi-planar420 and semi-planar422
- A multiple of 2 for the input horizontal resolution, a multiple of 4 for the interlaced 420 vertical resolution, and a multiple of 2 for other vertical resolutions
- Minimum input/output resolution of 32 x 32, and maximum input/output resolution of 1920 x 1080

Display Position

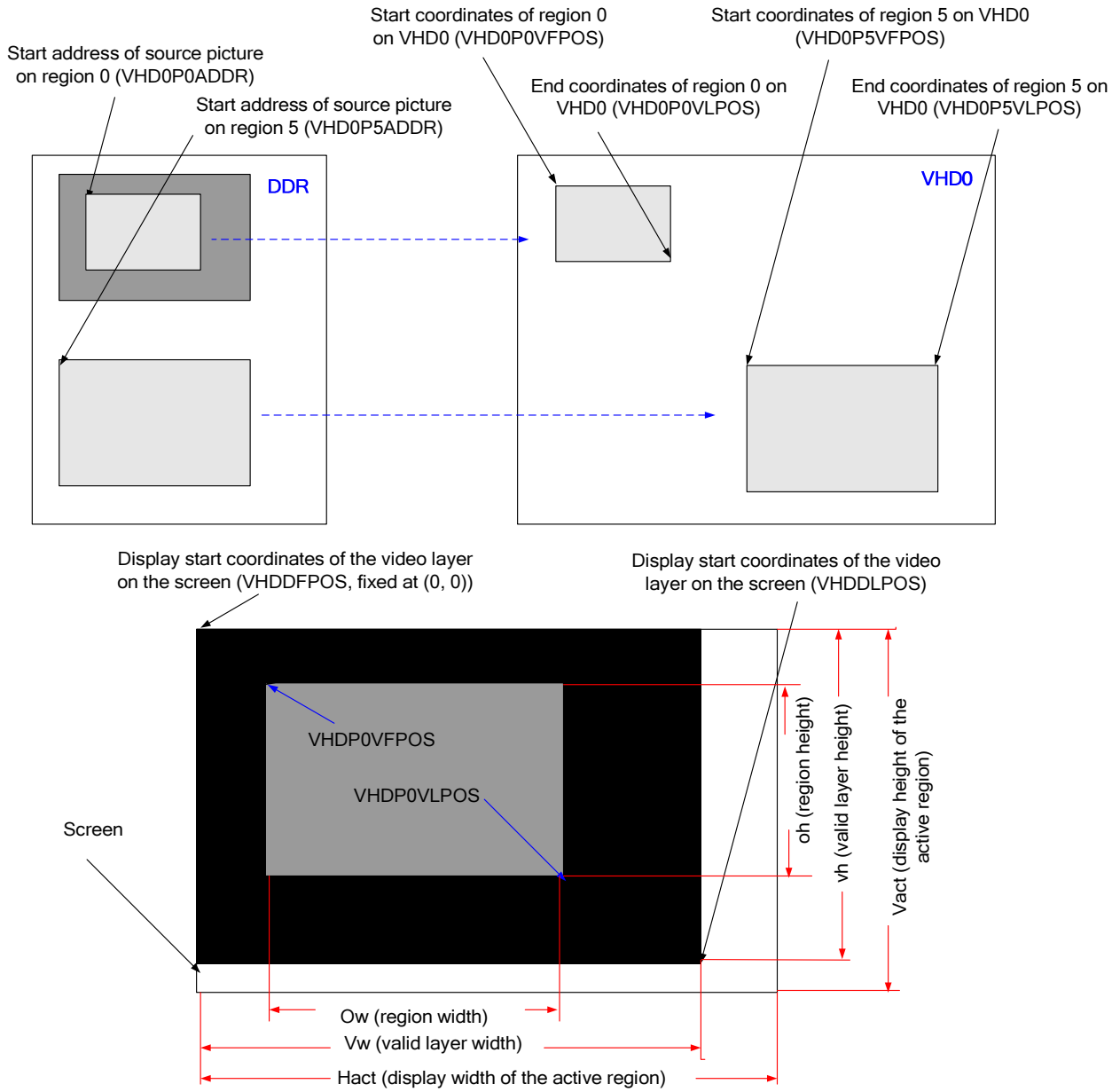
The VDP module allows you to set the video display position.

The video layer has three sets of coordinates.

- Source start coordinates for reading data. The VDP module is configured with the start address calculated by the CPU.
- Start and end coordinates of the video layer relative to the displayed area
- Display start and end coordinates of the video layer on the screen

- The combination of three sets of coordinates enables video sources to be displayed anywhere on the screen.

Figure 10-29 Three sets of coordinates



CAUTION

In multi-region mode, the display start coordinates of the video layer on the screen must be set to (0, 0).

Scaling

The VDP module has a high-performance scaling engine that supports scaling at various ratios. The details are as follows:

- The V3 scaling function supports only zoom in and at most 16x zoom in.
- The video formats semi-planar420 and semi-planar422 are supported.
- The filtering mode and replication mode are supported.
- The functions of 8-tap horizontal luminance filtering and 4-tap horizontal chrominance filtering are supported. For each filtering type, 32 phases are provided, and filtering coefficients can be configured.
- The functions of 4-tap vertical luminance filtering and 4-tap vertical chrominance filtering are supported. For each filtering type, 32 phases are provided, and filtering coefficients can be configured.
- The AXI automatically loads scaling coefficients from the DDR.
- Vertical luminance/chrominance and horizontal luminance/chrominance can be configured separately.
- One pixel is output every one clock cycle.

420-422 (Vertical Chrominance Up Sampling)

When YUV420 data is input, 2x vertical scaling must be performed on the chrominance to convert the data format into YUV422.

V1 supports the following two configurable data conversion modes:

- 4-tap filtering
- Replication

CAUTION

V4 supports only the replication mode.

IFIR (Horizontal Chrominance Up Sampling)

After horizontal chrominance up sampling, the YCbCr422 data format is converted into YCbCr444.

This function can be implemented in three ways:

- Replication
- Bilinear interpolation
- 16-tap filtering

CSC

- CSC between YUV709 and YUV601
- CSC between RGB and YUV

10.2.4 SD Video Layers

The VDP module has one SD video layer V4. The details are as follows:

- Support for only one region
- Input pixel formats of semi-planar420 and semi-planar422
- Minimum input resolution of 32 x 32 and maximum input resolution of 720 x 576
- Minimum output resolution of 32 x 32 and maximum output resolution of 720 x 576
- A multiple of 2 for the input horizontal resolution, and a multiple of 4 for the interlaced 420 vertical resolution and other vertical resolutions
- Interlaced mode and progressive mode
- User-defined source luminance and chrominance start addresses, 2-byte-aligned
- User-defined source luminance and chrominance stride, 16-byte aligned
- CSC from YCbCr to RGB and adjustment of contrast, hue, and saturation
- User-defined display position, anywhere on the screen
- User-defined global alpha ranging from 0 to 255
- Data format conversion from 420 to 422 for V4 by repeatedly reading chrominance

10.2.4.1 Graphics Layers

The graphics layers include G1 and G4.

Decompression

Only G4 can decompress the pictures that are compressed in lossless mode. The details are as follows:

- Input pixel format of ARGB8888/ARGB1555
- Interlaced compression and progressive compression
- Minimum input/output resolution 32 x 32 and maximum input/output resolution 1920 x 1080.
- A multiple of 2 for the vertical resolution
- Compression mode and RAW mode. In compression mode, the pixel and alpha can be separately configured as the lossy mode or lossless mode. Note that the lossless pixel compression mode and lossy alpha compression mode are not supported at the same time.
- Decompression performance of 1 pixel/clock

Data is decompressed by line. The data to be decompressed consists of two parts: header information and compressed data. The header information contains the number of pixels (in the unit of 128 bits) in a line. The header information is stored in the lower 16 bits (bit[15:0]) of the first data segment in a line.

CSC

The CSCs among RGB, YCbCr601, YCbCr709, xvYCC601, and xvYCC709 are supported.

Alpha Processing

The alpha value sources of graphics layers are as follows:

- Pixel alpha value: overlay attribute of a pixel
- Global alpha value: overlay attributes of a layer

There is a special case for the pixel alpha value. In ARGB1555 format, the alpha value is only one bit. This bit is the index of the alpha value rather than the actual alpha value. The index value is used to select the actual alpha value from the alpha register. When the index value is 0, alpha0 is selected; when the index value is other values, alpha1 is selected.

Colorkey

- The key mode is configurable. The pixels inside or outside the range can be selected for key processing.
- The key bit can be masked.

Premultiplication

Premultiplication and colorkey are not supported at the same time.

HC Layer

The details of the G2 cursor layer are as follows:

- Input pixel formats of ARGB1555 and ARGB8888
- Minimum input resolution of 2 x 2 and maximum input resolution of 256x256
- Minimum output resolution of 2 x 2 and maximum output resolution is 256x256
- A multiple of 2 for the input vertical resolution
- Interlaced mode and progressive mode
- Frame update and field update
- User-defined source start address, 128-bit-aligned (16-byte-aligned)
- User-defined source stride, 128-bit-aligned (16-byte-aligned)
- CSC from RGB to YUV 709 and from RGB to YUV 601
- User-defined display position, anywhere on the screen
- User-defined global alpha ranging from 0 to 255
- Enabling or disabling of the pixel alpha, and alpha0 or alpha1 for the picture in ARGB1555 format with pixel alpha
- Colorkey processing
- Premultiplication

10.2.4.2 Layer Overlay

The VDP supports three mixers. The data of the two mixers is output through specific channels. The mapping between mixers and output channel is as follows:

- MIXHD1 –> DHD1
- MIXSD –> DSD

The binding relationships are as follows:

- The video/graphics layers V3, V1, and G4 are always bound to MIXHD1.
- The video/graphics layers V4 and G1 are always bound to MIXSD.
- The G2 cursor layer can be bound to MIXHD1 or MIXSD.

- The background colors of MIXHD1 and MIXSD can be separately configured.

The following configurations are performed:

Step 1 Disable related VO interfaces.

Step 2 Configure the registers of each layer.

Step 3 Configure the priority of each layer.

Step 4 Enable related VO interfaces.

----End

CAUTION

- G2 can be bound only to MIXHD1 or MIXSD.
- G2 can drive different mixers. However, the driven mixer cannot be switched in real-time. That is, you must disable the related VO interface before changing the mixer driven by the layer.

10.2.4.3 Processing Functions of HD Interfaces

Clip

The VDP provides flexible clip function.

- According to the interface timing protocol, the output data must be within a range. If the data exceeds the range, the data must be clipped.
- You can determine whether to enable the clip function. The upper and lower limits for clipping can be configured and the clipping performance is 1 pixel/clock.
- Only the HDMI supports the clip function.

H_SHARPEN

The VGA interface of the VDP module has the configurable horizontal sharpening (HSP) function.

- The HSP function is used to enhance HSP effects on the VGA channel.
- The HSP function can be enabled or disabled.
- Only the VGA interface supports HSP.

CSC

- CSC from YUV601 to RGB and from YUV709 to RGB
- Adjustment of luminance, contrast, hue, and saturation
- The HDMI and VGA interfaces each have as a set of separate CSC logic.

10.2.4.4 Processing Functions of SD Interface

The VDP has one SD interface: CVBS. The details are as follows:

- Data of the SD channel DSD output from the CVBS interface
- PAL and NTSC standards
- Clip enable
- User-defined upper and lower limits for clipping

10.2.4.5 WB Function of the WBC_DHD Channel

After the video data or overlaid video and graphics data is scaled, the WBC_DHD channel writes the data back to the DDR.

The WBC_DHD channel supports two WB points:

- V3 WB points. For these WB points, only valid video data is written back.
- MIXHD1 WB points. For these WB points, the full-screen data obtained after videos and graphics are overlaid is written back.

Progressive and Interlaced WBC

The progressive and interlaced WBC modes of the VDP module can be configured.

- WBC_DHD WBC enable (configurable)
- Output data formats of semi-planar422 and semi-planar420
- Progressive WBC and interlaced WBC
- Input resolution range of 32 x 32 to 1920 x 1080
- Output resolution range of 32 x 32 to 1280 x 720

WBC_DHD Scaling

The VDP module supports high-quality zoom-out with configurable zoom-out multiple during WBC.

- Only WBC_DHD zoom-out function is supported.
- The minimum input resolution is 32 x 32 and the maximum input resolution is 1920 x 1080 during WBC_DHD scaling.
- The minimum output resolution is 32 x 32 and the maximum output resolution is 1280x720 during WBC_DHD scaling.
- The filtering mode and replication mode are supported.
- The functions of 8-tap horizontal luminance filtering and 4-tap horizontal chrominance filtering are supported. For each filtering type, 32 phases are provided, and filtering coefficients can be configured
- The functions of 6-tap vertical luminance filtering and 4-tap vertical chrominance filtering are supported. For each filtering type, 32 phases are provided, and filtering coefficients can be configured
- The AXI automatically loads scaling coefficients from the DDR.
- Vertical luminance/chrominance and horizontal luminance/chrominance can be configured separately.
- One pixel is output every one clock cycle.

10.2.4.6 WB Function of the WBC_G4 Channel

When G4 works, WBC_G4 compresses the G4 data and writes the compressed data to the DDR. If the G4 input picture is not updated, the compressed data can be read and then decompressed for displaying, which reduces the system bandwidth and power consumption. WBC_G4 compresses the G4 data.

- Input and output data formats of ARGB8888/ARGB1555
- Minimum input/output resolution of 32 x 32 and maximum input/output resolution of 1920 x 1080
- Partial compression by line
- Automatic WB stop

10.2.4.7 Compression

The compression function supported by the VDP module has the following features:

- Input data formats of ARGB8888 and ARGB1555
- Minimum input/output resolution of 32 x 32 and maximum input/output resolution of 1920 x 1080
- Lossy and lossless compression modes
- Input picture with the horizontal resolution of a multiple of 2
- Partial compression by line. The compressed data is also stored by line. The compressed data in each line consists of two parts: header information and compressed data. The header information is stored in the lower 16 bits of the compressed data in each line, and is followed by the compressed data. The header information indicates the number of 128-bit data segments in the compressed data of each line.

10.2.4.8 Interrupts

The VDP module supports four types of interrupts:

- Vertical timing interrupt
- Low bandwidth interrupt
- WBC completion interrupt
- Offload interrupt

Vertical Timing Interrupt

Each channel of the VDP module has independent vertical timing interrupts. The positions for generating interrupts can be flexibly configured.

- Four vertical timing interrupts that indicate the end of a frame or field. The VDP module has one HD channel and one SD channel. The HD channel has three vertical timing interrupts and the SD channel has one vertical timing interrupt.
- Interrupt generation modes of generation by frame and by field
- Mode of generating vertical timing interrupts configured as generation by frame in progressive display mode
- Mode of generating vertical timing interrupts configured as generation by frame or by field in interlaced display mode. You are advised to set the interrupt generation mode to generation by field for HD and generation by field for SD.
- Configurable interrupt mask

- Configurable threshold of vertical timing interrupts
- Separate enabling and disabling of each interrupt source. Writing 1 clears the interrupt.

Low Bandwidth Interrupt

The VDP module has one HD channels and one SD channel. Each channel has an independent low bandwidth interrupt that indicates the low bandwidth information about a frame or field. The VDP module supports two low bandwidth interrupts (one for the HD channels and one for the SD channel). The details are as follows:

- Interrupt generation modes of generation by frame and field.
- Mode of generating vertical timing interrupts configured as generation by frame in progressive display mode.
- Mode of generating vertical timing interrupts configured as generation by frame or by field in interlaced display mode. You are advised to set the interrupt generation mode to generation by field for HD and generation by field for SD.
- Configurable interrupt mask.
- Separate enabling and disabling of each interrupt source. Writing 1 clears the interrupt.

WBC Completion Interrupt

The VDP module allows the WB status to be reported in interrupt mode.

- The VDP has a WB channel WBC_DHD and a compression WB channel WBC_G4. Therefore, the VDP module supports two WBC interrupts that indicate all frame/field data is written back.
- Configurable interrupt mask.
- Separate enabling and disabling of the interrupt source. Writing 1 clears the interrupt.

Offload Interrupt

The VDP module supports VDAC cable detection. The four DACs correspond to four DAC offload interrupts. The value 0 indicates that there are loads, and the value 1 indicates that there is no load.

- Configurable interrupt mask
- Separate enabling and disabling of the interrupt source. Writing 1 clears the interrupt.

10.2.4.9 Low-Power Control

The VDP module supports configurable clock gating:

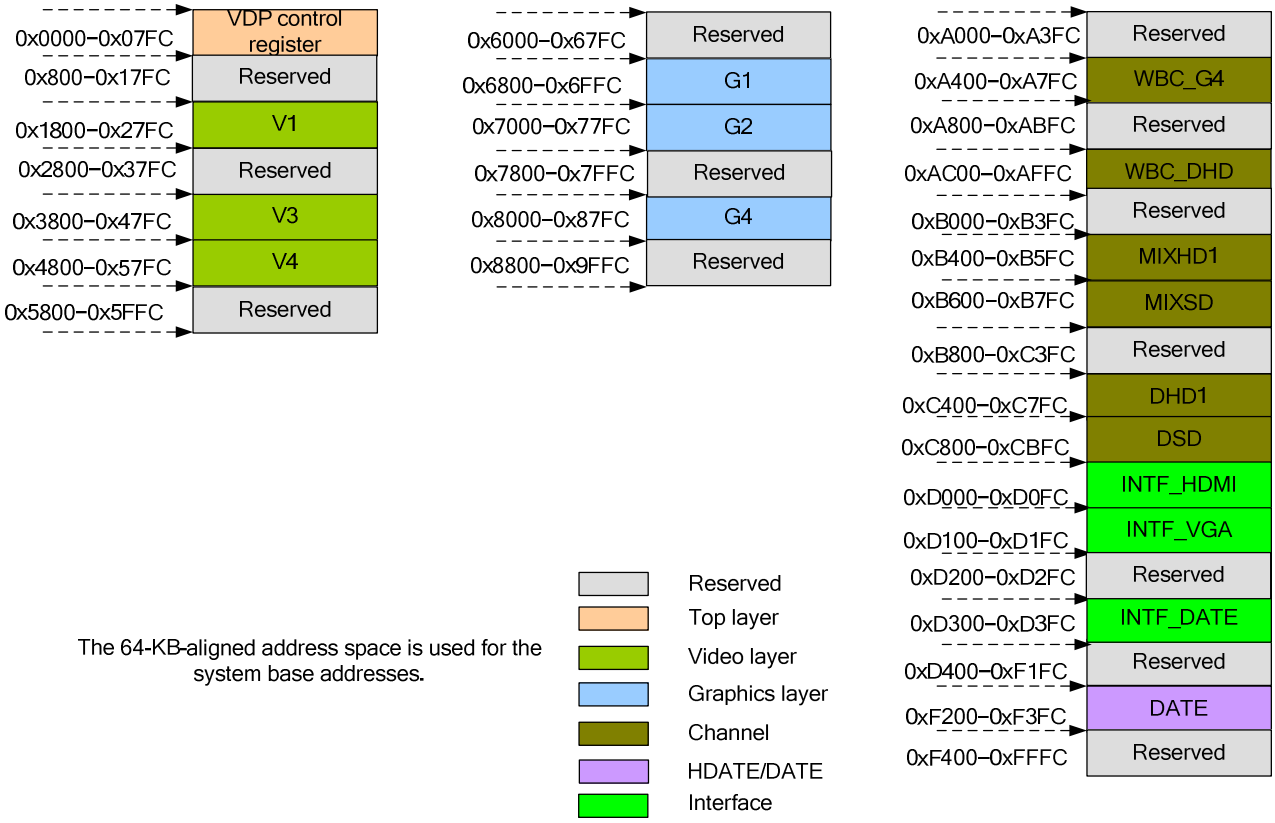
- The dynamic clock gating of the memory is controlled by using the clock gating signal ck_gate_en.
  - 0: The clock is directly input to the memory.
  - 1: The memory clock is forced to 0.
- All VDP services (including all layers and channels) must be disabled before dynamic clock gating is enabled.

10.2.5 Register Summary

10.2.5.1 Register Address Space

Figure 10-30 shows the address space of VDP registers.

Figure 10-30 Address space of VDP registers



Differences Among Video Layer Registers

Video layers include V1, V3, and V4. The following describes the differences based on V3 registers:

- The V3 registers support 16 regions (region 0–region 15).
- The V1 registers support only region 0.
- The V1 registers support only CVFIR but not ZME.
- The V4 registers support only region 0.
- The V4 registers do not support the ZME and decompression.

Differences Among Graphics Layer Registers

Graphics layers include G1, G2, and G4. The following describes the differences based on G4 registers:

- The G1 registers do not support decompression.

- The G2 CSC registers support two conversion modes. Their coefficients cannot be configured.

Differences Among Channel Registers

The registers for all channels are the same.

Differences Among Interface Processing Registers

The VDP interfaces include the HDMI, VGA, and CVBS interfaces.

- The CVBS interfaces support only clip.
- The VGA interface supports only HSP and CSC.
- The HDMI supports only CSC and clip.

CAUTION

For multi-region registers, only the seven registers (addresses ranging from 0x0A00 to 0x0A18) of region 0 are reserved. The addresses of other regions are obtained through the offset based on the address of region 0. The address of each region is calculated as follows: address = 0x0A00 + (0x20 x Region ID).

10.2.6 VDP Register Summary

Table 10-6 describes VDP registers.

Table 10-6 Summary of VDP registers (base address: 0x1302_0000)

Offset Address	Register	Description	Page
0x0000	VOCTRL	VO control register	10-106
0x0004	VOINTSTA	VO interrupt status register	10-107
0x0008	VOMSKINTSTA	VO masked interrupt status register	10-109
0x000C	VOINTMSK	VDP interrupt mask register	10-111
0x0010	VDPVERSION1	VDP version register 1	10-113
0x0014	VDPVERSION2	VDP version register 2	10-114
0x0034	VOAXICTRL	VO AXI bus configuration register	10-114
0x0100	VO_MUX	VO interface multiplexing register	10-115
0x0104	VO_MUX_DAC	VO DAC interface multiplexing register	10-115

Offset Address	Register	Description	Page
0x0108	VO_MUX_TESTSYNC	VO interface test register	10-117
0x010C	VO_MUX_TESTDATA	VO interface test data register	10-117
0x0120	VO_DAC_CTRL	VO DAC control register	10-118
0x0130	VO_DAC_C_CTRL	VO DAC C channel control register	10-119
0x0134	VO_DAC_R_CTRL	VO DAC R channel control register	10-120
0x0138	VO_DAC_G_CTRL	VO DAC G channel control register	10-120
0x013C	VO_DAC_B_CTRL	VO DAC B channel control register	10-121
0x030C	GDC_CORRESP	Graphics layer binding relationship register	10-122
0x0310	WBC_CORRESP	WBC point binding relationship register	10-123
0x0400	COEF_DATA	Virtual coefficient register	10-123
0x0414	V1_PARARD	V1 coefficient read flag register	10-124
0x041C	V3_PARARD	V3 coefficient read flag register	10-124
0x04C0	WBCDHD_PARARD	WBC_DHD coefficient read flag register	10-125
0x3800	V3_CTRL	V3 configuration register	10-126
0x3804	V3_UPD	V3 channel update enable register	10-128
0x3820	V3_PRERD	V3 prefetch enable register	10-128
0x3828	V3_IRESO	V3 input resolution register	10-129
0x382C	V3_ORESO	V3 output resolution register	10-129
0x3838	V3_CBMPARA	V3 overlay parameter register	10-130
0x3840	V3_PARAUP	V3 coefficient-related register update enable register	10-130
0x3850	V3_HLCOEFAD	V3 horizontal luminance filtering coefficient address register	10-131
0x3854	V3_HCCOEFAD	V3 horizontal chrominance filtering coefficient address register	10-132
0x3858	V3_VLCOEFAD	V3 vertical luminance filtering coefficient address register	10-132
0x385C	V3_VCCOEFAD	V3 vertical chrominance filtering coefficient address register	10-132

Offset Address	Register	Description	Page
0x3880	V3_CSC_IDC	V3 CSC input DC component register	10-133
0x3884	V3_CSC_ODC	V3 CSC output DC component register	10-133
0x3888	V3_CSC_IODC	CSC input/output DC component register	10-134
0x388C	V3_CSC_P0	CSC parameter 0 register	10-135
0x3890	V3_CSC_P1	CSC parameter 1 register	10-135
0x3894	V3_CSC_P2	CSC parameter 2 register	10-136
0x3898	V3_CSC_P3	CSC parameter 3 register	10-136
0x389C	V3_CSC_P4	CSC parameter 4 register	10-137
0x38C0	V3_HSP	V3 horizontal scaling parameter register	10-137
0x08C4	V3_HLOFFSET	V3 horizontal luminance offset register	10-138
0x38C8	V3_HCOFFSET	V3 horizontal chrominance offset register	10-139
0x38D8	V3_VSP	V3 vertical scaling parameter register	10-139
0x38DC	V3_VSR	Vertical luminance scaling ratio register	10-140
0x38E0	V3_VOFFSET	V3 vertical luminance scaling offset register	10-141
0x38E4	V3_VBOFFSET	V3 vertical luminance scaling offset register for the bottom field	10-141
0x3900	V3_DFPOS	V3 surface start position (in the display window) register	10-142
0x3904	V3_DLPOS	V3 surface end position (in the display window) register	10-142
0x3908	V3_VFPOS	V3 surface content start position (in the display window) register	10-143
0x390C	V3_VLPOS	V3 surface content end position (in the display window) register	10-143
0x3910	V3_BK	V3 background color register	10-144
0x3914	V3_ALPHA	V3 background filling color alpha register	10-144
0x3918	V3_RIMWIDTH	V3 RIM width register	10-145

Offset Address	Register	Description	Page
0x391C	V3_RIMCOL0	RIM color 0 register (non-instant register) for the upper 32 regions at the V3 video layer	10-145
0x3920	V3_RIMCOL1	RIM color 1 register (non-instant register) for the upper 32 regions at the V3 video layer	10-146
0x3980	V3_IFIRCOEF01	IFIR filtering coefficient 0/1 register	10-146
0x3984	V3_IFIRCOEF23	IFIR filtering coefficient 2/3 register	10-147
0x3988	V3_IFIRCOEF45	IFIR filtering coefficient 4/5 register	10-147
0x398C	V3_IFIRCOEF67	IFIR filtering coefficient 6/7 register	10-148
0x3A00	V3_P0RESO	V3 region 0 resolution register	10-148
0x3A04	V3_P0LADDR	V3 region 0 luminance address register	10-149
0x3A08	V3_P0CADDR	V3 region 0 chrominance address register	10-149
0x3A0C	V3_P0STRIDE	V3 region 0 stride register	10-150
0x3A10	V3_P0VFPOS	Video content start position (in the display window) register (non-instant) for V3 region 0	10-150
0x3A14	V3_P0VLPOS	Video content end position (in the display window) register (non-instant) for V3 region 0	10-150
0x3A18	V3_P0CTRL	V3 region 0 control register	10-151
0x4230	V3_MULTI_MODE	Multi-region mode enable register	10-152
0x4250	V3_FDRFIFOTHD	V3 FDR FIFO threshold register	10-152
0x4350	V3_MRGERRCLR	V3 multi-region register operation error status clear register	10-153
0x4354	V3_MRG_ERR	V3 multi-region register operation error signal register	10-153
0x8000	G4_CTRL	G4 configuration register (non-instant register)	10-154
0x8004	G4_UPD	G4 update enable register	10-156
0x8010	G4_ADDR	G4 address register	10-156
0x801C	G4_STRIDE	G4 stride register	10-156
0x8020	G4_IRESO	G4 input resolution register	10-157

Offset Address	Register	Description	Page
0x8024	G4_SFPOS	G4 surface read data start position (in the source bitmap) register	10-157
0x8030	G4_CBMPARA	G4 overlay parameter register	10-158
0x8034	G4_CKEYMAX	G4 maximum colorkey register	10-159
0x8038	G4_CKEYMIN	G4 minimum colorkey register	10-159
0x803C	G4_CMASK	G4 masked colorkey register	10-160
0x8048	G4_FIFOTHD	G4 buffer threshold register	10-160
0x8060	G4_DCMP_DBG	Debugging signal register for the DCMP module	10-161
0x8070	G4_DCMP_INTER	Error interrupt information register for the DCMP module	10-161
0x8080	G4_DFPOS	G4 surface start position (in the display window) register	10-162
0x8084	G4_DLPOS	G4 surface end position (in the display window) register	10-162
0x80C0	G4_CSC_IDC	G4 CSC input DC component register	10-163
0x80C4	G4_CSC_ODC	G4 CSC output DC component register	10-164
0x80C8	G4_CSC_IODC	G4 CSC input/output DC component register	10-164
0x80CC	G4_CSC_P0	G4 CSC parameter 0 register	10-165
0x80D0	G4_CSC_P1	G4 CSC parameter 1 register	10-165
0x80D4	G4_CSC_P2	G4 CSC parameter 2 register	10-166
0x80D8	G4_CSC_P3	G4 CSC parameter 3 register	10-167
0x80DC	G4_CSC_P4	G4 CSC parameter 4 register	10-167
0xA400	WBC_G4_CTRL	WBC0 control register	10-167
0xA404	WBC_G4_UPD	WBC0 channel update enable register	10-168
0xA410	WBC_G4_ADDR	Capture luminance write address register	10-169
0xA418	WBC_G4_STRIDE	Capture stride register	10-169
0xA420	WBC_G4_ORESO	Output resolution register	10-169
0xA424	WBC_G4_YCROP	Input picture crop start/end vertical coordinate register	10-170
0xA434	WBC_G4_CSTR_ERR	Compressed picture stride configuration error status register	10-170

Offset Address	Register	Description	Page
0xA438	WBC_G4_CLR_CSTR_ERR	Compressed picture stride configuration error status clear register	10-171
0xA480	WBC_G4_GLB_INFO	LCMP global control information register	10-171
0xA484	WBC_G4_FRAME_SIZE	Picture size register	10-172
0xA488	WBC_G4_RC_CFG0	Rate control (RC) parameter 0 register	10-173
0xA48C	WBC_G4_RC_CFG1	RC parameter 1 register	10-173
0xA490	WBC_G4_RC_CFG2	RC parameter 2 register	10-174
0xA494	WBC_G4_RC_CFG3	RC parameter 3 register	10-175
0xA498	WBC_G4_RC_CFG4	RC parameter 4 register	10-175
0xA49C	WBC_G4_RC_CFG5	RC parameter 5 register	10-176
0xA4A0	WBC_G4_RC_CFG6	RC parameter 6 register	10-176
0xA4A4	WBC_G4_RC_CFG7	RC parameter 7 register	10-177
0xA4A8	WBC_G4_RC_CFG8	RC parameter 8 register	10-177
0xA4AC	WBC_G4_RC_CFG9	RC parameter 9 register	10-178
0xA4B0	WBC_G4_MAX_ROW_LEN	128-bit unit register for the row with the lowest compression ratio	10-178
0xAC00	WBC_DHD1_CTRL	WBC0 control register	10-178
0xAC04	WBC_DHD1_UPD	WBC0 channel update enable register	10-180
0xAC10	WBC_DHD1_YADDR	Capture luminance write address register	10-180
0xAC14	WBC_DHD1_CADDR	Capture chrominance write address register	10-180
0xAC18	WBC_DHD1_STRIDE	Capture stride register	10-181
0xAC20	WBC_DHD1_ORESO	Output resolution register	10-181
0xAC40	WBC_DHD1_PARAUP	gp1 coefficient-related register update enable register	10-182
0xAC50	WBC_DHD1_HLCOEFAD	WBC horizontal luminance filtering coefficient address register	10-183
0xAC54	WBC_DHD1_HCCOEFAD	WBC horizontal chrominance filtering coefficient address register	10-183
0xAC58	WBC_DHD1_VLCOEFAD	WBC vertical luminance filtering coefficient address register	10-183

Offset Address	Register	Description	Page
0xAC5C	WBC_DHD1_VCCOEFAD	WBC vertical chrominance filtering coefficient address register	10-184
0xAD00	WBC_DHD1_DITHER_CTRL	Dither control register	10-184
0xAD04	WBC_DHD1_DITHER_COEF0	Dither coefficient 0 register	10-185
0xAD08	WBC_DHD1_DITHER_COEF1	Dither coefficient 1 register	10-185
0xAE10	WBC_DHD1_HCDS	Horizontal chrominance down sampling parameter configuration register	10-186
0xAE14	WBC_DHD1_HCDS_COEF0	Down sampling coefficient register 0	10-187
0xAE18	WBC_DHD1_HCDS_COEF1	Down sampling coefficient register 1	10-187
0xAEC0	WBC_DHD1_ZME_HSP	Horizontal scaling parameter configuration register	10-187
0xAEC4	WBC_DHD1_ZME_HLOFFSET	Horizontal luminance offset register	10-189
0xAEC8	WBC_DHD1_ZME_HCOFFSET	Horizontal chrominance offset register	10-189
0xAED8	WBC_DHD1_ZME_VSP	Vertical scaling parameter register	10-189
0xAEDC	WBC_DHD1_ZME_VSR	Vertical luminance scaling ratio register	10-191
0xAEE0	WBC_DHD1_ZME_VOFFSET	Vertical luminance scaling offset register	10-191
0xAEE4	WBC_DHD1_ZME_VBOFFSET	Vertical luminance scaling offset register for the bottom field	10-192
0xB420	CBM_BKG2	CBM mixer 2 overlay background color register	10-192
0xB428	CBM_MIX2	CBM mixer 2 priority configuration register	10-193
0xB600	MIXDSD_BKG	DSD mixer 1 overlay background color register	10-194
0xB608	MIXDSD_MIX	DSD mixer 1 priority configuration register	10-195
0xC400	DHD1_CTRL	Display channel global control register	10-196

Offset Address	Register	Description	Page
0xC404	DHD1_VSYNC	Top field vertical sync timing register in interlaced output mode or frame vertical sync timing register in progressive output mode	10-197
0xC408	DHD1_HSYNC1	Horizontal sync configuration register 1 in interlaced or progressive output mode	10-198
0xC40C	DHD1_HSYNC2	Horizontal sync configuration register 2 in interlaced or progressive output mode	10-198
0xC410	DHD1_VPLUS	Bottom field vertical sync timing in interlaced output mode	10-198
0xC414	DHD1_PWR	Sync signal pulse width register	10-199
0xC418	DHD1_VTTHD3	Vertical timing threshold register	10-199
0xC41C	DHD1_VTTHD	Vertical timing threshold register	10-200
0xC430	DHD1_AFFTHD	DHD buffer FIFO register	10-201
0xC434	DHD1_ABUFTHD	DHD buffer register	10-201
0xC438	DHD1_DACDET1	DAC automatic detection register 1	10-202
0xC43C	DHD1_DACDET2	DAC automatic detection register 2	10-202
0xC4B0	DHD1_PARATHD	PARA coefficient update point threshold register	10-203
0xC4B4	DHD1_START_POS	DHD start signal start position register	10-203
0xC4F0	DHD1_STATE	DHD1 status register	10-204
0xD000	INTF_CTRL	Output interface control register	10-205
0xD008	INTF_SYNC_INV	Sync signal polarity configuration register in external sync timing output mode	10-205
0xD010	INTF_CLIP0_L	Clip lowest threshold register	10-206
0xD014	INTF_CLIP0_H	Clip highest threshold register	10-206
0xD020	INTF_CSC_IDC	CSC input DC component register	10-207
0xD024	INTF_CSC_ODC	CSC output DC component register	10-208
0xD028	INTF_CSC_IODC	CSC input/output DC component register	10-208
0xD02C	INTF_CSC_P0	CSC parameter 0 register	10-209
0xD030	INTF_CSC_P1	CSC parameter 1 register	10-209

Offset Address	Register	Description	Page
0xD034	INTF_CSC_P2	CSC parameter 2 register	10-210
0xD038	INTF_CSC_P3	CSC parameter 3 register	10-210
0xD03C	INTF_CSC_P4	CSC parameter 4 register	10-211
0xD040	INTF_HSPCFG0	HSP configuration register 0	10-211
0xD044	INTF_HSPCFG1	HSP configuration register 1	10-211
0xD054	INTF_HSPCFG5	HSP configuration register 5	10-212
0xD058	INTF_HSPCFG6	HSP configuration register 6	10-212
0xD05C	INTF_HSPCFG7	HSP configuration register 7	10-213
0xD060	INTF_HSPCFG8	HSP configuration register 8	10-214
0xD070	INTF_HSPCFG12	HSP configuration register 12	10-214
0xD074	INTF_HSPCFG13	HSP configuration register 13	10-214
0xD078	INTF_HSPCFG14	HSP configuration register 14	10-215
0xD07C	INTF_HSPCFG15	HSP configuration register 15	10-216
0xF200	DATE_COEFF0	Standard parameter configuration register	10-217
0xF204	DATE_COEFF1	Amplitude configuration register	10-221
0xF208	DATE_COEFF2	DATE coefficient 2 register	10-222
0xF20C	DATE_COEFF3	DATE coefficient 3 register	10-222
0xF210	DATE_COEFF4	DATE coefficient 4 register	10-222
0xF214	DATE_COEFF5	DATE coefficient 5 register	10-223
0xF218	DATE_COEFF6	DATE coefficient 6 register	10-223
0xF254	DATE_COEFF21	Output matrix control register	10-224
0xF258	DATE_COEFF22	DTO initial phase configuration register	10-226
0xF25C	DATE_COEFF23	Video output delay configuration register	10-226
0xF260	DATE_COEFF24	ColorBurst start position register	10-228
0xF264	DATE_COEFF25	SECAM preemphasis curve input coefficient register	10-228
0xF268	DATE_COEFF26	Preemphasis curve input coefficient register	10-228

Offset Address	Register	Description	Page
0xF26C	DATE_COEFF27	SECAM preemphasis curve output coefficient register	10-229
0xF270	DATE_COEFF28	SECAM color burst start coordinate register	10-229
0xF274	DATE_COEFF29	SECAM color burst end coordinate register	10-230
0xF278	DATE_COEFF30	SECAM peak video signal level width coefficient register	10-230
0xF280	DATE_ISRMASK	Interrupt mask register	10-230
0xF284	DATE_ISRSTATE	Interrupt status register	10-231
0xF288	DATE_ISR	Interrupt register	10-231
0xF294	DATE_COEFF37	Up-sampling filtering coefficient 1 register	10-232
0xF298	DATE_COEFF38	Up-sampling filtering coefficient 2 register	10-232
0xF29C	DATE_COEFF39	Up-sampling filtering coefficient 3 register	10-233
0xF2A0	DATE_COEFF40	Up-sampling filtering coefficient 4 register	10-233
0xF2A4	DATE_COEFF41	Up-sampling filtering coefficient 5 register	10-234
0xF2A8	DATE_COEFF42	Up-sampling filtering coefficient 6 register	10-234
0xF2C0	DATE_DACDET1	DAC automatic detection register 1	10-234
0xF2C4	DATE_DACDET2	DAC automatic detection register 2	10-235
0xF2C8	DATE_COEFF50	Over-sampling filtering coefficient 1 register	10-235
0xF2CC	DATE_COEFF51	Over-sampling filtering coefficient 2 register	10-236
0xF2D0	DATE_COEFF52	Over-sampling filtering coefficient 3 register	10-236
0xF2D4	DATE_COEFF53	Over-sampling filtering coefficient 4 register	10-237
0xF2D8	DATE_COEFF54	Over-sampling filtering coefficient 5 register	10-237
0xF2DC	DATE_COEFF55	Over-sampling filtering coefficient 6 register	10-237

Offset Address	Register	Description	Page
0xF2E0	DATE_COEFF56	Over-sampling round-off register	10-238
0xF2E4	DATE_COEFF57	CVBS gain control register	10-238
0xF2E8	DATE_COEFF58	Component gain control register	10-239
0xF2EC	DATE_COEFF59	Clip control register	10-240

10.2.7 Register Description

VOCTRL

VOCTRL is a VO control register. It is used to configure the arbitration mode of surface bus requests.

Offset Address	Register Name	Total Reset Value
0x0000	VOCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_ck_gt_en	chk_sum_en	reserved																										m0_arb_mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vo_ck_gt_en	VDP clock gating enable 0: disabled 1: enabled
[30]	RW	chk_sum_en	Checksum enable 0: disabled 1: enabled
[29:4]	RO	reserved	Reserved
[3:0]	RW	m0_arb_mode	Arbitration mode of internal surface bus data requests of VO MAC0 0000: The polling mode is used. 0001: The graphics layer takes priority. Other values: reserved

VOINTSTA

VOINTSTA is a VO interrupt status register (read-only).

Offset Address	Register Name	Total Reset Value
0x0004	VOINTSTA	0x0000_0044

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	m0_be_int	reserved			g4rr_int	reserved	g2rr_int	g1rr_int	reserved	v4rr_int	v3rr_int	v1rr_int	reserved	dsd0uf_int	dsd0vtthd1_int	vdac3_unload_int	vdac2_unload_int	vdac1_unload_int	vdac0_unload_int	reserved		dwbc0_vte_int	reserved	dhd1uf_int	dhd1vtthd3_int	dhd1vtthd2_int	dhd1vtthd1_int	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RO	m0_be_int	AXI master 0 bus error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[29:27]	RO	reserved	Reserved
[26]	RO	g4rr_int	G4 register update interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RO	reserved	Reserved
[24]	RO	g2rr_int	G2 register update interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[23]	RO	g1rr_int	G1 register update interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[22]	RO	reserved	Reserved
[21]	RO	v4rr_int	V4 register update interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[20]	RO	v4rr_int	V3 register update interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[19]	RO	v3rr_int	V1 register update interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	reserved	Reserved
[17]	RO	dsd0uf_int	SD low-bandwidth alarm interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	dsd0vtthd1_int	SD vertical timing interrupt 1 0: No interrupt is generated. 1: An interrupt is generated.
[15]	RO	vdac3_unload_int	VDAC3 offload interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[14]	RO	vdac2_unload_int	VDAC2 offload interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[13]	RO	vdac1_unload_int	VDAC1 offload interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[12]	RO	vdac0_unload_int	VDAC0 offload interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[11:10]	RO	reserved	Reserved
[9]	RO	dwbc0_vte_int	DWBC0 task completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	reserved	Reserved
[7]	RO	dhd1uf_int	HD1 low-bandwidth alarm interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	dhd1vtthd3_int	HD1 vertical timing interrupt 3 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	dhd1vtthd2_int	HD1 vertical timing interrupt 2 0: No interrupt is generated. 1: An interrupt is generated.

[4]	RO	dhd1vtthd1_int	HD1 vertical timing interrupt 1 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

VOMSKINTSTA

VOMSKINTSTA is a VO masked interrupt status register. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0x0008	VOMSKINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	m0_be_clr	reserved			g4rr_clr	reserved	g2rr_clr	g1rr_clr	reserved	v4rr_clr	v3rr_clr	v1rr_clr	reserved	dsd0uf_clr	dsd0vtthd1_clr	vdac3_unload_int	vdac2_unload_int	vdac1_unload_int	vdac0_unload_int	g4wbc_vte_clr	g0wbc_vte_clr	dwbc0_vte_clr	reserved	dhd1uf_clr	dhd1vtthd3_clr	dhd1vtthd2_clr	dhd1vtthd1_clr	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	WC	m0_be_clr	AXI master 0 bus error interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[29:27]	RO	reserved	Reserved
[26]	WC	g4rr_clr	G4 register update interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[25]	RO	reserved	Reserved
[24]	WC	g2rr_clr	G2 register update interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[23]	WC	g1rr_clr	G1 register update interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[22]	RO	reserved	Reserved

[21]	WC	v4rr_clr	V4 register update interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[20]	WC	v4rr_clr	V3 register update interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[19]	WC	v3rr_clr	V1 register update interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[18]	RO	reserved	Reserved
[17]	RO	dsd0uf_clr	SD low-bandwidth alarm interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[16]	RO	dsd0vtthd1_clr	SD vertical timing interrupt 1 0: The interrupt is not cleared. 1: The interrupt is cleared.
[15]	RO	vdac3_unload_int	VDAC3 offload interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[14]	RO	vdac2_unload_int	VDAC2 offload interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[13]	RO	vdac1_unload_int	VDAC1 offload interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[12]	RO	vdac0_unload_int	VDAC0 offload interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[11]	RO	g4wbc_vte_clr	G4 WBC task completion interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[10]	RO	g0wbc_vte_clr	G0 WBC task completion interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[9]	WC	dwbc0_vte_clr	DWBC0 task completion interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.

[8]	RO	reserved	Reserved
[7]	WC	dhd1uf_clr	HD1 low-bandwidth alarm interrupt 0: The interrupt is not cleared. 1: The interrupt is cleared.
[6]	WC	dhd1vtthd3_clr	HD1 vertical timing interrupt 3 0: The interrupt is not cleared. 1: The interrupt is cleared.
[5]	WC	dhd1vtthd2_clr	HD1 vertical timing interrupt 2 0: The interrupt is not cleared. 1: The interrupt is cleared.
[4]	WC	dhd1vtthd1_clr	HD1 vertical timing interrupt 1 0: The interrupt is not cleared. 1: The interrupt is cleared.
[3:0]	RO	reserved	Reserved

VOINTMSK

VOINTMSK is a VDP interrupt mask register. It corresponds to VOINTSTA. When the corresponding bit is set to 1, the interrupt is enabled; when the corresponding bit is set to 0, the interrupt is masked.

Offset Address	Register Name	Total Reset Value
0x000C	VOINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	m0_be_intmsk	reserved			g4rr_intmsk	reserved	g2rr_intmsk	g1rr_intmsk	reserved	v4rr_intmsk	v3rr_intmsk	v1rr_intmsk	reserved	dsd0uf_intmsk	dsd0vtthd1_intmsk	vdac3_unload_intmsk	vdac2_unload_intmsk	vdac1_unload_intmsk	vdac0_unload_intmsk	g4wbc_vte_intmsk	g0wbc_vte_intmsk	dwbc0_vte_intmsk	reserved	dhd1uf_intmsk	dhd1vtthd3_intmsk	dhd1vtthd2_intmsk	dhd1vtthd1_intmsk	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	m0_be_intmsk	AXI master 0 bus error interrupt 0: masked 1: enabled

[29:27]	RO	reserved	Reserved
[26]	RW	g4rr_intmsk	G4 register update interrupt 0: masked 1: enabled
[25]	RO	reserved	Reserved
[24]	RW	g2rr_intmsk	G2 register update interrupt 0: masked 1: enabled
[23]	RW	g1rr_intmsk	G1 register update interrupt 0: masked 1: enabled
[22]	RO	reserved	Reserved
[21]	RW	v4rr_intmsk	V4 register update interrupt 0: masked 1: enabled
[20]	RW	v3rr_intmsk	V3 register update interrupt 0: masked 1: enabled
[19]	RW	v1rr_intmsk	V1 register update interrupt 0: masked 1: enabled
[18]	RO	reserved	Reserved
[17]	RO	dsd0uf_intmsk	SD low-bandwidth alarm interrupt 0: masked 1: enabled
[16]	RO	dsd0vtthd1_intmsk	SD vertical timing interrupt 1 0: masked 1: enabled
[15]	RW	vdac3_unload_intmsk	VDAC3 offload interrupt 0: masked 1: enabled
[14]	RW	vdac2_unload_intmsk	VDAC2 offload interrupt 0: masked 1: enabled
[13]	RW	vdac1_unload_intmsk	VDAC1 offload interrupt 0: masked 1: enabled

[12]	RW	vdac0_unload_intmsk	VDAC0 offload interrupt 0: masked 1: enabled
[11]	RW	g4wbc_vte_intmsk	G4 WBC task completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RW	g0wbc_vte_intmsk	G0 WBC task completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RW	dwbc0_vte_intmsk	DWBC task completion interrupt 0: masked 1: enabled
[8]	RO	reserved	Reserved
[7]	RW	dhd1uf_intmsk	HD1 low-bandwidth alarm interrupt 0: masked 1: enabled
[6]	RW	dhd1vtthd3_intmsk	HD1 vertical timing interrupt 3 0: masked 1: enabled
[5]	RW	dhd1vtthd2_intmsk	HD1 vertical timing interrupt 2 0: masked 1: enabled
[4]	RW	dhd1vtthd1_intmsk	HD1 vertical timing interrupt 1 0: masked 1: enabled
[3:0]	RO	reserved	Reserved

VDPVERSION1

VDPVERSION1 is VDP version register 1.

Offset Address	Register Name	Total Reset Value
0x0010	VDPVERSION1	0x7675_6F76

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdpversion1																															

Reset	0	1	1	1	0	1	1	0	0	1	1	1	0	1	0	1	0	1	1	0	1	1	1	1	0	1	1	1	0	1	1	0

Bits	Access	Name	Description
[31:0]	RO	vdpversion1	VDP version register 1

VDPVERSION2

VDPVERSION2 is VDP version register 2.

Offset Address	Register Name	Total Reset Value
0x0014	VDPVERSION2	0x3031_3134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdpversion2																															
Reset	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:0]	RO	vdpversion2	VDP version register 2

VOAXICTRL

VOAXICTRL is a VO AXI bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	VOAXICTRL	0x0111_0111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																m0_id_sel	reserved			m0_wr_ostd				m0_outstd_rid1				m0_outstd_rid0			
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	m0_id_sel	AXI master 0 multi-ID enable 0: disabled 1: enabled
[14:12]	RO	reserved	Reserved
[11:8]	RW	m0_wr_ostd	Write ID outstanding of AXI master 0. The value ranges from 1 to 15.

[7:4]	RW	m0_outstd_rid1	Read ID 1 outstanding of AXI master 0. The value ranges from 1 to 15.
[3:0]	RW	m0_outstd_rid0	Read ID 0 outstanding of AXI master 0. The value ranges from 1 to 15.

VO_MUX

VO_MUX is a VO interface multiplexing register.

Offset Address	Register Name	Total Reset Value
0x0100	VO_MUX	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bt1120_sel				reserved				hdmi_sel				vga_sel				reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	hdmi_sel	HDMI data select 0: reserved 1: DHD1 HDMI
[11:8]	RW	vga_sel	VGA data select 0: reserved 1: DHD1 VGA
[7:4]	RO	reserved	Reserved
[3:0]	RW	sddate_sel	SDDATE data select. The default value is 4. 4: DSD0 SDDATE Other values: reserved

VO_MUX_DAC

VO_MUX_DAC is a VO DAC interface multiplexing register.

Offset Address	Register Name	Total Reset Value
0x0104	VO_MUX_DAC	0x0000_0987

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dac3_sel				dac2_sel				dac1_sel				dac0_sel			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	dac3_sel	DAC3 output select. The default value is 0x0. 0x0: CVBS video (SDATE) 0x1: SD analog video Y/R component (SDATE) 0x2: SD analog video Cb/G component (SDATE) 0x3: SD analog video Cr/B component (SDATE) 0x4: HD analog video Y/R component (HDATE) 0x5: HD analog video Cb/G component (HDATE) 0x6: HD analog video Cr/B component (HDATE) 0x7: VGA video R component 0x8: VGA video G component 0x9: VGA video B component Other values: reserved
[11:8]	RW	dac2_sel	DAC2 output select. The default value is 0x0. 0x0: CVBS video (SDATE) 0x1: SD analog video Y/R component (SDATE) 0x2: SD analog video Cb/G component (SDATE) 0x3: SD analog video Cr/B component (SDATE) 0x4: HD analog video Y/R component (HDATE) 0x5: HD analog video Cb/G component (HDATE) 0x6: HD analog video Cr/B component (HDATE) 0x7: VGA video R component 0x8: VGA video G component 0x9: VGA video B component Other values: reserved
[7:4]	RW	dac1_sel	DAC1 output select. The default value is 0x0. 0x0: CVBS video (SDATE) 0x1: SD analog video Y/R component (SDATE) 0x2: SD analog video Cb/G component (SDATE) 0x3: SD analog video Cr/B component (SDATE) 0x4: HD analog video Y/R component (HDATE) 0x5: HD analog video Cb/G component (HDATE) 0x6: HD analog video Cr/B component (HDATE) 0x7: VGA video R component 0x8: VGA video G component 0x9: VGA video B component

[3:0]	RW	dac0_sel	DAC0 output select. The default value is 0x0. 0x0: CVBS video (SDATE) 0x1: SD analog video Y/R component (SDATE) 0x2: SD analog video Cb/G component (SDATE) 0x3: SD analog video Cr/B component (SDATE) 0x4: HD analog video Y/R component (HDATE) 0x5: HD analog video Cb/G component (HDATE) 0x6: HD analog video Cr/B component (HDATE) 0x7: VGA video R component 0x8: VGA video G component 0x9: VGA video B component

VO_MUX_TESTSYNC

VO_MUX_TESTSYNC is a VO interface test register.

Offset Address	Register Name	Total Reset Value
0x0108	VO_MUX_TESTSYNC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_test_en	reserved																											test_field	test_vsync	test_hsync	test_dv	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vo_test_en	VDP output interface test mode enable 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved
[3]	RW	test_field	Test value of the field signal
[2]	RW	test_vsync	Test value of the vsync signal
[1]	RW	test_hsync	Test value of the hsync signal
[0]	RW	test_dv	Test value of the dv signal

VO_MUX_TESTDATA

VO_MUX_TESTDATA is a VO interface test data register.

Offset Address	Register Name	Total Reset Value
0x010C	VO_MUX_TESTDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				test_data																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:0]	RW	test_data	Output data in test mode The output of DAC0−3 channels is the lower 10 bits of the register value, the output of the BT.1120 channel is the lower 16 bits of the register value, the output of the LCD channel is bits 29−22, 19−12, and 9−2 of the register, and the output of other channels is the register value. The output is in the RGB or YUV format from upper bits to lower bits.

VO_DAC_CTRL

VO_DAC_CTRL is a VO DAC control register.

Offset Address	Register Name	Total Reset Value
0x0120	VO_DAC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									envbg	pdchopper	enextref	reserved				dac_reg_rev															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	envbg	VBG reference voltage enable 0: disabled 1: enabled
[21]	RW	pdchopper	VBG chopper enable 0: enabled 1: disabled

[20]	RW	enextref	VBG output test enable 0: The internal VBG is used. The VBG is not output to the test pin. 1: The VBG is output for external tests.
[19:16]	RO	reserved	Reserved
[15:0]	RW	dac_reg_rev	The test is reserved.

VO_DAC_C_CTRL

VO_DAC_C_CTRL is a VO DAC C channel control register.

Offset Address	Register Name	Total Reset Value
0x0130	VO_DAC_C_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	endac	reserved																							dacgc					reserved		cablectr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	endac	DAC enable 0: disabled 1: enabled
[30:10]	RO	reserved	Reserved
[9:4]	RW	dacgc	DAC output amplitude control The output voltage of the DAC at full scale ranges from 0.52 V to 1.37 V. The output amplitude is adjusted in 64 phases and the adjustment precision is 1%. The formula is as follows: Ifs = 13.9 + Gain x 0.358 (mA) 000000: 0.52 V … 111111: 1.37 V
[3:2]	RO	reserved	Reserved
[1:0]	RW	cablectr	DAC VREF_CABLE reference voltage adjustment 00: normal by default 01: −10% 10: −20% 11: +10%

VO_DAC_R_CTRL

VO_DAC_R_CTRL is a VO DAC R channel control register.

Offset Address	Register Name	Total Reset Value
0x0134	VO_DAC_R_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	endac	reserved																							dacgc					reserved		cablectr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	endac	DAC enable 0: disabled 1: enabled
[30:10]	RO	reserved	Reserved
[9:4]	RW	dacgc	DAC output amplitude control The output voltage of the DAC at full scale ranges from 0.52 V to 1.37 V. The output amplitude is adjusted in 64 phases and the adjustment precision is 1%. The formula is as follows: Ifs = 13.9 + Gain x 0.358 (mA) 000000: 0.52 V … 111111: 1.37 V
[3:2]	RO	reserved	Reserved
[1:0]	RW	cablectr	DAC VREF_CABLE reference voltage adjustment 00: normal by default 01: −10% 10: −20% 11: +10%

VO_DAC_G_CTRL

VO_DAC_G_CTRL is a VO DAC G channel control register.

Offset Address	Register Name	Total Reset Value
0x0138	VO_DAC_G_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dac_en	reserved																					dacgc								reserved		cablectr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dac_en	DAC enable 0: disabled 1: enabled
[30:10]	RO	reserved	Reserved
[9:4]	RW	dacgc	DAC output amplitude control The output voltage of the DAC at full scale ranges from 0.52 V to 1.37 V. The output amplitude is adjusted in 64 phases and the adjustment precision is 1%. The formula is as follows: Ifs = 13.9 + Gain x 0.358 (mA) 000000: 0.52 V … 111111: 1.37 V
[3:2]	RO	reserved	Reserved
[1:0]	RW	cablectr	DAC VREF_CABLE reference voltage adjustment 00: normal by default 01: −10% 10: −20% 11: +10%

VO_DAC_B_CTRL

VO_DAC_B_CTRL is a VO DAC B channel control register.

Offset Address	Register Name	Total Reset Value
0x013C	VO_DAC_B_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dac_en	reserved																					dacgc						reserved		cablectr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dac_en	DAC enable 0: disabled 1: enabled
[30:10]	RO	reserved	Reserved
[9:4]	RW	dacgc	DAC output amplitude control The output voltage of the DAC at full scale ranges from 0.52 V to 1.37 V. The output amplitude is adjusted in 64 phases and the adjustment precision is 1%. The formula is as follows: Ifs = 13.9 + Gain x 0.358 (mA) 000000: 0.52 V … 111111: 1.37 V
[3:2]	RO	reserved	Reserved
[1:0]	RW	cablectr	DAC VREF_CABLE reference voltage adjustment 00: normal by default 01: −10% 10: −20% 11: +10%

GDC_CORRESP

GDC_CORRESP is a graphics layer binding relationship register.

Offset Address	Register Name	Total Reset Value
0x030C	GDC_CORRESP	0x0001_1100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				g2_corresp				reserved							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	g2_corresp	G2 binding relationship 0010: G2 is bound to CBM 1 or CBM2. 0100: G2 is bound to MIXSD, and pictures are displayed through the DSD. Other values: reserved
[7:0]	RO	reserved	Reserved

WBC_CORRESP

WBC_CORRESP is a WBC point binding relationship register.

Offset Address	Register Name	Total Reset Value
0x0310	WBC_CORRESP	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												wbc_corresp			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:0]	RW	wbc_corresp	WBC point binding relationship of WBC_DHD 0x1: WBC_DHD is bound to the output end of CBM mixer 1. 0x2: WBC_DHD is bound to the output end of CBM mixer 2. 0x10: WBC_DHD is bound to the output end of V3. Other values: reserved

COEF_DATA

COEF_DATA is a virtual coefficient register. All VDP coefficients are read from this register. The coefficients are distinguished from each other by using the PARARD read enable registers.

Offset Address	Register Name	Total Reset Value
0x0400	COEF_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_data																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	coef_data	Coefficient

V1_PARARD

V1_PARARD is a V1 coefficient read flag register.

Offset Address	Register Name	Total Reset Value
0x0414	V1_PARARD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												v1_vccoef_rd	v1_vlcoef_rd	v1_hccoef_rd	v1_hlcoef_rd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	v1_vccoef_rd	Read enable for the V1 vertical chrominance filtering coefficient 0: disabled 1: enabled
[2]	RW	v1_vlcoef_rd	Read enable for the V1 vertical luminance filtering coefficient 0: disabled 1: enabled
[1]	RW	v1_hccoef_rd	Read enable for the V1 horizontal chrominance filtering coefficient 0: disabled 1: enabled
[0]	RW	v1_hlcoef_rd	Read enable for the V1 horizontal luminance filtering coefficient 0: disabled 1: enabled

V3_PARARD

V3_PARARD is a V3 coefficient read flag register.

Offset Address	Register Name	Total Reset Value
0x041C	V3_PARARD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												v3_vccoef_rd	v3_vlcoef_rd	v3_hccoef_rd	v3_hlcoef_rd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	v3_vccoef_rd	Read enable for the V3 vertical chrominance filtering coefficient 0: disabled 1: enabled
[2]	RW	v3_vlcoef_rd	Read enable for the V3 vertical luminance filtering coefficient 0: disabled 1: enabled
[1]	RW	v3_hccoef_rd	Read enable for the V3 horizontal chrominance filtering coefficient 0: disabled 1: enabled
[0]	RW	v3_hlcoef_rd	Read enable for the V3 horizontal luminance filtering coefficient 0: disabled 1: enabled

WBCDHD_PARARD

WBCDHD_PARARD is a WBC_DHD coefficient read flag register.

Offset Address	Register Name	Total Reset Value
0x04C0	WBCDHD_PARARD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							wbcdhd_vccoef_rd	wbcdhd_vlcoef_rd	wbcdhd_hccoef_rd	wbcdhd_hlcoef_rd
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	wbcdhd_vccoef_rd	Read enable for the WBC_DHD vertical chrominance filtering coefficient 0: disabled 1: enabled
[2]	RW	wbcdhd_vlcoef_rd	Read enable for the WBC_DHD vertical luminance filtering coefficient 0: disabled 1: enabled
[1]	RW	wbcdhd_hccoef_rd	Read enable for the WBC_DHD horizontal chrominance filtering coefficient 0: disabled 1: enabled
[0]	RW	wbcdhd_hlcoef_rd	Read enable for the WBC_DHD horizontal luminance filtering coefficient 0: disabled 1: enabled

V3_CTRL

V3_CTRL is a V3 configuration register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x3800	V3_CTRL	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved			mute_en	reserved							ifir_mode		reserved		reserved		lm_rmode		chm_rmode		reserved				req_ctrl			reserved		ifmt		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register) 0: disabled 1: enabled
[30:28]	RO	reserved	Reserved
[27]	RW	mute_en	V3 mute enable (non-instant register) 0: disabled 1: enabled
[26:20]	RO	reserved	Reserved
[19:18]	RW	ifir_mode	Horizontal chrominance IFIR mode 00: reserved 01: chrominance IFIR replication mode 10: bilinear interpolation 11: 6-tap FIR
[17]	RO	reserved	Reserved
[16]	RO	reserved	Reserved
[15:14]	RW	lm_rmode	Luminance read mode 00: The read mode is bound to the interface. 01: The frame buffer data is read in progressive mode. 10: The top field is read in interlaced mode. 11: The bottom field is read in interlaced mode.
[13:12]	RW	chm_rmode	Chrominance read mode 00: The read mode is bound to the interface. 01: The frame buffer data is read in progressive mode. 10: The top field is read in interlaced mode. 11: The bottom field is read in interlaced mode.
[11:8]	RO	reserved	Reserved

[7:5]	RW	req_ctrl	Register for controlling the number of 16-burst requested consecutively at a time 0x0: One 16-burst is requested consecutively at a time. 0x1: Two 16-burst are requested consecutively at a time. Other values: reserved
[4]	RO	reserved	Reserved
[3:0]	RW	ifmt	Format of the input data 0x3: SPYCbCr420 0x4: SPYCbCr422 Other values: reserved

V3_UPD

V3_UPD is a V3 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x3804	V3_UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WC	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is automatically cleared by the hardware.

V3_PRERD

V3_PRERD is a V3 prefetch enable register.

Offset Address	Register Name	Total Reset Value
0x3820	V3_PRERD	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pre_rd_en	reserved																														
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	pre_rd_en	V3 prefetch enable 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

V3_IRESO

V3_IRESO is a V3 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x3828	V3_IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. The frame height is referenced and the unit is line.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1.

V3_ORESO

V3_ORESO is a V3 output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x382C	V3_ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. The frame height is referenced and the unit is line.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1.

V3_CBMPARA

V3_CBMPARA is a V3 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x3838	V3_CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 128. The value 128 indicates opaque, and the value 0 indicates full transparent.

V3_PARAUP

V3_PARAUP is a V3 coefficient-related register update enable register. The VDP scaling coefficients are configured by using the AXI master. Software configures the start addresses and parameter update flags by using the slave.

Offset Address	Register Name	Total Reset Value
0x3840	V3_PARAUP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												v3_vccoef_upd	v3_vlcoef_upd	v3_hccoef_upd	v3_hlcoef_upd
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	v3_vccoef_upd	Whether the V3 vertical chrominance filtering coefficients need to be updated. This bit is automatically cleared after the hardware updates the coefficients. 0: not updated 1: updated
[2]	WO	v3_vlcoef_upd	Whether the V3 vertical luminance filtering coefficients need to be updated. This bit is automatically cleared after the hardware updates the coefficients. 0: not updated 1: updated
[1]	WO	v3_hccoef_upd	Whether the V3 horizontal chrominance filtering coefficients need to be updated. This bit is automatically cleared after the hardware updates the coefficients. 0: not updated 1: updated
[0]	WO	v3_hlcoef_upd	Whether the V3 horizontal luminance filtering coefficients need to be updated. This bit is automatically cleared after the hardware updates the coefficients. 0: not updated 1: updated

V3_HLCOEFAD

V3_HLCOEFAD is a V3 horizontal luminance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0x3850	V3_HLCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address for storing coefficients in the local memory

V3_HCCOEFAD

V3_HCCOEFAD is a V3 horizontal chrominance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0x3854	V3_HCCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address for storing coefficients in the local memory

V3_VLCOEFAD

V3_VLCOEFAD is a V3 vertical luminance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0x3858	V3_VLCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address for storing coefficients in the local memory

V3_VCCOEFAD

V3_VCCOEFAD is a V3 vertical chrominance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0x385C	V3_VCCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address for storing coefficients in the local memory

V3_CSC_IDC

V3_CSC_IDC is a V3 CSC input DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x3880	V3_CSC_IDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									csc_en	cscidc1														cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_en	CSC enable 0: disabled 1: enabled
[21:11]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as a complement.

V3_CSC_ODC

V3_CSC_ODC is a V3 CSC output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x3884	V3_CSC_ODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		csc_sign_mode	cscodc1		cscodc0		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_sign_mode	CSC output mode 0: The CSC output is a 10-bit unsigned number. 1: The CSC output is a 12-bit signed number.
[21:11]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as a complement.

V3_CSC_IODC

V3_CSC_IODC is a CSC input/output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x3888	V3_CSC_IODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cscodc2		cscidc2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:11]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as a complement.

V3_CSC_P0

V3_CSC_P0 is a CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x388C	V3_CSC_P0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp01	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp00	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

V3_CSC_P1

V3_CSC_P1 is a CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x3890	V3_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp10	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp02	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

V3_CSC_P2

V3_CSC_P2 is a CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x3894	V3_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp12	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp11	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

V3_CSC_P3

V3_CSC_P3 is a CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x3898	V3_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp21	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved

[14:0]	RW	cscp20	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

V3_CSC_P4

V3_CSC_P4 is a CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x389C	V3_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cscp22															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:0]	RW	cscp22	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

V3_HSP

V3_HSP is a V3 horizontal scaling parameter register (non-instant register).

Scaling ratio = Input width/Output width

Offset Address	Register Name	Total Reset Value
0x38C0	V3_HSP	0x0010_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hlmsc_en	hchmsc_en	hlmid_en	hchmid_en	non_lnr_en	hlfir_en	hchfir_en	hfir_order	hratio																							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hlmsc_en	Horizontal luminance scaling enable 0: disabled 1: enabled
[30]	RW	hchmsc_en	Horizontal chrominance scaling enable 0: disabled 1: enabled

[29]	RW	hlmid_en	Median filtering enable for horizontal luminance scaling. This bit is invalid when hlfir_en is invalid. 0: disabled 1: enabled
[28]	RW	hchmid_en	Median filtering enable for horizontal chrominance scaling. This bit is invalid when hchfir_en is invalid. 0: disabled 1: enabled
[27]	RW	non_lnr_en	Non-linear scaling enable 0: disabled 1: enabled
[26]	RW	hlfir_en	Horizontal luminance scaling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[25]	RW	hchfir_en	Horizontal chrominance scaling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[24]	RW	hfir_order	Horizontal scaling sequence 0: Horizontal scaling is performed before vertical scaling. 1: Horizontal scaling is performed after vertical scaling.
[23:0]	RW	hratio	Horizontal scaling ratio, in (u, 4, 20) format

V3_HLOFFSET

V3_HLOFFSET is a V3 horizontal luminance offset register (non-instant register). It is used for pan-scan.

Offset Address	Register Name	Total Reset Value
0x38C4	V3_HLOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hor_loffset																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	hor_loffset	Horizontal luminance offset, in (s, 8, 20) format. The value is expressed as a complement.

V3_HCOFFSET

V3_HCOFFSET is a V3 horizontal chrominance offset register (non-instant register). It is used for pan-scan.

Offset Address	Register Name	Total Reset Value
0x38C8	V3_HCOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hor_coffset																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	hor_coffset	Horizontal chrominance offset, in (s, 8, 20) format. The value is expressed as a complement.

V3_VSP

V3_VSP is a V3 vertical scaling parameter register.

Offset Address	Register Name	Total Reset Value
0x38D8	V3_VSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vlmsc_en	vchmsc_en	vlmid_en	vchmid_en	reserved	vsc_chroma_tap	reserved	vlfir_en	vchfir_en	zme_out_fmt		zme_in_fmt	reserved																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vlmsc_en	Vertical luminance scaling enable 0: disabled 1: enabled
[30]	RW	vchmsc_en	Vertical chrominance scaling enable 0: disabled 1: enabled

[29]	RW	vlmid_en	Median filtering enable for vertical luminance scaling. This bit is invalid when vlfir_en is invalid. 0: disabled 1: enabled
[28]	RW	vchmid_en	Median filtering enable for vertical chrominance scaling. This bit is invalid when vchfir_en is invalid. 0: disabled 1: enabled
[27]	RO	reserved	Reserved
[26]	RW	vsc_chroma_tap	Vertical chrominance scaling tap 0: 4-tap FIR 1: 2-tap FIR
[25]	RO	reserved	Reserved
[24]	RW	vlfir_en	Vertical luminance scaling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[23]	RW	vchfir_en	Vertical chrominance scaling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[22:21]	RW	zme_out_fmt	Output data format for scaling 0: 422 1: 420
[20:19]	RW	zme_in_fmt	Input data format for scaling 0: 422 1: 420
[18:0]	RO	reserved	Reserved

V3_VSR

V3_VSR is a vertical luminance scaling ratio register (non-instant register).

Scaling ratio = Input height/Output height

Offset Address	Register Name	Total Reset Value
0x38DC	V3_VSR	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vratio															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vratio	Vertical scaling ratio, in (u, 4, 12) format

V3_VOFFSET

V3_VOFFSET is a V3 vertical luminance scaling offset register. The vertical scaling offset is affected by the field offset during pan-scan and the field offset when repeated frames occur. If no field offset occurs, vluma_offset is the lowest integral part plus the decimal part of offset_pan-scan. In YCbCr422 format, vchroma_offset is equal to vluma_offset; in YCbCr420 format, vchroma_offset is calculated as follows: vchroma_offset = scaling_chroma/2 – 0.25. If the field offset is required (such as static frames or repeated frames) and the bottom field is repeated, the values of vluma_offset and vchroma_offset configured for the top field are the same as those in the case of no field offset. The field offset must be considered when coefficients are configured for the bottom field.

Offset Address	Register Name	Total Reset Value
0x38E0	V3_VOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vluma_offset																vchroma_offset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	vluma_offset	Vertical luminance offset, in (s, 4, 12) format. The value is expressed as a complement.
[15:0]	RW	vchroma_offset	Vertical chrominance offset, in (s, 4, 12) format. The value is expressed as a complement.

V3_VBOFFSET

V3_VBOFFSET is a V3 vertical luminance scaling offset register for the bottom field. The vertical scaling offset is affected by the field offset during pan-scan and the field offset when repeated frames occur. If no field offset occurs, vluma_offset is the lowest integral part plus the decimal part of offset_pan-scan. In YCbCr422 format, vchroma_offset is equal to vluma_offset; in YCbCr420 format, vchroma_offset is calculated as follows: vchroma_offset = scaling_chroma/2 – 0.25. If the field offset is required (such as static frames or repeated frames) and the bottom field is repeated, the values of vluma_offset and vchroma_offset

configured for the top field are the same as those in the case of no field offset. The field offset must be considered when coefficients are configured for the bottom field.

Offset Address	Register Name	Total Reset Value
0x38E4	V3_VBOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vbluma_offset																vbchroma_offset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	vbluma_offset	Vertical luminance offset, in (s, 4, 12) format. The value is expressed as a complement.
[15:0]	RW	vbchroma_offset	Vertical chrominance offset, in (s, 4, 12) format. The value is expressed as a complement.

V3_DFPOS

V3_DFPOS is a V3 surface start position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x3900	V3_DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_yfpos	Start coordinates of the display column The frame height is referenced and the unit is line.
[11:0]	RW	disp_xfpos	Start coordinates of the display row

V3_DLPOS

V3_DLPOS is a V3 surface end position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x3904	V3_DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_ylpos	End coordinates of the display column The frame height is referenced and the unit is line.
[11:0]	RW	disp_xlpos	End coordinates of the display row

V3_VFPOS

V3_VFPOS is a V3 surface content start position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x3908	V3_VFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_yfpos												video_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	video_yfpos	Start coordinates of the video column The frame height is referenced and the unit is line.
[11:0]	RW	video_xfpos	Start coordinates of the video row

V3_VLPOS

V3_VLPOS is a V3 surface content end position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x390C	V3_VLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_ylpos												video_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	video_ylpos	End coordinates of the video column The frame height is referenced and the unit is line.
[11:0]	RW	video_xlpos	End coordinates of the video row

V3_BK

V3_BK is a V3 background color register.

Offset Address	Register Name	Total Reset Value
0x3910	V3_BK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vbk_y								vbk_cb								vbk_cr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	vbk_y	Y component
[19:10]	RW	vbk_cb	Cb component
[9:0]	RW	vbk_cr	Cr component

V3_ALPHA

V3_ALPHA is a V3 background filling color alpha register.

Offset Address	Register Name	Total Reset Value
0x3914	V3_ALPHA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								vbk_alpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	vbk_alpha	Levels 0−255 of the background filling color for the video layer

V3_RIMWIDTH

V3_RIMWIDTH is a V3 RIM width register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x3918	V3_RIMWIDTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														v0_rim_width	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved
[2:0]	RW	v0_rim_width	Thickness of all the region borders 00: The border width is 0. 01: The border width is 1. 10: The border width is 2. 11: The border width is 4.

V3_RIMCOL0

V3_RIMCOL0 is a RIM color 0 register (non-instant register) for the upper 32 regions at the V3 video layer.

Offset Address	Register Name	Total Reset Value
0x391C	V3_RIMCOL0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				v0_rim_y0								v0_rim_u0								v0_rim_v0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved
[29:20]	RW	v0_rim_y0	RIM color 0, R component
[19:10]	RW	v0_rim_u0	RIM color 0, G component
[9:0]	RW	v0_rim_v0	RIM color 0, B component

V3_RIMCOL1

V3_RIMCOL1 is a RIM color 1 register (non-instant register) for the upper 32 regions at the V3 video layer.

Offset Address	Register Name	Total Reset Value
0x3920	V3_RIMCOL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				v0_rim_y1								v0_rim_u1								v0_rim_v1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	reserved	Reserved
[29:20]	RW	v0_rim_y1	RIM color 1, R component
[19:10]	RW	v0_rim_u1	RIM color 1, G component
[9:0]	RW	v0_rim_v1	RIM color 1, B component

V3_IFIRCOEF01

V3_IFIRCOEF01 is an IFIR filtering coefficient 0/1 register.

Offset Address	Register Name	Total Reset Value
0x3980	V3_IFIRCOEF01	0x000F_03F5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef1								reserved								coef0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	coef1	IFIR filtering coefficient 1
[15:10]	RO	reserved	Reserved
[9:0]	RW	coef0	IFIR filtering coefficient 0

V3_IFIRCOEF23

V3_IFIRCOEF23 is an IFIR filtering coefficient 2/3 register.

Offset Address	Register Name	Total Reset Value
0x3984	V3_IFIRCOEF23	0x001C_03EC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef3								reserved								coef2							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	coef3	IFIR filtering coefficient 3
[15:10]	RO	reserved	Reserved
[9:0]	RW	coef2	IFIR filtering coefficient 2

V3_IFIRCOEF45

V3_IFIRCOEF45 is an IFIR filtering coefficient 4/5 register.

Offset Address	Register Name	Total Reset Value
0x3988	V3_IFIRCOEF45	0x003D_03D8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef5								reserved								coef4							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	coef5	IFIR filtering coefficient 5
[15:10]	RO	reserved	Reserved
[9:0]	RW	coef4	IFIR filtering coefficient 4

V3_IFIRCOEF67

V3_IFIRCOEF67 is an IFIR filtering coefficient 6/7 register.

Offset Address	Register Name	Total Reset Value
0x398C	V3_IFIRCOEF67	0x014A_0395

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef7								reserved								coef6							
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1	1	0	0	1	0	1	0	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	coef7	IFIR filtering coefficient 7
[15:10]	RO	reserved	Reserved
[9:0]	RW	coef6	IFIR filtering coefficient 6

V3_P0RESO

V3_P0RESO is V3 region 0 resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x3A00	V3_P0RESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				w											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved
[11:0]	RW	w	Width (in pixel). The value is the actual width minus 1. Note: The actual width must be an even number.

V3_P0LADDR

V3_P0LADDR is a V3 region 0 luminance address register.

Offset Address	Register Name	Total Reset Value
0x3A04	V3_P0LADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Luminance start address for VHD region 0

V3_P0CADDR

V3_P0CADDR is a V3 region 0 chrominance address register.

Offset Address	Register Name	Total Reset Value
0x3A08	V3_P0CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Chrominance start address for VHD region 0

V3_P0STRIDE

V3_P0STRIDE is a V3 region 0 stride register.

Offset Address	Register Name	Total Reset Value
0x3A0C	V3_P0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance buffer of VHD region 0 (valid in semi-planar format), 128-bit alignment
[15:0]	RW	surface_stride	Luminance stride of the luminance buffer of VHD region 0 (valid in semi-planar format), 128-bit alignment

V3_P0VFPOS

V3_P0VFPOS is a video content start position (in the display window) register (non-instant) for V3 region 0. The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x3A10	V3_P0VFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_yfpos												video_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved
[23:12]	RW	video_yfpos	Start coordinates of the video column The frame height is referenced and the unit is line.
[11:0]	RW	video_xfpos	Start coordinates of the video row

V3_P0VLPOS

V3_P0VLPOS is a video content end position (in the display window) register (non-instant) for V3 region 0. The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x3A14	V3_P0VLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								video_ylpos												video_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved
[23:12]	RW	video_ylpos	End coordinates of the video column The frame height is referenced and the unit is line.
[11:0]	RW	video_xlpos	End coordinates of the video row

V3_P0CTRL

V3_P0CTRL is a V3 region 0 control register.

Offset Address	Register Name	Total Reset Value
0x3A18	V3_P0CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mute_en	p0_en	p0_dcmp_en	p0_l_loss_en	p0_c_loss_en	p0_rim_en	p0_rim_col_mod	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RW	reserved	Reserved
[6]	RW	mute_en	Region 0 mute enable 0: disabled 1: enabled
[5]	RW	p0_en	Region 0 enable 0: disabled 1: enabled
[4]	RW	p0_dcmp_en	Region 0 decompression enable 0: disabled 1: enabled

[3]	RW	p0_l_loss_en	Region 0 l_loss enable 0: disabled 1: enabled
[2]	RW	p0_c_loss_en	Region 0 c_loss enable 0: disabled 1: enabled
[1]	RW	p0_rim_en	Region 0 rim enable 0: disabled 1: enabled
[0]	RW	p0_rim_col_mod	Region 0 rim_mod select 0: color 0 1: color 1

V3_MULTI_MODE

V3_MULTI_MODE is a multi-region mode enable register. This register must be enabled when there are multiple regions.

Offset Address	Register Name	Total Reset Value
0x4230	V3_MULTI_MODE	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								mrg_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	1

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	mrg_mode	Multi-region mode enable (valid only for V1 or V4) 0: single-region mode (with LBOX) 1: multi-region mode (without LBOX)

V3_FDRFIFOTHD

V3_FDRFIFOTHD is a V3 FDR FIFO threshold register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x4250	V0_FDRFIFOTHD	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						ff_thd									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	ff_thd	FDR FIFO threshold. The minimum value is 32. The value must be 2 to the power of n.

V3_MRGERRCLR

V3_MRGERRCLR is a V3 multi-region register operation error status clear register. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0x4350	V3_MRGERRCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mrg_errclr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	mrg_errclr	VO multi-region register operation error status clear register 0: not cleared 1: cleared

V3_MRG_ERR

V3_MRG_ERR is a V3 multi-region register operation error signal register.

Offset Address	Register Name	Total Reset Value
0x4354	V3_MRG_ERR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								mrg_wrong
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	mrg_wrong	V3 multi-region register operation error signal register 0: The multi-region register operation is correct. 1: The multi-region register operation is incorrect.

G4_CTRL

G4_CTRL is a G4 configuration register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x8000	G4_CTRL	0x4000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19 18 17 16	15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 0
Name	surface_en	reserved	reserved	reserved	upd_mode	read_mode	dcmp_en	reserved	lossless	lossless_a	cmp_mode		reserved	req_ctrl	reserved	bitext	ifmt	
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0 0 0 0	0 0 0 0	0 0	0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant register) 0: disabled 1: enabled
[30]	RO	reserved	Reserved
[29]	RO	reserved	Reserved
[28]	RO	reserved	Reserved
[27]	RW	upd_mode	Update mode 0: update by frame 1: update by field

[26]	RW	read_mode	Data read mode 0: The read mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 1: The progressive read mode is selected forcibly.
[25]	RW	dcmp_en	Decompression enable 0: disabled 1: enabled
[24]	RO	reserved	Reserved
[23]	RW	lossless	Compression mode select 0: lossy compression 1: lossless compression
[22]	RW	lossless_a	Compression mode select for a 0: lossy compression of a 1: lossless compression of a
[21]	RW	cmp_mode	Compressed data type 1: RAM mode 0: compression mode
[20:15]	RO	reserved	Reserved
[14:12]	RW	req_ctrl	Register for controlling the number of 16-burst requested consecutively at a time 0x0: One 16-burst is requested consecutively at a time. 0x1: Two 16-burst are requested consecutively at a time. 0x2: Four 16-burst are requested consecutively at a time. 0x3: Eight 16-burst are requested consecutively at a time. Other values: reserved
[11:10]	RO	reserved	Reserved
[9:8]	RW	bitext	Bit extend mode of the input bitmap 00: extend 0s to lower bits 01: reserved 10: extend the value of the MSB to a lower bit 11: extend the values of upper bits to lower bits
[7:0]	RW	ifmt	Format of the input data 0x49: ARGB1555 0x68: ARGB8888 Other values: reserved

G4_UPD

G4_UPD is a G4 update enable register.

Offset Address	Register Name	Total Reset Value
0x8004	G4_UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is automatically cleared by the hardware.

G4_ADDR

G4_ADDR is a G4 address register. When the horizontal pixel offsets, you need to calculate the address by following the description of G4_SFPOS.

Offset Address	Register Name	Total Reset Value
0x8010	G4_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Address for the surface frame buffer

G4_STRIDE

G4_STRIDE is a G4 stride register.

Offset Address	Register Name	Total Reset Value
0x801C	G4_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	surface_stride	Frame buffer stride

G4_IRESO

G4_IRESO is a G4 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x8020	G4_IRESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ih												iw											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	ih	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	iw	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

G4_SFPOS

G4_SFPOS is a G4 surface read data start position (in the source bitmap) register (non-instant register). If the read position is not 128-bit-word-aligned, this register indicates the number of pixels required for completing a 128-bit word. Note: The start position offset must be less than or equal to a 128-bit word. The exceeded part is expressed by an address.

The details are as follows:

The following assumes that the start address for the graphics layer of the source picture is addr_ori, the address configured for the logical graphics layer is addr_offset, the graphics layer offset is offsetp (in pixel), and the data format at the graphics layer is bpp (for example, the bpp for ARGB8888 is 32). The formulas are as follows:

G4ADDR = addr_offset = addr_ori + int (offset x bpp/128)

G4SFPOS = offset%128

where int indicates the rounding operation, and % indicates the modulo operation.

Offset Address	Register Name	Total Reset Value
0x8024	G4_SFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								src_xfpos							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:0]	RW	src_xfpos	Start horizontal coordinate of the source picture. The value 0 indicates the first pixel of a line.

G4_CBMPARA

G4_CBMPARA is a G4 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x8030	G4_CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_mode	key_en	premult_en	palpha_en	reserved	reserved	reserved	palpha_range	galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	key_mode	Colorkey mode 0: The color is regarded as the colorkey when the following condition is met: Keymin ≤ Pixel ≤ Keymax 1: The color is regarded as the colorkey when either of the following conditions is met: Pixel ≤ Keymin or Pixel ≥ Keymax
[14]	RW	key_en	Colorkey enable 0: disabled 1: enabled

[13]	RW	premult_en	Whether the input bitmap is a premultiplied bitmap 0: non-premultiplied bitmap 1: premultiplied bitmap
[12]	RW	palpha_en	Pixel alpha enable 0: disabled 1: enabled
[11]	RO	reserved	Reserved
[10]	RO	reserved	Reserved
[9]	RO	reserved	Reserved
[8]	RW	palpha_range	Pixel alpha range selection 0: The pixel alpha range is 0−128. 1: The pixel alpha range is 0−255.
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 128. The value 128 indicates opaque, and the value 0 indicates full transparent.

G4_CKEYMAX

G4_CKEYMAX is a G4 maximum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x8034	G4_CKEYMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	va0								keyr_max								keyg_max								keyb_max							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	va0	Alpha0 value. When the data format is alphaRGB1555 and the alpha value is 0, the alpha0 value is used.
[23:16]	RW	keyr_max	Maximum value of the colorkey R component
[15:8]	RW	keyg_max	Maximum value of the colorkey G component
[7:0]	RW	keyb_max	Maximum value of the colorkey B component

G4_CKEYMIN

G4_CKEYMIN is a G4 minimum colorkey register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x8038	G4_CKEYMIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	va1		keyr_min		keyg_min		keyb_min	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	va1	Alpha1 value. When the data format is alphaRGB1555 and the alpha value is 1, the alpha1 value is used.
[23:16]	RW	keyr_min	Minimum value of the colorkey R component
[15:8]	RW	keyg_min	Minimum value of the colorkey G component
[7:0]	RW	keyb_min	Minimum value of the colorkey B component

G4_CMASK

G4_CMASK is a G4 masked colorkey register (non-instant register). The value 1 indicates that the bit corresponding to a pixel is retained during colorkey comparison; the value 0 indicates that the bit corresponding to a pixel is forcibly set to 0 during color comparison no matter whether the bit is 0 or 1.

Offset Address	Register Name	Total Reset Value
0x803C	G4_CMASK	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		kmsk_r		kmsk_g		kmsk_b	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	kmsk_r	R component of the masked colorkey
[15:8]	RW	kmsk_g	G component of the masked colorkey
[7:0]	RW	kmsk_b	B component of the masked colorkey

G4_FIFOTHD

G4_FIFOTHD is a G4 buffer threshold register.

Offset Address	Register Name	Total Reset Value
0x8048	G4_FIFOTHD	0x8000_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						buf_wr_thd									
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	buf_wr_thd	Buffer threshold

G4_DCMP_DBG

G4_DCMP_DBG is a debugging signal register for the DCMP module.

Offset Address	Register Name	Total Reset Value
0x8060	G4_DCMP_DBG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcmp_dbg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dcmp_dbg	Status information about the DCMP module. The initial value can be changed.

G4_DCMP_INTER

G0_DCMP_INTER is an error interrupt information register for the DCMP module.

Offset Address	Register Name	Total Reset Value
0x8070	G4_DCMP_INTER	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								gdccerrclr
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WC	gdccerrclr	This interrupt register indicates whether the output of the DCMP module is correct. If an error occurs, the bit is 1. Writing 1 clears the interrupt.

G4_DFPOS

G4_DFPOS is a G4 surface start position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x8080	G4_DFPOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved				disp_yfpos				disp_xfpos
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_yfpos	Column start coordinates
[11:0]	RW	disp_xfpos	Row start coordinates

G4_DLPOS

G4_DLPOS is a G4 surface end position (in the display window) register (non-instant register). The position unit is pixel.

Offset Address	Register Name	Total Reset Value
0x8084	G4_DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_ylpos	Column end coordinates
[11:0]	RW	disp_xlpos	Row end coordinates

G4_CSC_IDC

G4_CSC_IDC is a G4 CSC input DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x80C0	G4_CSC_IDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						csc_mode		csc_en	cscidc1											cscidc0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:23]	RW	csc_mode	This field is valid only when the G2 CSC coefficients are fixed. 000: reserved 001: YUV2YUV 010: YUV601_RGB 011: YUV709_RGB 100: YUV2YUV_709_601 101: YUV2YUV_601_709 110: RGB2YUV_601 111: RGB2YUV_709
[22]	RW	csc_en	CSC enable 0: disabled 1: enabled

[21:11]	RW	cscidc1	DC parameter of input component 1. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscidc0	DC parameter of input component 0. The MSB is the signed bit. The value is expressed as a complement.

G4_CSC_ODC

G4_CSC_ODC is a G4 CSC output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x80C4	G4_CSC_ODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									csc_sign_mode	cscodc1														cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_sign_mode	CSC output mode 0: The CSC output is a 10-bit unsigned number. 1: The CSC output is a 12-bit signed number.
[21:11]	RW	cscodc1	DC parameter of output component 1. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscodc0	DC parameter of output component 0. The MSB is the signed bit. The value is expressed as a complement.

G4_CSC_IODC

G4_CSC_IODC is a G4 CSC input/output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x80C8	G4_CSC_IODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cscodc2		cscidc2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:11]	RW	cscodc2	DC parameter of output component 2. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscidc2	DC parameter of input component 2. The MSB is the signed bit. The value is expressed as a complement.

G4_CSC_P0

G4_CSC_P0 is a G4 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x80CC	G4_CSC_P0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	cscp01			reserved	cscp00		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp01	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp00	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

G4_CSC_P1

G4_CSC_P1 is a G4 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x80D0	G4_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp10															reserved	cscp02														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp10	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp02	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

G4_CSC_P2

G4_CSC_P2 is a G4 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x80D4	G4_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp12															reserved	cscp11														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp12	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp11	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

G4_CSC_P3

G4_CSC_P3 is a G4 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x80D8	G4_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp21															reserved	cscp20														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp21	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp20	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

G4_CSC_P4

G4_CSC_P4 is a G4 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x80DC	G4_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:0]	RW	cscp22	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

WBC_G4_CTRL

WBC_G4_CTRL is a WBC0 control register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xA400	WBC_G4_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbc_en	reserved																				auto_stop_en	reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wbc_en	WBC enable 0: disable 1: enable
[30:11]	RO	reserved	Reserved
[10]	RW	auto_stop_en	When the bandwidth is low due to the rapid WBC, WBC is automatically disabled.
[9:0]	RO	reserved	Reserved

WBC_G4_UPD

WBC_G4_UPD is a WBC0 channel update enable register.

Offset Address	Register Name	Total Reset Value
0xA404	WBC_G4_UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WC	regup	Capture register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is automatically cleared by the hardware.

WBC_G4_ADDR

WBC_G4_ADDR is a capture luminance write address register.

Offset Address	Register Name	Total Reset Value
0xA410	WBC_G4_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbcaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wbcaddr	Start address for compressing the WBC data

WBC_G4_STRIDE

WBC_G4_STRIDE is a capture stride register.

Offset Address	Register Name	Total Reset Value
0xA418	WBC_G4_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																wbcstride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	wbcstride	Frame buffer stride, 16-byte-aligned

WBC_G4_ORESO

WBC_G4_ORESO is an output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xA420	WBC_G4_ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

WBC_G4_YCROP

WBC_G4_YCROP is an input picture crop start/end vertical coordinate register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xA424	WBC_G4_YCROP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ylcrop												yfcrop											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	ylcrop	End vertical coordinate for cropping
[11:0]	RW	yfcrop	Start vertical coordinate for cropping

WBC_G4_CSTR_ERR

WBC_G4_CSTR_ERR is a compressed picture stride configuration error status register. This register is read-only.

Offset Address	Register Name	Total Reset Value
0xA434	WBC_G4_CSTR_ERR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								str_err_flag
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	str_err_flag	When the configured stride length is less than the length of the header information, str_err_flag is pulled up.

WBC_G4_CLR_CSTR_ERR

WBC_G4_CLR_CSTR_ERR is a compressed picture stride configuration error status clear register. This register is write-only.

Offset Address	Register Name	Total Reset Value
0xA438	WBC_G4_CLR_CSTR_ERR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								clr_err_flag
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	clr_err_flag	Compressed picture stride configuration error status clear register Writing 1 clears the compressed picture stride configuration error status register (WBC_G4_CSTR_ERR).

WBC_G4_GLB_INFO

WBC_G4_GLB_INFO is a LCMP global control information register.

Offset Address	Register Name	Total Reset Value
0xA480	WBC_G4_GLB_INFO	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								part_num			partition_en	osd_mode		cmp_mode	is_lossless_alpha	is_lossless
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8:6]	RW	part_num	Number of split partitions
[5]	RW	partition_en	Whether to split compression 0: no spit 1: split
[4:3]	RW	osd_mode	OSD mode 0: 8888 2: 1555 Other values: reserved
[2]	RW	cmp_mode	Compression mode 0: compression 1: RAW mode
[1]	RW	is_lossless_alpha	Whether the compression mode of alpha is lossless compression 0: lossy compression 1: lossless compression
[0]	RW	is_lossless	Whether the compression mode is lossless compression mode 0: lossy compression mode 1: lossless compression mode

WBC_G4_FRAME_SIZE

WBC_G4_FRAME_SIZE is a picture size register.

Offset Address	Register Name	Total Reset Value
0xA484	WBC_G4_FRAME_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				frame_height												reserved				frame_width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	frame_height	Height (in line). The configured value is the actual height minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	frame_width	Width (in pixel). The configured value is the actual width minus 1.

WBC_G4_RC_CFG0

WBC_G4_RC_CFG0 is an RC parameter 0 register.

Offset Address	Register Name	Total Reset Value
0xA488	WBC_G4_RC_CFG0	0x0177_01F4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								min_mb_bits								reserved								budget_bits_mb							
Reset	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	min_mb_bits	Minimum number of bits that can be allocated during rate control
[15:10]	RW	reserved	Reserved
[9:0]	RW	budget_bits_mb	Number of rated bits for an RC unit

WBC_G4_RC_CFG1

WBC_G4_RC_CFG1 is an RC parameter 1 register.

Offset Address	Register Name	Total Reset Value
0xA48C	WBC_G4_RC_CFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						budget_bits_mb_cap									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	budget_bits_mb_cap	Number of rated bits for an RC unit

WBC_G4_RC_CFG2

WBC_G4_RC_CFG2 is an RC parameter 2 register.

Offset Address	Register Name	Total Reset Value
0xA490	WBC_G4_RC_CFG2	0x0404_0A25

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				special_bit_gain				reserved				rc_smth_ngain				reserved				sad_bits_ngain				smth_qp				max_qp			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	special_bit_gain	Gain coefficient of special bits
[23:19]	RO	reserved	Reserved
[18:16]	RW	rc_smth_ngain	Steady factor of the RC quality and bandwidth
[15:12]	RO	reserved	Reserved
[11:8]	RW	sad_bits_ngain	Number of allocated bits corresponding to the complexity
[7:4]	RW	smth_qp	Reserved
[3:0]	RW	max_qp	Maximum quantization level

WBC_G4_RC_CFG3

WBC_G4_RC_CFG3 is an RC parameter 3 register.

Offset Address	Register Name	Total Reset Value
0xA494	WBC_G4_RC_CFG3	0x000C_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												min_sad_thr				reserved								max_sad_thr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22:16]	RW	min_sad_thr	Minimum SAD threshold
[15:7]	RO	reserved	Reserved
[6:0]	RW	max_sad_thr	Maximum SAD threshold

WBC_G4_RC_CFG4

WBC_G4_RC_CFG4 is an RC parameter 4 register.

Offset Address	Register Name	Total Reset Value
0xA498	WBC_G4_RC_CFG4	0x0010_0103

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								big_grad_thr								reserved	still_thr							reserved	smth_thr						
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	big_grad_thr	Large gradient threshold
[15]	RO	reserved	Reserved
[14:8]	RW	still_thr	Static region threshold
[7]	RO	reserved	Reserved
[6:0]	RW	smth_thr	Smooth region threshold

WBC_G4_RC_CFG5

WBC_G4_RC_CFG5 is an RC parameter 5 register.

Offset Address	Register Name	Total Reset Value
0xA49C	WBC_G4_RC_CFG5	0x0A18_0306

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	large_smth_pix_num_thr	reserved	noise_pix_num_thr	reserved	still_pix_num_thr	reserved	smth_pix_num_thr
Reset	0 0 0 0	1 0 1 0	0 0 0 1	1 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 1 1 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:24]	RW	large_smth_pix_num_thr	Threshold for determining whether a region is a large smooth region
[23:22]	RO	reserved	Reserved
[21:16]	RW	noise_pix_num_thr	Threshold for determining whether a region is a noise region
[15:14]	RO	reserved	Reserved
[13:8]	RW	still_pix_num_thr	Threshold for determining whether a region is a static region
[7:6]	RO	reserved	Reserved
[5:0]	RW	smth_pix_num_thr	Threshold for determining whether a region is a smooth region

WBC_G4_RC_CFG6

WBC_G4_RC_CFG6 is an RC parameter 6 register.

Offset Address	Register Name	Total Reset Value
0xA4A0	WBC_G4_RC_CFG6	0x0032_0020

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		pix_diff_thr		reserved		noise_sad	
Reset	0 0 0 0	0 0 0 0	0 0 1 1	0 0 1 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	pix_diff_thr	Difference threshold
[15:7]	RO	reserved	Reserved
[6:0]	RW	noise_sad	SAD of the noise region

WBC_G4_RC_CFG7

WBC_G4_RC_CFG7 is an RC parameter 7 register.

Offset Address	Register Name	Total Reset Value
0xA4A4	WBC_G4_RC_CFG7	0x0000_0A1E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																max_trow_bits								reserved	adj_sad_bits_thr						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	max_trow_bits	Maximum number of bits in the previous row
[7]	RO	reserved	Reserved
[6:0]	RW	adj_sad_bits_thr	Number of adjusted bits for SAD

WBC_G4_RC_CFG8

WBC_G4_RC_CFG8 is an RC parameter 8 register.

Offset Address	Register Name	Total Reset Value
0xA4A8	WBC_G4_RC_CFG8	0x825A_2832

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	qp_dec3_bits_thr								qp_dec2_bits_thr								qp_dec1_bits_thr								qp_inc1_bits_thr							
Reset	1	0	0	0	0	0	1	0	0	1	0	1	1	0	1	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:24]	RW	qp_dec3_bits_thr	Threshold 3 for the number of bits adjusted to decrease the QP value
[23:16]	RW	qp_dec2_bits_thr	Threshold 2 for the number of bits adjusted to decrease the QP value
[15:8]	RW	qp_dec1_bits_thr	Threshold 1 for the number of bits adjusted to decrease the QP value
[7:0]	RW	qp_inc1_bits_thr	Threshold for the number of bits adjusted to increase the QP value

WBC_G4_RC_CFG9

WBC_G4_RC_CFG9 is an RC parameter 9 register.

Offset Address	Register Name	Total Reset Value
0xA4AC	WBC_G4_RC_CFG9	0x0014_0046

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								force_qp_thr_cap								reserved								force_qp_thr							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	force_qp_thr_cap	Threshold for forcible qp_cap variance
[15:10]	RO	reserved	Reserved
[9:0]	RW	force_qp_thr	Threshold for forcible qp variance

WBC_G4_MAX_ROW_LEN

WBC_G4_MAX_ROW_LEN is a 128-bit unit register for the row with the lowest compression ratio.

Offset Address	Register Name	Total Reset Value
0xA4B0	WBC_G4_MAX_ROW_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						max_row_len									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	max_row_len	128-bit unit occupied by the row with the lowest compression ratio

WBC_DHD1_CTRL

WBC_DHD1_CTRL is a WBC0 control register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xAC00	WBC_DHD1_CTRL	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbc_en	reserved	mode_out		format_out				reserved											wbc_vtthd_mode	reserved	auto_stop_en	reserved									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wbc_en	WBC enable 0: disabled 1: enabled
[30]	RO	reserved	Reserved
[29:28]	RW	mode_out	WBC output mode 00: The output mode is automatically selected based on the interface read mode. That is, the progressive read mode is selected in progressive display mode, and the interlaced read mode is selected in interlaced display mode. 01: The progressive output mode is selected. 10: The top field is output. 11: The bottom field is output.
[27:24]	RW	format_out	WBC output data format semiplanar 0100: YUV420 0101: YUV422 Other values: reserved
[23:13]	RO	reserved	Reserved
[12]	RW	wbc_vtthd_mode	WBC interrupt report mode 0: report by frame 1: report by field
[11]	RO	reserved	Reserved
[10]	RW	auto_stop_en	When the bandwidth is low due to the rapid WBC speed, WBC is automatically disabled.
[9:0]	RO	reserved	Reserved

WBC_DHD1_UPD

WBC_DHD1_UPD is a WBC0 channel update enable register.

Offset Address	Register Name	Total Reset Value
0xAC04	WBC_DHD1_UPD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															regup
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WC	regup	Capture register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is automatically cleared by the hardware.

WBC_DHD1_YADDR

WBC_DHD1_YADDR is a capture luminance write address register.

Offset Address	Register Name	Total Reset Value
0xAC10	WBC_DHD1_YADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbcaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wbcaddr	When the output format is a semi-planar format, this register indicates the start address for the frame buffer luminance component. When the output format is a package or ARGB format, this register is the start address for a picture. In this case, WBC_G0_CADDR is meaningless. The address must be 4-byte-aligned, and the lower two bits are invalid (seamless combination is supported).

WBC_DHD1_CADDR

WBC_DHD1_CADDR is a capture chrominance write address register.

Offset Address	Register Name	Total Reset Value
0xAC14	WBC_DHD1_CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbccaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wbccaddr	Start address for the frame buffer chrominance component. The address must be 4-byte-aligned, and the lower two bits are invalid (seamless combination is supported).

WBC_DHD1_STRIDE

WBC_DHD1_STRIDE is a capture stride register.

Offset Address	Register Name	Total Reset Value
0xAC18	WBC_DHD1_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wbccstride																wbclstride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	wbccstride	Chrominance stride of the frame buffer, 16-byte-aligned
[15:0]	RW	wbclstride	Luminance stride of the frame buffer, 16-byte-aligned

WBC_DHD1_ORESO

WBC_DHD1_ORESO is an output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xAC20	WBC_DHD1_ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:12]	RW	oh	Height (in line). The value is the actual height minus 1. Note: In interlaced output mode, the actual layer height must be an even number. There is no such limitation in progressive output mode.
[11:0]	RW	ow	Width (in pixel). The value is the actual width minus 1. Note: The actual layer width must be an even number.

WBC_DHD1_PARAUP

WBC_DHD1_PARAUP is a gp1 coefficient-related register update enable register. The VDP scaling coefficients are configured by using the AXI master. Software configures the start addresses and parameter update flags by using the slave.

Offset Address	Register Name	Total Reset Value
0xAC40	WBC_DHD1_PARAUP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							wbc_vccoef_upd	wbc_vlcoef_upd	wbc_hccoef_upd	wbc_hlcoef_upd
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	wbc_vccoef_upd	Whether vertical chrominance filtering coefficients need to be updated. This bit is automatically cleared after the hardware updates the coefficients. 0: not updated 1: updated
[2]	WO	wbc_vlcoef_upd	Whether vertical luminance filtering coefficients need to be updated. This bit is automatically cleared after the hardware updates the coefficients. 0: not updated 1: updated
[1]	WO	wbc_hccoef_upd	Whether horizontal chrominance filtering coefficients need to be updated. This bit is automatically cleared after the hardware updates the coefficients. 0: not updated 1: updated

[0]	WO	wbc_hlcoef_upd	Whether horizontal luminance filtering coefficients need to be updated. This bit is automatically cleared after the hardware updates the coefficients. 0: not updated 1: updated

WBC_DHD1_HLCOEFAD

WBC_DHD1_HLCOEFAD is a WBC horizontal luminance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0xAC50	WBC_DHD1_HLCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address for storing coefficients in the local memory

WBC_DHD1_HCCOEFAD

WBC_DHD1_HCCOEFAD is a WBC horizontal chrominance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0xAC54	WBC_DHD1_HCCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address for storing coefficients in the local memory

WBC_DHD1_VLCOEFAD

WBC_DHD1_VLCOEFAD is a WBC vertical luminance filtering coefficient address register

Offset Address	Register Name	Total Reset Value
0xAC58	WBC_DHD1_VLCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address for storing coefficients in the local memory

WBC_DHD1_VCCOEFAD

WBC_DHD1_VCCOEFAD is a WBC vertical chrominance filtering coefficient address register.

Offset Address	Register Name	Total Reset Value
0xAC5C	WBC_DHD1_VCCOEFAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef_addr	Start address for storing coefficients in the local memory

WBC_DHD1_DITHER_CTRL

WBC_DHD1_DITHER_CTRL is a dither control register.

Offset Address	Register Name	Total Reset Value
0xAD00	WBC_DHD1_DITHER_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_md				reserved																											
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	dither_md	Dither mode select 000: 10-bit inputs, 8-bit outputs, no dithering, and direct bit truncation 011: 10-bit inputs, 8-bit outputs, and time-domain and spatial-domain dithering 101: 10-bit inputs, 8-bit outputs, and round off Other values: reserved
[28:0]	RO	reserved	Reserved

WBC_DHD1_DITHER_COEF0

WBC_DHD1_DITHER_COEF0 is a dither coefficient 0 register.

Offset Address	Register Name	Total Reset Value
0xAD04	WBC_DHD1_DITHER_COEF0	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef3								dither_coef2								dither_coef1								dither_coef0							
Reset	1	1	0	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef3	Coefficient 3 for time-domain dithering
[23:16]	RW	dither_coef2	Coefficient 2 for time-domain dithering
[15:8]	RW	dither_coef1	Coefficient 1 for time-domain dithering
[7:0]	RW	dither_coef0	Coefficient 0 for time-domain dithering

WBC_DHD1_DITHER_COEF1

WBC_DHD1_DITHER_COEF1 is a dither coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xAD08	WBC_DHD1_DITHER_COEF1	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef7								dither_coef6								dither_coef5								dither_coef4							
Reset	1	1	0	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef7	Coefficient 7 for time-domain dithering
[23:16]	RW	dither_coef6	Coefficient 6 for time-domain dithering
[15:8]	RW	dither_coef5	Coefficient 5 for time-domain dithering
[7:0]	RW	dither_coef4	Coefficient 4 for time-domain dithering

WBC_DHD1_HCDS

WBC_DHD1_HCDS is a horizontal chrominance down sampling parameter configuration register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xAE10	WBC_DHD1_HCDS	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hcds_en	hchmid_en	hchfir_en	reserved																												
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hcds_en	Horizontal chrominance down sampling enable 0: disabled 1: enabled
[30]	RW	hchmid_en	Median filtering enable for horizontal chrominance down sampling. This bit is invalid when hchfir_en is invalid. 0: disabled 1: enabled
[29]	RW	hchfir_en	Horizontal chrominance down sampling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[28:0]	RO	reserved	Reserved

WBC_DHD1_HCDS_COEF0

WBC_DHD1_HCDS_COEF0 is down sampling coefficient register 0.

Offset Address	Register Name	Total Reset Value
0xAE14	WBC_DHD1_HCDS_COEF0	0x0675_3C67

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef2								coef1										coef0									
Reset	0	0	0	0	0	1	1	0	0	1	1	1	0	1	0	1	0	0	1	1	1	1	0	0	0	1	1	0	0	1	1	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RO	coef2	Horizontal down sampling coefficient 2 (signed number)
[19:10]	RO	coef1	Horizontal down sampling coefficient 1 (signed number)
[9:0]	RO	coef0	Horizontal down sampling coefficient 0 (signed number)

WBC_DHD1_HCDS_COEF1

WBC_DHD1_HCDS_COEF1 is down sampling coefficient register 1.

Offset Address	Register Name	Total Reset Value
0xAE18	WBC_DHD1_HCDS_COEF1	0x0000_03E3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						coef3									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RO	coef3	Horizontal down sampling coefficient 3 (signed number)

WBC_DHD1_ZME_HSP

WBC_DHD1_ZME_HSP is a horizontal scaling parameter configuration register (non-instant register).

Scaling ratio = Input width/Output width

Offset Address	Register Name	Total Reset Value
0xAEC0	WBC_DHD1_ZME_HSP	0x0010_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hlmsc_en	hchmsc_en	hlmid_en	hchmid_en	non_lnr_en	hlfir_en	hchfir_en	hfir_order	hratio																							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hlmsc_en	Horizontal luminance scaling enable 0: disabled 1: enabled
[30]	RW	hchmsc_en	Horizontal chrominance scaling enable 0: disabled 1: enabled
[29]	RW	hlmid_en	Median filtering enable for horizontal luminance scaling. This bit is invalid when hlfir_en is invalid. 0: disabled 1: enabled
[28]	RW	hchmid_en	Median filtering enable for horizontal chrominance scaling. This bit is invalid when hchfir_en is invalid. 0: disabled 1: enabled
[27]	RW	non_lnr_en	Non-linear scaling enable 0: disabled 1: enabled
[26]	RW	hlfir_en	Horizontal luminance scaling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[25]	RW	hchfir_en	Horizontal chrominance scaling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[24]	RW	hfir_order	Horizontal scaling sequence 0: Horizontal scaling is performed before vertical scaling. 1: Horizontal scaling is performed after vertical scaling.
[23:0]	RW	hratio	Horizontal scaling ratio, in (u, 4, 20) format

WBC_DHD1_ZME_HLOFFSET

WBC_DHD1_ZME_HLOFFSET is a horizontal luminance offset register (non-instant register). It is used for pan-scan.

Offset Address	Register Name	Total Reset Value
0xAEC4	WBC_DHD1_ZME_HLOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hor_loffset																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	hor_loffset	Horizontal luminance offset, in (s, 8, 20) format. The value is expressed as a complement.

WBC_DHD1_ZME_HCOFFSET

WBC_DHD1_ZME_HCOFFSET is a horizontal chrominance offset register (non-instant register). It is used for pan-scan.

Offset Address	Register Name	Total Reset Value
0xAEC8	WBC_DHD1_ZME_HCOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hor_coffset																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	hor_coffset	Horizontal chrominance offset, in (s, 8, 20) format. The value is expressed as a complement.

WBC_DHD1_ZME_VSP

WBC_DHD1_ZME_VSP is a vertical scaling parameter register.

Offset Address	Register Name	Total Reset Value
0xAED8	WBC_DHD1_ZME_VSP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vlmsc_en	vchmsc_en	vlmid_en	vchmid_en	reserved	vsc_chroma_tap	reserved	vlfir_en	vchfir_en	zme_out_fmt		zme_in_fmt	reserved																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vlmsc_en	Vertical luminance scaling enable 0: disabled 1: enabled
[30]	RW	vchmsc_en	Vertical chrominance scaling enable 0: disabled 1: enabled
[29]	RW	vlmid_en	Median filtering enable for vertical luminance scaling. This bit is invalid when vlfir_en is invalid. 0: disabled 1: enabled
[28]	RW	vchmid_en	Median filtering enable for vertical chrominance scaling. This bit is invalid when vchfir_en is invalid. 0: disabled 1: enabled
[27]	RO	reserved	Reserved
[26]	RW	vsc_chroma_tap	Vertical chrominance scaling tap 0: 4-tap FIR 1: 2-tap FIR
[25]	RW	reserved	Reserved
[24]	RW	vlfir_en	Vertical luminance scaling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)
[23]	RW	vchfir_en	Vertical chrominance scaling mode 0: replication mode (filtering disabled) 1: filtering mode (filtering enabled)

[22:21]	RW	zme_out_fmt	Output data format for scaling 0: 422 1: 420
[20:19]	RW	zme_in_fmt	Input data format for scaling 0: 422 1: 420
[18:0]	RO	reserved	Reserved

WBC_DHD1_ZME_VSR

WBC_DHD1_ZME_VSR is a vertical luminance scaling ratio register (non-instant register).

Scaling ratio = Input height/Output height

Offset Address	Register Name	Total Reset Value
0xAEDC	WBC_DHD1_ZME_VSR	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vratio															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vratio	Vertical scaling ratio, in (u, 4, 12) format

WBC_DHD1_ZME_VOFFSET

WBC_DHD1_ZME_VOFFSET is a vertical luminance scaling offset register. The vertical scaling offset is affected by the field offset during pan-scan and the field offset when repeated frames occur. If no field offset occurs, vluma_offset is the lowest integral part plus the decimal part of offset_pan-scan. In YCbCr422 format, vchroma_offset is equal to vluma_offset; in YCbCr420 format, vchroma_offset is calculated as follows: vchroma_offset = scaling_chroma/2 – 0.25. If the field offset is required (such as static frames or repeated frames) and the bottom field is repeated, the values of vluma_offset and vchroma_offset configured for the top field are the same as those in the case of no field offset. The field offset must be considered when coefficients are configured for the bottom field.

Offset Address	Register Name	Total Reset Value
0xAEE0	WBC_DHD1_ZME_VOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vluma_offset																vchroma_offset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	vluma_offset	Vertical luminance offset, in (s, 4, 12) format. The value is expressed as a complement.
[15:0]	RW	vchroma_offset	Vertical chrominance offset, in (s, 4, 12) format. The value is expressed as a complement.

WBC_DHD1_ZME_VBOFFSET

WBC_DHD1_ZME_VBOFFSET is a vertical luminance scaling offset register for the bottom field. The vertical scaling offset is affected by the field offset during pan-scan and the field offset when repeated frames occur. If no field offset occurs, vluma_offset is the lowest integral part plus the decimal part of offset_pan-scan. In YCbCr422 format, vchroma_offset is equal to vluma_offset; in YCbCr420 format, vchroma_offset is calculated as follows: vchroma_offset = scaling_chroma/2 – 0.25. If the field offset is required (such as static frames or repeated frames) and the bottom field is repeated, the values of vluma_offset and vchroma_offset configured for the top field are the same as those in the case of no field offset. The field offset must be considered when coefficients are configured for the bottom field.

Offset Address	Register Name	Total Reset Value
0xAEE4	WBC_DHD1_ZME_VBOFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vbluma_offset																vbchroma_offset															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	vbluma_offset	Vertical luminance offset, in (s, 4, 12) format. The value is expressed as a complement.
[15:0]	RW	vbchroma_offset	Vertical chrominance offset, in (s, 4, 12) format. The value is expressed as a complement.

CBM_BKG2

CBM_BKG2 is a CBM mixer 2 overlay background color register.

Offset Address	Register Name	Total Reset Value
0xB420	CBM_BKG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cbm_bkgy2								cbm_bkgcb2								cbm_bkgcr2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	cbm_bkgy2	Overlay background color of CBM mixer 2, Y component
[19:10]	RW	cbm_bkgcb2	Overlay background color of CBM mixer 2, Cb component
[9:0]	RW	cbm_bkgcr2	Overlay background color of CBM mixer 2, Cr component

CBM_MIX2

CBM_MIX2 is a CBM mixer 2 priority configuration register (instant register). The register configuration takes effect only when the VSYNC signal is valid. mixer_prio_x is the overlay layer priority *x*.

Offset Address	Register Name	Total Reset Value
0xB428	CBM_MIX2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mixer_prio4				mixer_prio3				mixer_prio2				mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RW	mixer_prio4	Drive layer of CBM mixer 2 with priority 4 0000: no drive layer 0011: V3 0100: G4 1001: V1 1010: HC0 Other values: reserved

[15:12]	RW	mixer_prio3	Drive layer of CBM mixer 2 with priority 3 0000: no drive layer 0011: V3 0100: G4 1001: V1 1010: HC0 Other values: reserved
[11:8]	RW	mixer_prio2	Drive layer of CBM mixer 2 with priority 2 0000: no drive layer 0011: V3 0100: G4 1001: V1 1010: HC0 Other values: reserved
[7:4]	RW	mixer_prio1	Drive layer of CBM mixer 2 with priority 1 0000: no drive layer 0011: V3 0100: G4 1001: V1 1010: HC0 Other values: reserved
[3:0]	RW	mixer_prio0	Drive layer of CBM mixer 2 with priority 0 0000: no drive layer 0011: V3 0100: G4 1001: V1 1010: HC0 Other values: reserved

MIXDSD_BKG

MIXDSD_BKG is a DSD mixer 1 overlay background color register.

Offset Address	Register Name	Total Reset Value
0xB600	MIXDSD_BKG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				mixer_bkgy								mixer_bkgcb								mixer_bkgcr											

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	mixer_bkgy	Overlay background color of MIXDSD, Y component
[19:10]	RW	mixer_bkgcb	Overlay background color of MIXDSD, Cb component
[9:0]	RW	mixer_bkgcr	Overlay background color of MIXDSD, Cr component

MIXDSD_MIX

MIXDSD_MIX is a DSD mixer 1 priority configuration register (instant register). The register configuration takes effect only when the VSYNC signal is valid. mixer_prio_x is overly layer priority *x*.

Offset Address	Register Name	Total Reset Value
0xB608	MIXDSD_MIX	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mixer_prio3				mixer_prio2				mixer_prio1				mixer_prio0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	mixer_prio3	Drive layer of DSD mixer 1 with priority 3 000: no drive layer 0001: V4 0010: G1 1001: HC1 1010: HC0 Other values: reserved
[11:8]	RW	mixer_prio2	Drive layer of DSD mixer 1 with priority 2 000: no drive layer 0001: V4 0010: G1 1010: HC0 Other values: reserved

[7:4]	RW	mixer_prio1	Drive layer of DSD mixer 1 with priority 1 000: no drive layer 0001: V4 0010: G1 1010: HC0 Other values: reserved
[3:0]	RW	mixer_prio0	Drive layer of DSD mixer 1 with priority 0 000: no drive layer 0001: V4 0010: G1 1010: HC0 Other values: reserved

DHD1_CTRL

DHD1_CTRL is a display channel global control register. You must configure any bit of this register before configuring DHD1_CTRL[intf_en]. Otherwise, the configuration does not take effect.

Offset Address	Register Name	Total Reset Value
0xC400	DHD1_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en		cbar_en		cbar_sel		reserved		fpga_lmt_en		fpga_lmt_width						reserved											iop		reserved			regup
Reset	0		0		0		0		0		0		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[31]	RW	intf_en	Display interface enable (instant register). Data is output over the interface only when this field is enabled. 0: disabled 1: enabled
[30]	RW	cbar_en	Color bar enable. The color bar is output over the interface when this field is enabled. 0: disabled 1: enabled
[29]	RW	cbar_sel	Color space select for the output color bar (instant register) 0: VGA 1: YPbPr

[28]	RO	reserved	Reserved
[27]	RW	fpga_lmt_en	Debug field. As the frequency of the FPGA clock bus is limited, the 1080i picture cannot be displayed. After this bit is enabled, the picture with 1280-pixel width can be displayed over the 1080i interface. 0: disabled 1: enabled
[26:20]	RW	fpga_lmt_width	Debug field. When fpga_lmt_en is enabled, the active region width of the VDP interface depends on this field. The actual width of the active region is calculated as follows: Actual width of the active region = fpga_lmt_width x 16
[19:5]	RO	reserved	Reserved
[4]	RW	iop	Progressive or interlaced display (non-instant register) 0: interlaced display 1: progressive display
[3:1]	RO	reserved	Reserved
[0]	WC	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After updates, this bit is automatically cleared by the hardware.

DHD1_VSYNC

DHD1_VSYNC is a top field vertical sync timing register in interlaced output mode or frame vertical sync timing register in progressive output mode. This register is a non-instant register.

Offset Address	Register Name	Total Reset Value
0xC404	DHD1_VSYNC	0x0011_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:20]	RW	vfb	In interlaced output mode: top vertical front blanking (TVFB) In progressive output mode: vertical front blanking (VFB)
[19:12]	RW	vbb	In interlaced output mode: top vertical back blanking (TVBB) In progressive output mode: vertical back blanking (VBB)+vertical pulse width (VPW)

[11:0]	RW	vact	In interlaced output mode: height of active picture on the top field In progressive output mode: height of an active picture in a frame. The register value is the actual value minus 1.

DHD1_HSYNC1

DHD1_HSYNC1 is horizontal sync configuration register 1 in interlaced or progressive output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC408	DHD1_HSYNC1	0x00BF_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	Horizontal back blanking (HBB), in pixel
[15:0]	RW	hact	Number of horizontal pixels in an active region

DHD1_HSYNC2

DHD1_HSYNC2 is horizontal sync configuration register 2 in interlaced or progressive output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC40C	DHD1_HSYNC2	0x0000_020F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hmid																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hmid	Bottom vertical sync active pixel (active region)
[15:0]	RW	hfb	Horizontal front blanking (HFB), in pixel

DHD1_VPLUS

DHD1_VPLUS is a bottom field vertical sync timing in interlaced output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC410	DHD1_VPLUS	0x0021_321B

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	bvfb		bvbb		bvact		
Reset	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 1	0 0 1 1	0 0 1 0	0 0 0 1	1 0 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:20]	RW	bvfb	Bottom vertical front blanking (BVFB) in interlaced output mode
[19:12]	RW	bvbb	Bottom vertical back blanking (BVBB)+VPW in interlaced output mode
[11:0]	RW	bvact	Height of an active picture in the bottom field in interlaced output mode The register value is the actual value minus 1.

DHD1_PWR

DHD1_PWR is a sync signal pulse width register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC414	DHD1_PWR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		vpw		hpw			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	vpw	VPW minus 1.
[15:0]	RW	hpw	Horizontal pulse width (HPW) minus 1.

DHD1_VTTHD3

DHD1_VTTHD3 is a vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xC418	DHD`_VTTHD3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	thd4_mode	reserved			vtmgthd4												thd3_mode	reserved			vtmgthd3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	thd4_mode	Mode of generating threshold 4 0: frame mode. The threshold count is in the unit of frame. 1: field mode. The threshold count is in the unit of field during interlaced displaying.
[30:29]	RO	reserved	Reserved
[28:16]	RW	vtmgthd4	Vertical timing threshold 4 for simultaneously triggering DHD and DSD. The start time of the DSD interface timing is later than that of the DHD interface timing and is equal to the number of lines configured in vtmgthd4.
[15]	RW	thd3_mode	Mode of generating threshold 3 0: frame mode. The threshold count is in the unit of frame. 1: field mode. The threshold count is in the unit of field during interlaced displaying.
[14:13]	RO	reserved	Reserved
[12:0]	RW	vtmgthd3	Vertical timing threshold 3. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd3_int] interrupt is triggered.

DHD1_VTTHD

DHD1_VTTHD is a vertical timing threshold register (instant register). It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xC11C	DHD1_VTTHD	0x0001_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	thd2_mode	reserved			vtmgthd2												thd1_mode	reserved			vtmgthd1											

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	thd2_mode	Mode of generating threshold 2 0: frame mode. The threshold count is in the unit of frame. 1: field mode. The threshold count is in the unit of field during interlaced displaying
[30:29]	RO	reserved	Reserved
[28:16]	RW	vtmgthd2	Vertical timing threshold 2. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd2_int] interrupt is triggered.
[15]	RW	thd1_mode	Mode of generating threshold 1 0: frame mode. The threshold count is in the unit of frame. 1: field mode. The threshold count is in the unit of field during interlaced displaying
[14:13]	RO	reserved	Reserved
[12:0]	RW	vtmgthd1	Vertical timing threshold 1. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd_int1] interrupt is triggered.

DHD1_AFFTHD

DHD1_AFFTHD is a DHD buffer FIFO register.

Offset Address	Register Name	Total Reset Value
0xC430	DHD1_AFFTHD	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					dhd_aff_thd										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RW	reserved	Reserved
[10:0]	RW	dhd_aff_thd	DHD buffer FIFO register

DHD1_ABUFTHD

DHD1_ABUFTHD is a DHD buffer register.

Offset Address	Register Name	Total Reset Value
0xC434	DHD1_ABUFTHD	0x0000_0073

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dhd_buf_thd							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1

Bits	Access	Name	Description
[31:11]	RW	reserved	Reserved
[10:0]	RW	dhd_buf_thd	DHD buffer register

DHD1_DACDET1

DHD1_DACDET1 is DAC automatic detection register 1.

Offset Address	Register Name	Total Reset Value
0xC438	DHD1_VGA_DACDET1	0x000D_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								det_line								reserved				vdac_det_high											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	det_line	Line of the detected level
[15:10]	RO	reserved	Reserved
[9:0]	RW	vdac_det_high	Detected level

DHD1_DACDET2

DHD1_DACDET2 is DAC automatic detection register 2.

Offset Address	Register Name	Total Reset Value
0xC43C	DHD1_VGA_DACDET2	0x0030_0118

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdac_det_en	reserved							det_pixel_wid								reserved				det_pixel_sta											

Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[31]	RW	vdac_det_en	DAC automatic detection enable 0: disabled 1: enabled
[30:27]	RO	reserved	Reserved
[26:16]	RW	det_pixel_wid	Level width
[15:11]	RO	reserved	Reserved
[10:0]	RW	det_pixel_sta	Start position of a line

DHD1_PARATHD

DHD1_PARATHDis a PARA coefficient update point threshold register.

Offset Address	Register Name	Total Reset Value
0xC4B0	DHD1_PARATHD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfs_en	reserved																							para_thd								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RW	reserved	Reserved
[5:0]	RW	para_thd	PARA coefficient update point threshold. It indicates the line after the vertical back blanking where the update point occurs. This field is valid only after DFS is enabled.

DHD1_START_POS

DHD1_START_POS is a DHD start signal start position register.

Offset Address	Register Name	Total Reset Value
0xC4B4	DHD1_START_POS	0x0000_0805

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																timing_start_pos								start_pos							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15:8]	RW	timing_start_pos	Number of lines before the active region where the timing_gen state machine starts to work
[7:0]	RW	start_pos	Number of lines before the active region where the start signal is generated in online mode

DHD1_STATE

DHD1_STATE is a DHD1 status register.

Offset Address	Register Name	Total Reset Value
0xC4F0	DHD1_STATE	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								count_int								vcnt													bottom_field	vblank	vback_blank
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RO	count_int	DHD1 interrupt count. The interrupt count is increased by 1 each time a vertical timing interrupt is reported.
[15:3]	RO	vcnt	Active display line count of DHD1
[2]	RO	bottom_field	DHD1 top/bottom field display flag 0: top field 1: bottom field
[1]	RO	vblank	DHD1 blanking region display flag 0: active region 1: blanking region
[0]	RO	vback_blank	DHD1 back blanking region display flag 0: non-back blanking region 1: blanking region

INTF_CTRL

INTF_CTRL is an output interface control register.

Offset Address	Register Name	Total Reset Value
0xD000	INTF_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hdmi_mode	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hdmi_mode	Color space select for the output HDMI data (non-instant register) 0: YUV 1: RGB
[30:0]	RO	reserved	Reserved

INTF_SYNC_INV

INTF_SYNC_INV is sync signal polarity configuration register in external sync timing output mode. The setting of this register takes effect immediately after configuration. That is, the polarity of the corresponding sync signal is immediately affected.

Offset Address	Register Name	Total Reset Value
0xD008	INTF_SYNC_INV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												f_inv	vs_inv	hs_inv	dv_inv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	f_inv	Output phase reverse enable for the odd/even field indicator signal (instant register) 0: disabled 1: enabled

[2]	RW	vs_inv	Output phase reverse enable for the vertical sync pulse (instant register) 0: disabled 1: enabled
[1]	RW	hs_inv	Output phase reverse enable for the horizontal sync pulse (instant register) 0: disabled 1: enabled
[0]	RW	dv_inv	Output phase reverse enable for the data validity signal (instant register) 0: disabled 1: enabled

INTF_CLIP0_L

INTF_CLIP0_L is a clip lowest threshold register (instant register).

Offset Address	Register Name	Total Reset Value
0xD010	INTF_CLIP0_L	0x0100_4010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_cl2								clip_cl1								clip_cl0											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	clip_cl2	Lowest threshold Y/R of component 2, unsigned integer
[19:10]	RW	clip_cl1	Lowest threshold Cb/G of component 1, unsigned integer
[9:0]	RW	clip_cl0	Lowest threshold Cr/B of component 0, unsigned integer

INTF_CLIP0_H

INTF_CLIP0_H is a clip highest threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

Offset Address	Register Name	Total Reset Value
0xD014	INTF_CLIP0_H	0x0EB3_C0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_ch2								clip_ch1												clip_ch0							
Reset	0	0	0	0	1	1	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	clip_ch2	Highest threshold Y/R of component 2, unsigned integer
[19:10]	RW	clip_ch1	Highest threshold Cb/G of component 1, unsigned integer
[9:0]	RW	clip_ch0	Highest threshold Cr/B of component 0, unsigned integer

INTF_CSC_IDC

INTF_CSC_IDC is a CSC input DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0xD020	INTF_CSC_IDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									csc_en			cscidc1												cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_en	CSC enable 0: disabled 1: enabled
[21:11]	RW	cscidc1	DC parameter of the input component 1. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscidc0	DC parameter of the input component 0. The MSB is the signed bit. The value is expressed as a complement.

INTF_CSC_ODC

INTF_CSC_ODC is a CSC output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0xD024	INTF_CSC_ODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		csc_sign_mode	cscodc1		cscodc0		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_sign_mode	CSC output mode 0: The CSC output is a 10-bit unsigned number. 1: The CSC output is a 12-bit signed number.
[21:11]	RW	cscodc1	DC parameter of the output component 1. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscodc0	DC parameter of the output component 0. The MSB is the signed bit. The value is expressed as a complement.

INTF_CSC_IODC

INTF_CSC_IODC is a CSC input/output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0xD028	INTF_CSC_IODC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cscodc2		cscidc2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:11]	RW	cscodc2	DC parameter of the output component 2. The MSB is the signed bit. The value is expressed as a complement.
[10:0]	RW	cscidc2	DC parameter of the input component 2. The MSB is the signed bit. The value is expressed as a complement.

INTF_CSC_P0

INTF_CSC_P0 is a CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0xD02C	INTF_CSC_P0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp01												reserved				cscp00											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp01	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp00	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

INTF_CSC_P1

INTF_CSC_P1 is a CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0xD030	INTF_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp10	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved

[14:0]	RW	cscp02	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

INTF_CSC_P2

INTF_CSC_P2 is a CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0xD034	INTF_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp12	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp11	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

INTF_CSC_P3

INTF_CSC_P3 is a CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0xD038	INTF_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp21	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.
[15]	RO	reserved	Reserved

[14:0]	RW	cscp20	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

INTF_CSC_P4

INTF_CSC_P4 is a CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0xD03C	INTF_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cscp22															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:0]	RW	cscp22	5.10 data format indicating one sign bit, four integer bits, and 10 decimal bits. The value is represented by a complement.

INTF_HSPCFG0

INTF_HSPCFG0 is HSP configuration register 0 (instant register).

Offset Address	Register Name	Total Reset Value
0xD040	INTF_HSPCFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hsp_hf0_tmp3								hsp_hf0_tmp2								hsp_hf0_tmp1								hsp_hf0_tmp0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	hsp_hf0_tmp3	High-frequency filtering coefficient 3, signed number
[23:16]	RW	hsp_hf0_tmp2	High-frequency filtering coefficient 2, signed number
[15:8]	RW	hsp_hf0_tmp1	High-frequency filtering coefficient 1, signed number
[7:0]	RW	hsp_hf0_tmp0	High-frequency filtering coefficient 0, signed number

INTF_HSPCFG1

INTF_HSPCFG1 is HSP configuration register 1 (instant register).

Offset Address	Register Name	Total Reset Value
0xD044	INTF_HSPCFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hsp_en	reserved																							hsp_hf0_coring							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hsp_en	HSP enable 0: disabled 1: enabled
[30:8]	RO	reserved	Reserved
[7:0]	RW	hsp_hf0_coring	High-frequency coring coefficient, unsigned number

INTF_HSPCFG5

INTF_HSPCFG5 is HSP configuration register 5 (instant register).

Offset Address	Register Name	Total Reset Value
0xD054	INTF_HSPCFG5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hsp_hf0_gainneg												reserved				hsp_hf0_gainpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	hsp_hf0_gainneg	High-frequency gain negative polarity coefficient, signed number (10.8)
[15:11]	RO	reserved	Reserved
[10:0]	RW	hsp_hf0_gainpos	High-frequency gain positive polarity coefficient, signed number (10.8)

INTF_HSPCFG6

INTF_HSPCFG6 is HSP configuration register 6 (instant register).

Offset Address	Register Name	Total Reset Value
0xD058	INTF_HSPCFG6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hsp_hf0_adpshoot_en	hsp_hf0_winsize			reserved				hsp_hf0_mixratio								hsp_hf0_underth								hsp_hf0_overth							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hsp_hf0_adpshoot_en	High-frequency adjustment threshold enable 0: disabled 1: enabled
[30:28]	RW	hsp_hf0_winsize	High-frequency window size, unsigned number. The value range is 0–4.
[27:24]	RO	reserved	Reserved
[23:16]	RW	hsp_hf0_mixratio	High-frequency adjustment threshold ratio, unsigned number (8.7)
[15:8]	RW	hsp_hf0_underth	High-frequency adjustment lower threshold, unsigned number
[7:0]	RW	hsp_hf0_overth	High-frequency adjustment upper threshold, unsigned number

INTF_HSPCFG7

INTF_HSPCFG7 is HSP configuration register 7 (instant register).

Offset Address	Register Name	Total Reset Value
0xD05C	INTF_HSPCFG7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hsp_hf1_tmp3								hsp_hf1_tmp2								hsp_hf1_tmp1								hsp_hf1_tmp0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	hsp_hf1_tmp3	High-frequency filtering coefficient 3, signed number
[23:16]	RW	hsp_hf1_tmp2	High-frequency filtering coefficient 2, signed number
[15:8]	RW	hsp_hf1_tmp1	High-frequency filtering coefficient 1, signed number

[7:0]	RW	hsp_hf1_tmp0	High-frequency filtering coefficient 0, signed number

INTF_HSPCFG8

INTF_HSPCFG8 is HSP configuration register 8 (instant register).

Offset Address	Register Name	Total Reset Value
0xD060	INTF_HSPCFG8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hsp_hf1_coring							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	hsp_hf1_coring	High-frequency coring coefficient, unsigned number

INTF_HSPCFG12

INTF_HSPCFG12 is HSP configuration register 12 (instant register).

Offset Address	Register Name	Total Reset Value
0xD070	INTF_HSPCFG12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hsp_hf1_gainneg												reserved				hsp_hf1_gainpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	hsp_hf1_gainneg	High-frequency gain negative polarity coefficient, signed number (10.8)
[15:11]	RO	reserved	Reserved
[10:0]	RW	hsp_hf1_gainpos	High-frequency gain positive polarity coefficient, signed number (10.8)

INTF_HSPCFG13

INTF_HSPCFG13 is HSP configuration register 13 (instant register).

Offset Address	Register Name	Total Reset Value
0xD074	INTF_HSPCFG13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hsp_hf1_adpshoot_en	hsp_hf1_winsize			reserved				hsp_hf1_mixratio								hsp_hf1_underth								hsp_hf1_overth							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hsp_hf1_adpshoot_en	High-frequency adjustment threshold enable 0: disabled 1: enabled
[30:28]	RW	hsp_hf1_winsize	High-frequency window size, unsigned number. The value range is 0–4.
[27:24]	RO	reserved	Reserved
[23:16]	RW	hsp_hf1_mixratio	High-frequency adjustment threshold ratio, unsigned number (8.7)
[15:8]	RW	hsp_hf1_underth	High-frequency adjustment lower threshold, unsigned number
[7:0]	RW	hsp_hf1_overth	High-frequency adjustment upper threshold, unsigned number

INTF_HSPCFG14

INTF_HSPCFG14 is HSP configuration register 14 (instant register).

Offset Address	Register Name	Total Reset Value
0xD078	INTF_HSPCFG14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hsp_h0_en	hsp_h1_en	hsp_ltih_en	hsp_ctih_en	reserved			hsp_hf_shootdiv	hsp_lti_ratio								hsp_ldti_gain								hsp_cdti_gain							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hsp_h0_en	High-frequency filtering 0 enable 0: disabled 1: enabled
[30]	RW	hsp_h1_en	High-frequency filtering 1 enable 0: disabled 1: enabled
[29]	RW	hsp_ltih_en	Horizontal LTI enable 0: disabled 1: enabled
[28]	RW	hsp_ctih_en	Horizontal CTI enable 0: disabled 1: enabled
[27]	RO	reserved	Reserved
[26:24]	RW	hsp_hf_shootdiv	High-frequency adjustment shift coefficient, unsigned number. The value range is 1−7.
[23:16]	RW	hsp_lti_ratio	Luminance enhancement ratio, unsigned number (8.7)
[15:8]	RW	hsp_ldti_gain	Luminance enhancement gain coefficient, unsigned number (8.5)
[7:0]	RW	hsp_cdti_gain	Chrominance enhancement gain coefficient, unsigned number (8.5)

INTF_HSPCFG15

INTF_HSPCFG15 is HSP configuration register 15 (instant register).

Offset Address	Register Name	Total Reset Value
0xD07C	INTF_HSPCFG15	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				hsp_peak_ratio								reserved	hsp_glb_overth									reserved	hsp_glb_underth								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:20]	RW	hsp_peak_ratio	Luminance enhancement ratio, unsigned number (8.7)

[19]	RO	reserved	Reserved
[18:10]	RW	hsp_glb_overth	Luminance enhancement global upper threshold, unsigned number
[9]	RO	reserved	Reserved
[8:0]	RW	hsp_glb_underth	Luminance enhancement global lower threshold, unsigned number

DATE_COEFF0

DATE_COEFF0 is a standard parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xF200	DATE_COEFF0	0x5284_14FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clpf_sel		dis_ire	reserved	pal_half_en	pbpr_lpf_en	scanline	rgb_en	vbi_lpf_en	fm_sel	style_sel		sync_mode_sel				sync_mode_scart	length_sel	agc_amp_sel	luma_dl				reserved	oversam_en		lunt_en	oversam2_en	chlp_en	sylp_en	chgain_en	tt_seq
Reset	0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Bandwidth of the chrominance low-pass filter 00: 1.1 MHz (NTSC) 01: 1.3 MHz (PAL) 10: 1.6 MHz (for test) 11: reserved
[29]	RW	dis_ire	For the (M) NTSC and (M, N) PAL standards, the black level is 7.5 IRE higher than the blanking level; for other standards, the black level is equal to the blanking level. This bit controls whether the black level is 7.5 IRE higher than the blanking level. 0: The black level is 7.5 IRE higher than the blanking level. 1: The black level is equal to the blanking level.
[28]	RO	reserved	Reserved
[27]	RW	pal_half_en	PAL half line reduction enable 0: disabled 1: enabled

[26]	RW	pbpr_lpf_en	Component chrominance low-pass filtering enable 0: disabled 1: enabled
[25]	RW	scanline	Number of scanned lines in each frame based on standards. For the (M) NTSC, NTSC-J, and (M) PAL standards, each line contains 525 lines; for the (B, D, J, H, I) PAL, (N) PAL, and (Nc) PAL standards, each frame contains 625 lines. 0: 525 lines in a frame 1: 625 lines in a frame
[24]	RW	rgb_en	When intf_sel is set to 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr 1: RGB
[23]	RW	vbi_lpf_en	VBI data low-pass filtering enable 0: no filtering 1: filtering
[22]	RW	fm_sel	FMSECAM frequency modulation select 0: SIN mode 1: COS mode
[21:18]	RW	style_sel	CVBS/S-Video output signal standard when this bit works with the scanline bit When the scanline bit is 0 (525 scanned lines in a frame), the definition of the style_sel bit is as follows: 0001: (M) NTSC standard 0010: NTSC-J standard 0100: (M) PAL standard When the scanline bit is 1 (625 scanned lines in a frame), the definition of the style_sel bit is as follows: 0001: (B, D, G, H, I) PAL standard 0010: (N) PAL standard 0100: (Nc) PAL standard 1000: SECAM standard

[17:16]	RW	sync_mode_sel	bit[17]: specifies whether there are sync signals in three channels during component output. This bit takes effect only when the sync_mode_scart bit is set to 0. bit[17] is valid only when intf_sel is set to 100 (component output enabled). The definition of bit[17] is as follows: 0: Only one channel contains sync signals during component output. 1: Three channels contain sync signals during component output. When bit[17] is set to 0, the sync channel must be the Y channel for YPbPr output or G channel for RGB output. bit[16]: specifies whether there are blanking radixes during RGB output. bit[16] is valid only when intf_sel is set to 100 and rgb_en is set to 1. The definition of bit[16] is as follows: 0: There are no blanking radixes during RGB output. 1: There are blanking radixes during RGB output.
[15]	RW	sync_mode_scart	Overlay sync control for the components of three channels 0: Component sync output is configured based on sync_mode_sel bit[1]. 1: The components of the three channels are not overlaid and synchronized. In this case, sync_mode_sel bit[1] must be set to 0.
[14]	RW	length_sel	Active width of each video line (in pixel) 0: output according to the line active pixel width in BT.601 mode. 1: output according to the line active pixel width in BT.470 mode When this bit is set to 0, the active width of the line is 720 pixels. When this bit is set to 1, the active width of the line is 704 pixels for the 625-line standard or 712 pixels for the 525-line standard. Currently, the BT.601 mode and BT.470 mode cannot be dynamically switched. You can change the mode only after reset. The BT.601 mode is recommended, and this mode is the default mode after power-on reset.
[13]	RW	agc_amp_sel	AGC pulse select 0: The AGC pulse is generated based on the on-chip default value (recommended). 1: The AGC pulse is generated based on the off-chip configuration. DATE_COEFF1[amp_outside]

[12:9]	RW	luma_dl	Lead or lag-behind offset of the chrominance signal relative to the luminance signal, in the unit of half a pixel width. bit[12]: offset direction of the chrominance signal relative to the luminance signal. 0: The chrominance signal lags behind the luminance signal. 1: The chrominance signal leads the luminance signal. bit[11:9]: absolute offset of the chrominance signal relative to the luminance signal. The value is in binary format and ranges from 0 to 7. 000: The chrominance signal is aligned with the luminance signal. No adjustment is required. 001−111: The chrominance signal leads or lags behind the luminance signal by one to seven units.
[8]	RO	reserved	Reserved
[7:6]	RW	oversam_en	Level-1 over-sampling enable. Both luminance over-sampling and chrominance over-sampling are controlled. bit[7]: luminance over-sampling enable 0: disabled 1: enabled bit[6]: chrominance over-sampling enable 0: disabled 1: enabled
[5]	RW	lunt_en	Luminance notch enable 0: disabled 1: enabled
[4]	RW	oversam2_en	Level-2 over-sampling enable. Both the luminance channel and chrominance channel are controlled. 0: disabled 1: enabled
[3]	RW	chlp_en	Chrominance low-pass filtering enable 0: disabled 1: enabled
[2]	RW	sylp_en	Sync low-pass filtering enable 0: disabled 1: enabled
[1]	RW	chgain_en	Chrominance gain enable 0: disabled 1: enabled
[0]	RW	tt_seq	Sequence of transmitting the bits of the teletext data 0: from upper bits to lower bits 1: from lower bits to upper bits

DATE_COEFF1

DATE_COEFF1 is an amplitude configuration register.

Offset Address	Register Name	Total Reset Value
0xF204	DATE_COEFF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_gain			cvbs_limit_en	wss_seq	vps_seq	cgms_seq	cc_seq	c_limit_en	amp_outside										date_test_en	date_test_mode				dac_test							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	c_gain	Adjustment of the chrominance sync gain amplitude
[28]	RW	cvbs_limit_en	CVBS amplitude limit control 0: not limited 1: limited
[27]	RW	wss_seq	Sequence of transmitting the bits of the WSS data 0: from upper bits to lower bits 1: from lower bits to upper bits
[26]	RW	vps_seq	Sequence of transmitting the bits of the video programming system (VPS) data 0: from upper bits to lower bits 1: from lower bits to upper bits
[25]	RW	cgms_seq	Sequence of transmitting the bits of the copy generation management system (CGMS) data 0: from upper bits to lower bits 1: from lower bits to upper bits
[24]	RW	cc_seq	Sequence of transmitting the bits of the closed caption data 0: from upper bits to lower bits 1: from lower bits to upper bits
[23]	RW	c_limit_en	Chrominance amplitude limit control 0: not limited 1: limited
[22:13]	RW	amp_outside	Pulse amplitude input of the external AGC

[12]	RW	date_test_en	Test valid signal
[11:10]	RW	date_test_mode	Test mode signal
[9:0]	RW	dac_test	DAC test value input

DATE_COEFF2

DATE_COEFF2 is a DATE coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF208	DATE_COEFF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef02																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	coef02	DATE coefficient 2

DATE_COEFF3

DATE_COEFF3 is a DATE coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF20C	DATE_COEFF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								coef03																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:0]	RW	coef03	DATE coefficient 3

DATE_COEFF4

DATE_COEFF4 is a DATE coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF210	DATE_COEFF4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef04																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:0]	RW	coef04	DATE coefficient 4

DATE_COEFF5

DATE_COEFF5 is a DATE coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF214	DATE_COEFF5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef05																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:0]	RW	coef05	DATE coefficient 5

DATE_COEFF6

DATE_COEFF6 is a DATE coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF218	DATE_COEFF6	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef06_0	reserved											coef06_1																			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	coef06_0	DATE coefficient 6 register 0
[30:23]	RO	reserved	Reserved
[22:0]	RW	coef06_1	DATE coefficient 6 register 1

DATE_COEFF21

DATE_COEFF21 is an output matrix control register.

Offset Address	Register Name	Total Reset Value
0xF254	DATE_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac5_in_sel			reserved	dac4_in_sel			reserved	dac3_in_sel			reserved	dac2_in_sel			reserved	dac1_in_sel			reserved	dac0_in_sel		
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22:20]	RW	dac5_in_sel	DAC5 output mode 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0

[19]	RO	reserved	Reserved
[18:16]	RW	dac4_in_sel	DAC4 output mode 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[15]	RO	reserved	Reserved
[14:12]	RW	dac3_in_sel	DAC3 output mode 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[11]	RO	reserved	Reserved
[10:8]	RW	dac2_in_sel	DAC2 output mode 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[7]	RO	reserved	Reserved

[6:4]	RW	dac1_in_sel	DAC1 output mode 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0
[3]	RO	reserved	Reserved
[2:0]	RW	dac0_in_sel	DAC0 output mode 000: 0 001: CVBS 010: G/Y 011: B/Pb 100: R/Pr 101: svideo_y 110: svideo_c 111: 0

DATE_COEFF22

DATE_COEFF22 is a DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xF258	DATE_COEFF22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								video_phase_delta							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:0]	RW	video_phase_delta	DTO initial phase

DATE_COEFF23

DATE_COEFF23 is a video output delay configuration register.

Offset Address	Register Name	Total Reset Value
0xF25C	DATE_COEFF23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											dac5_out_dly	reserved			dac4_out_dly	reserved			dac3_out_dly	reserved			dac2_out_dly	reserved			dac1_out_dly	reserved			dac0_out_dly
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22:20]	RW	dac5_out_dly	DAC5 output delay cycle The value is measured by a 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.
[19]	RO	reserved	Reserved
[18:16]	RW	dac4_out_dly	DAC4 output delay cycle The value is measured by a 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.
[15]	RO	reserved	Reserved
[14:12]	RW	dac3_out_dly	DAC3 output delay cycle The value is measured by a 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.
[11]	RO	reserved	Reserved
[10:8]	RW	dac2_out_dly	DAC2 output delay cycle The value is measured by a 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.
[7]	RO	reserved	Reserved
[6:4]	RW	dac1_out_dly	DAC1 output delay cycle The value is measured by a 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.
[3]	RO	reserved	Reserved
[2:0]	RW	dac0_out_dly	DAC0 output delay cycle The value is measured by a 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.

DATE_COEFF24

DATE_COEFF24 is a ColorBurst start position register.

Offset Address	Register Name	Total Reset Value
0xF260	DATE_COEFF24	0x0001_2C99

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	burst_start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	0	1	1	0	0	1

Bits	Access	Name	Description
[31:0]	RW	burst_start	ColorBurst start position

DATE_COEFF25

DATE_COEFF25 is a SECAM preemphasis curve input coefficient register.

Offset Address	Register Name	Total Reset Value
0xF264	DATE_COEFF25	0x15B5_09C5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				x_n_1_coef												reserved				x_n_coef											
Reset	0	0	0	1	0	1	0	1	1	0	1	1	0	1	0	1	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	x_n_1_coef	Input coefficient 2 of the SECAM preemphasis curve
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_n_coef	Input coefficient 1 of the SECAM preemphasis curve

DATE_COEFF26

DATE_COEFF26 is a preemphasis curve input coefficient register.

Offset Address	Register Name	Total Reset Value
0xF268	DATE_COEFF26	0x0000_0945

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				x_n_1_coef											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:0]	RW	x_n_1_coef	Input coefficient 3 of the SECAM preemphasis curve

DATE_COEFF27

DATE_COEFF27 is a SECAM preemphasis curve output coefficient register.

Offset Address	Register Name	Total Reset Value
0xF26C	DATE_COEFF27	0x0780_00D0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_n_1_coef												reserved				y_n_coef											
Reset	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	y_n_1_coef	Output coefficient 2 of the SECAM preemphasis curve
[15:11]	RO	reserved	Reserved
[10:0]	RW	y_n_coef	Output coefficient 1 of the SECAM preemphasis curve

DATE_COEFF28

DATE_COEFF28 is a SECAM color burst start coordinate register.

Offset Address	Register Name	Total Reset Value
0xF270	DATE_COEFF28	0x06B0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				pixel_begin2												reserved				pixel_begin1											
Reset	0	0	0	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26:16]	RW	pixel_begin2	Start position 2 for SECAM color burst
[15:11]	RO	reserved	Reserved
[10:0]	RW	pixel_begin1	Start position 1 for SECAM color burst

DATE_COEFF29

DATE_COEFF29 is a SECAM color burst end coordinate register.

Offset Address	Register Name	Total Reset Value
0xF274	DATE_COEFF29	0x0000_00A2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pixel_end							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:0]	RW	pixel_end	End position for SECAM color burst

DATE_COEFF30

DATE_COEFF30 is a SECAM peak video signal level width coefficient register.

Offset Address	Register Name	Total Reset Value
0xF278	DATE_COEFF30	0x0000_003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												g_secam			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6:0]	RW	g_secam	SECAM peak video signal level width coefficient

DATE_ISRMASK

DATE_ISRMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0xF280	DATE_ISRMASK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								tt_mask
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	tt_mask	Teletext interrupt mask 0: enabled 1: masked

DATE_ISRSTATE

DATE_ISRSTATE is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0xF284	DATE_ISRSTATE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								tt_status
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WC	tt_status	Teletext interrupt status After the DATE module reads all the teletext data, the bit is set to 1. Writing 1 to this bit clears the interrupt.

DATE_ISR

DATE_ISR is an interrupt register.

Offset Address	Register Name	Total Reset Value
0xF288	DATE_ISR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															tt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	tt_int	Teletext interrupt. This bit indicates the interrupt status after tt_status is masked by tt_mask.

DATE_COEFF37

DATE_COEFF37 is an up-sampling filtering coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xF294	DATE_COEFF37	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y1_coeff3								fir_y1_coeff2								fir_y1_coeff1								fir_y1_coeff0							
Reset	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[31:24]	RW	fir_y1_coeff3	Coefficient 13 for luminance up-sampling filtering
[23:16]	RW	fir_y1_coeff2	Coefficient 12 for luminance up-sampling filtering
[15:8]	RW	fir_y1_coeff1	Coefficient 11 for luminance up-sampling filtering
[7:0]	RW	fir_y1_coeff0	Coefficient 10 for luminance up-sampling filtering

DATE_COEFF38

DATE_COEFF38 is an up-sampling filtering coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF298	DATE_COEFF38	0x003A_FFDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y2_coeff1																fir_y2_coeff0															

Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff1	Coefficient 21 for luminance up-sampling filtering
[15:0]	RW	fir_y2_coeff0	Coefficient 20 for luminance up-sampling filtering

DATE_COEFF39

DATE_COEFF39 is an up-sampling filtering coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF29C	DATE_COEFF39	0x0148_FF97

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y2_coeff3																fir_y2_coeff2															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff3	Coefficient 23 for luminance up-sampling filtering
[15:0]	RW	fir_y2_coeff2	Coefficient 22 for luminance up-sampling filtering

DATE_COEFF40

DATE_COEFF40 is an up-sampling filtering coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF2A0	DATE_COEFF40	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c1_coeff3								fir_c1_coeff2								fir_c1_coeff1								fir_c1_coeff0							
Reset	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[31:24]	RW	fir_c1_coeff3	Coefficient 13 for chrominance up-sampling filtering
[23:16]	RW	fir_c1_coeff2	Coefficient 12 for chrominance up-sampling filtering
[15:8]	RW	fir_c1_coeff1	Coefficient 11 for chrominance up-sampling filtering
[7:0]	RW	fir_c1_coeff0	Coefficient 10 for chrominance up-sampling filtering

DATE_COEFF41

DATE_COEFF41 is an up-sampling filtering coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF2A4	DATE_COEFF41	0x003A_FFDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c2_coeff1																fir_c2_coeff0															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff1	Coefficient 21 for chrominance up-sampling filtering
[15:0]	RW	fir_c2_coeff0	Coefficient 20 for chrominance up-sampling filtering

DATE_COEFF42

DATE_COEFF42 is an up-sampling filtering coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF2A8	DATE_COEFF42	0x0148_FF97

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c2_coeff3																fir_c2_coeff2															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff3	Coefficient 23 for chrominance up-sampling filtering
[15:0]	RW	fir_c2_coeff2	Coefficient 22 for chrominance up-sampling filtering

DATE_DACDET1

DATE_DACDET1 is DAC automatic detection register 1.

Offset Address	Register Name	Total Reset Value
0xF2C0	DATE_DACDET1	0x000D_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								det_line								reserved				vdac_det_high											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved

[25:16]	RW	det_line	Line of the detected level
[15:10]	RO	reserved	Reserved
[9:0]	RW	vdac_det_high	Detected level

DATE_DACDET2

DATE_DACDET2 is DAC automatic detection register 2.

Offset Address	Register Name	Total Reset Value
0xF2C4	DATE_DACDET2	0x0030_0118

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdac_det_en	reserved							det_pixel_wid								reserved				det_pixel_sta											
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[31]	RW	vdac_det_en	DAC automatic detection enable 0: disabled 1: enabled
[30:27]	RO	reserved	Reserved
[26:16]	RW	det_pixel_wid	Level width
[15:11]	RO	reserved	Reserved
[10:0]	RW	det_pixel_sta	Start position of a line

DATE_COEFF50

DATE_COEFF50 is an over-sampling filtering coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xF2C8	DATE_COEFF50	0x07FF_07FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ovs_coeff1								reserved				ovs_coeff0											

Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 11 for luminance over-sampling filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 10 for luminance over-sampling filtering

DATE_COEFF51

DATE_COEFF51 is an over-sampling filtering coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF2CC	DATE_COEFF51	0x07FF_0204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 21 for luminance over-sampling filtering
[15:11]	RO	reserved	Reserved.
[10:0]	RW	ovs_coeff0	Coefficient 20 for luminance over-sampling filtering

DATE_COEFF52

DATE_COEFF52 is an over-sampling filtering coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF2D0	DATE_COEFF52	0x0000_07FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 31 for luminance over-sampling filtering
[15:11]	RO	reserved	Reserved

[10:0]	RW	ovs_coeff0	Coefficient 30 for luminance over-sampling filtering

DATE_COEFF53

DATE_COEFF53 is an over-sampling filtering coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF2D4	DATE_COEFF53	0x07BF_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 41 for luminance over-sampling filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 40 for luminance over-sampling filtering

DATE_COEFF54

DATE_COEFF54 is an over-sampling filtering coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF2D8	DATE_COEFF54	0x0135_0135

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 51 for luminance over-sampling filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 50 for luminance over-sampling filtering

DATE_COEFF55

DATE_COEFF55 is an over-sampling filtering coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF2DC	DATE_COEFF55	0x000C_07BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ovs_coeff1												reserved				ovs_coeff0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ovs_coeff1	Coefficient 61 for luminance over-sampling filtering
[15:11]	RO	reserved	Reserved
[10:0]	RW	ovs_coeff0	Coefficient 60 for luminance over-sampling filtering

DATE_COEFF56

DATE_COEFF56 is an over-sampling round-off register.

Offset Address	Register Name	Total Reset Value
0xF2E0	DATE_COEFF56	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															oversam2_round_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	oversam2_round_en	Round-off enable during 2x up-sampling 0: disabled 1: enabled

DATE_COEFF57

DATE_COEFF57 is a CVBS gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E4	DATE_COEFF57	0x0080_8080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cvbs_gain_en	reserved							ycvbs_gain								u_gain								v_gain							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	cvbs_gain_en	CVBS gain enable 0: disabled 1: enabled
[30:24]	RO	reserved	Reserved
[23:16]	RW	ycvbs_gain	Gain control of the luminance component Y
[15:8]	RW	u_gain	Gain control of the chrominance component U
[7:0]	RW	v_gain	Gain control of the chrominance component V

DATE_COEFF58

DATE_COEFF58 is a component gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E8	DATE_COEFF58	0x0080_8080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	comp_gain_en	reserved							ycomp_gain								pb_gain								pr_gain							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	comp_gain_en	Component gain enable 0: disabled 1: enabled
[30:24]	RO	reserved	Reserved

[23:16]	RW	ycomp_gain	Gain control of the luminance component Y
[15:8]	RW	pb_gain	Gain control of the chrominance component U
[7:0]	RW	pr_gain	Gain control of the chrominance component V

DATE_COEFF59

DATE_COEFF59 is a clip control register.

Offset Address	Register Name	Total Reset Value
0xF2EC	DATE_COEFF59	0x0001_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															cb_gain_polar	reserved		cr_os_clip_fullrange	cb_os_clip_fullrange	reserved		v_os_clip_fullrange	u_os_clip_fullrange	reserved			y_os_clip_fullrange	reserved		clpf_clip_fullrange	ynotch_clip_fullrange
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	cb_gain_polar	Chrominance subcarrier polarity control 0: negative gain 1: positive gain
[15:14]	RO	reserved	Reserved
[13]	RW	cr_os_clip_fullrange	Clip enable for the Cr component in the up-sampling module 0: disabled 1: enabled
[12]	RW	cb_os_clip_fullrange	Clip enable for the Cb component in the up-sampling module 0: disabled 1: enabled
[11:10]	RO	reserved	Reserved
[9]	RW	v_os_clip_fullrange	Clip enable for the V component in the up-sampling module 0: disabled 1: enabled

[8]	RW	u_os_clip_fullrange	Clip enable for the U component in the up-sampling module 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	y_os_clip_fullrange	Clip enable for the Y component in the up-sampling module 0: disabled 1: enabled
[3:2]	RO	reserved	Reserved
[1]	RW	clpf_clip_fullrange	Clip enable for the chrominance low-pass module 0: disabled 1: enabled
[0]	RW	ynotch_clip_fullrange	Clip enable for the luminance notch module 0: disabled 1: enabled

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11 Audio Encoding

11.1 Overview

The voice engine (VOIE) module encodes, compresses, and outputs 16-bit linear pulse code modulation (PCM) audio data. It supports data inputs at the sampling rate of 8 kHz, 16 kHz, 32 kHz, or 48 kHz and G726, G711A/U, and ADPCM outputs.

11.2 Features

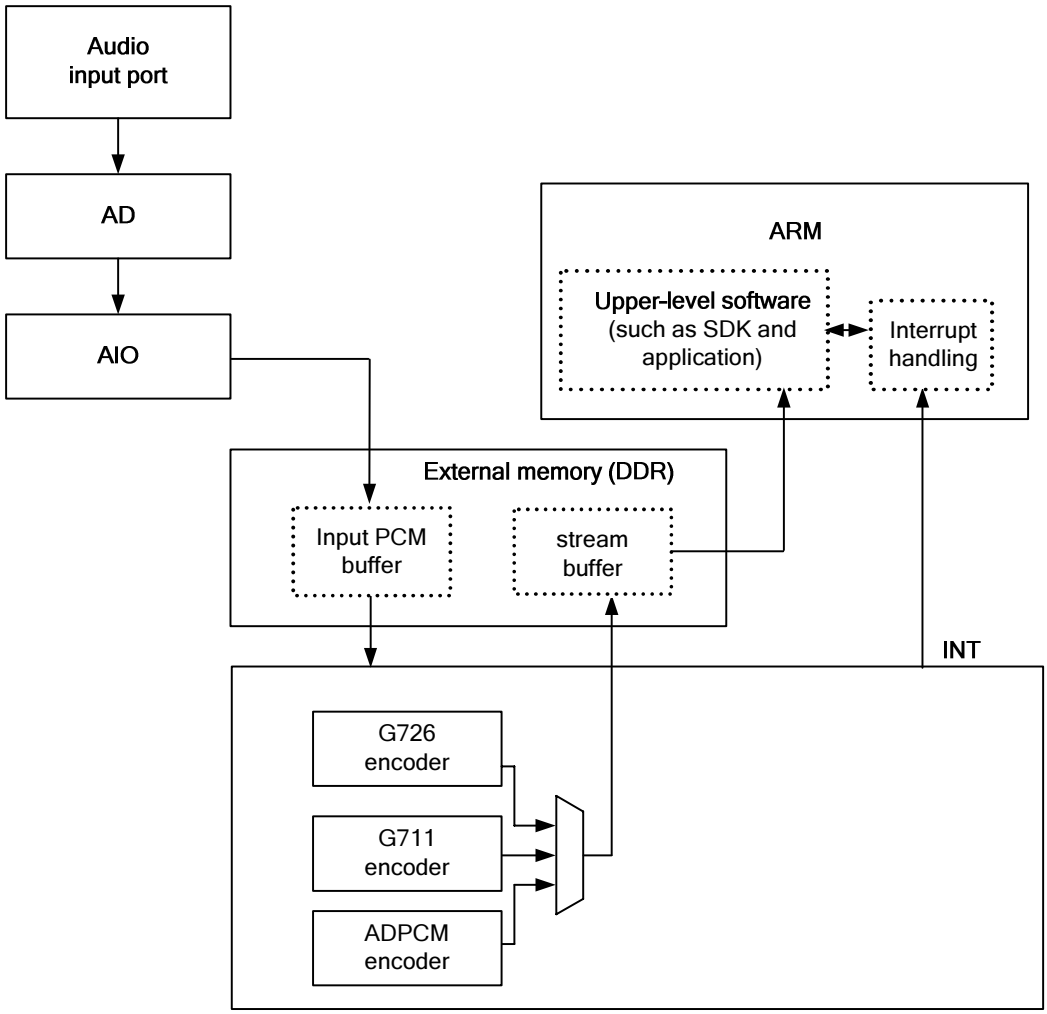
The VOIE module has the following features:

- Inputs audio sampling format which supports 16-bit linear PCM in little endian mode.
- Supports the sampling rate of 8 kHz, 16 kHz, 32 kHz, or 48 kHz.
- Supports the audio frame length of 10 ms, 20 ms, 30 ms, 40 ms, 50 ms, or 60 ms.
- Supports at most 17 input audio channels for each frame (including 16 channels for encoding outputs and one channel for talkback).
- Supports 80–2880 (an integral multiple of 80) input sampling points of each frame.
- Supports the ITU-G.726 protocol providing 40 kbit/s, 32 kbit/s, 24 kbit/s, and 16 kbit/s encoding compression ratios.
- Supports ITU-G.711A/U encoding output.
- Supports the ADPCM encoding outputs in ADPCM_DVI4 and ADPCM_ORG_DVI4 encapsulation modes.
- Supports HiSilicon frame header output after encoding.
- Checks the input frames, discards the frames with errors, and reports interrupts.
- Checks the input frame length and encoding mode, discards the frames incompliant with configuration requirements, and the interrupts.
- Supports encoding of consecutive frames.

11.3 Function Description

Figure 11-1 shows the functional block diagram of the VOIE.

Figure 11-1 Functional Block Diagram of VOIE



The VOIE consists of the G726 encoder, G711 encoder, and ADPCM encoder. The encoder is selected based on the configured encoding mode.

Before the VOIE starts encoding, the audio data is input through the audio-to-digital converter (ADC), and is stored in the audio data buffer over the AIO interface (for details, see the AIO operating mode). Then the data is transferred to the DDR in DMA mode. After encoding, the VOIE stores the encoded streams in the stream buffer, and reports an interrupt, indicating that encoding of a frame of audio data is complete.

For details about encoding modes, see section 11.6 "Register Description."

11.4 Operating Mode

NOTE

Exceptions may occur when packets are discarded during network transmission because the predicted transmission value is unavailable for ADPCM_ORG_DVI4. Therefore, you are advised not to use this protocol for encoding during audio stream network transmission.

The VOIE reads the linked list and voice frame data of a frame from the DDR and writes the streams to the DDR after the data is encoded by the encoder.

Before the VOIE is enabled for video encoding, the software allocates three types of buffers for the VOIE in an external DDR SDRAM:

- Input voice data buffer

  The VOIE reads the voice data to be encoded from this buffer during encoding. This buffer is written by the DMA.

- Encoding linked list configuration buffer

  When VOIE is started but encoding does not start, the VOIE reads the configuration information about the current channel from this buffer. The configuration information includes the data source address, the destination address, the channel variable address, the address of the next channel linked list, and the encoding control configuration information.

- Channel variable buffer

  The VOIE reads channel variables and check information from this buffer during encoding (the information is not required during the G711 encoding.) and refreshes the information after encoding.

  For details about the structures of the linked list and channel variables, see section 11.7 "Linked List Structure." G726_check in Figure 11-4 is the no-carry accumulated sum of the variables of eleven 32-bit channel registers. The value of ADPCM_check in Figure 11-5 is the same as the value of 32-bit channel variable registers in ADPCM encoding mode.

11.5 Register Summary

Table 11-1 describes the VOIE registers.

Table 11-1 Summary of the VOIE registers (base address: 0x1312_0000)

Offset addresses	Register	Description	Page
0x0000	VOIE_INTSTAT	Interrupt status register	11-5
0x0004	VOIE_INTMASK	Interrupt mask register	11-6
0x0008	VOIE_RAWINT	Raw interrupt status register	11-7
0x000C	VOIE_INTCLR	Interrupt clear register	11-7
0x0010	VIOE_START	Encoding start signal register	11-9
0x0014	VOIE_OUTSTDING	Outstanding configuration register	11-9

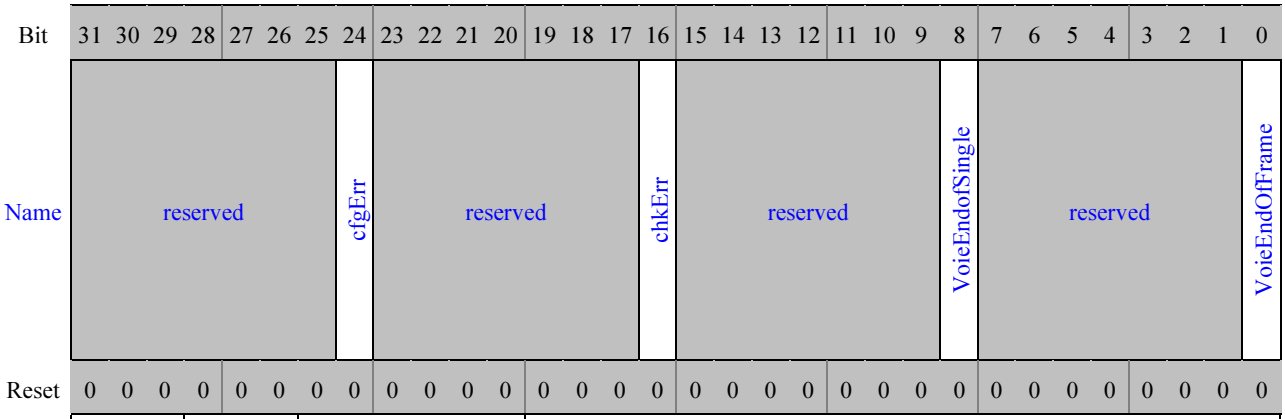
Offset addresses	Register	Description	Page
0x0020	VOIE_MODE	VOIE working mode register	11-10
0x0028	VOIE_CFG	First linked list address register	11-10
0x0030	VOIE_LLICFG0	Linked list member register (SrcPhyAddr)	11-11
0x0034	VOIE_LLICFG1	Linked list member register (DstPhyAddr)	11-11
0x0038	VOIE_LLICFG2	Linked list member register (StatePhyAddr)	11-12
0x003C	VOIE_LLICFG3	Linked list member register (NextLLiAddr)	11-12
0x0040	VOIE_LLICFG4	Linked list member register (StCtrl)	11-13
0x0050	VOIE_LLISTATE0	G726 encoding channel variable register 0	11-15
0x0054	VOIE_LLISTATE1	G726 encoding channel variable register 1	11-15
0x0058	VOIE_LLISTATE2	G726 encoding channel variable register 2	11-16
0x005C	VOIE_LLISTATE3	G726 encoding channel variable register 3	11-16
0x0060	VOIE_LLISTATE4	G726 encoding channel variable register 4	11-17
0x0064	VOIE_LLISTATE5	G726 encoding channel variable register 5	11-17
0x0068	VOIE_LLISTATE6	G726 encoding channel variable register 6	11-18
0x006C	VOIE_LLISTATE7	G726 encoding channel variable register 7	11-18
0x0070	VOIE_LLISTATE8	G726 encoding channel variable register 8	11-19
0x0074	VOIE_LLISTATE9	G726 encoding channel variable register 9	11-19
0x0078	VOIE_LLISTATE10	G726 encoding channel variable register 10	11-20
0x007C	VOIE_STATE_CHK 0	G726 channel variable check register	11-20
0x0080	VOIE_LLISTATE11	ADPCM encoding channel variable register 11	11-21
0x0084	VOIE_STATE_CHK 1	ADPCM channel variable check register	11-21

11.6 Register Description

VOIE_INTSTAT

VOIE_INTSTAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	VOIE_INTSTAT	0x0000_0000



Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24]	RO	cfgErr	Configuration error flag. 0: correct 1: error
[23:17]	RO	reserved	Reserved.
[16]	RO	chkErr	Channel variable check error flag. 0: correct 1: error
[15:9]	RO	reserved	Reserved.
[8]	RO	VoieEndofSingle	Single channel encoding completion flag. 0: incomplete 1: complete
[7:1]	RO	reserved	Reserved.
[0]	RO	VoieEndOfFrame	Frame encoding completion flag. 0: incomplete 1: complete

VOIE_INTMASK

VOIE_INTMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0004	VOIE_INTMASK	0x0101_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							cfgErrMask	reserved							chkErrMask	reserved							VoieEndofSingleMask	reserved							VoieEndOfPicMask
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24]	RW	cfgErrMask	Configuration error flag mask enable. 0: enabled 1: disabled
[23:17]	RO	reserved	Reserved.
[16]	RW	chkErrMask	Check error flag mask enable. 0: enabled 1: disabled
[15:9]	RO	reserved	Reserved.
[8]	RW	VoieEndofSingleMask	Single channel encoding completion mask enable. 0: enabled 1: disabled
[7:1]	RO	reserved	Reserved.
[0]	RW	VoieEndOfPicMask	Frame encoding completion mask enable. 0: enabled 1: disabled

VOIE_RAWINT

VOIE_RAWINT is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0008	VOIE_RAWINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							cfgErr	reserved							chkErr	reserved							VoieEndofSingle	reserved							VoieEndOfFrame
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24]	RO	cfgErr	Configuration error flag. 0: correct 1: incorrect
[23:17]	RO	reserved	Reserved.
[16]	RO	chkErr	Channel variable check error flag. 0: correct 1: error
[15:9]	RO	reserved	Reserved.
[8]	RO	VoieEndofSingle	Single channel encoding completion flag. 0: incomplete 1: complete
[7:1]	RO	reserved	Reserved.
[0]	RO	VoieEndOfFrame	Frame encoding completion flag. 0: incomplete 1: complete

VOIE_INTCLR

VOIE_INTCLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x000C	VOIE_INTCLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							cfgErrClr	reserved							chkErrClr	reserved							VoieEndofSingleClr	reserved							VoieEndOfFrameClr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved.
[24]	WC	cfgErrClr	Configuration error source interrupt clear. Writing 1 clears this bit.
[23:17]	RO	reserved	Reserved.
[16]	WC	chkErrClr	Channel variable check error flag source interrupt clear. Writing 1 clears this bit.
[15:9]	RO	reserved	Reserved.
[8]	WC	VoieEndofSingleClr	Single channel encoding completion source interrupt clear. Writing 1 clears this bit.
[7:1]	RO	reserved	Reserved.
[0]	WC	VoieEndOfFrameClr	Frame encoding completion source interrupt clear. Writing 1 clears this bit.

VIOE_START

VIOE_START is an encoding start signal register.

Offset Address	Register Name	Total Reset Value
0x0010	VIOE_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															Start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved.
[0]	WO	Start	Encoding start signal. 0: not start 1: start

VOIE_OUTSTDING

VOIE_OUTSTDING is an outstanding configuration register.

Offset Address	Register Name	Total Reset Value
0x0014	VOIE_OUTSTDING	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												xxx			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved.
[3:0]	RW	voieoutstd	Outstanding depth of the AXI port. The depth range is 0–7.

VOIE_MODE

VOIE_MODE is a VOIE working mode register.

Offset Address	Register Name	Total Reset Value
0x0020	VOIE_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													memClkGateEn	clkGateEn		reserved							accesslockEn	reserved							timeEn
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved.
[18]	RW	memClkGateEn	Memory clock gating enable. Note: This field is invalid and can be ignored.
[17:16]	RW	clkGateEn	Clock gating enable Note: This field is invalid and can be ignored.
[15:9]	RO	reserved	Reserved.
[8]	RW	accesslockEn	Internal configuration lock enable. Note: This field is invalid and can be ignored.
[7:2]	RO	reserved	Reserved.
[1:0]	RW	timeEn	Timeout check enable. Note: This field is invalid and can be ignored.

VOIE_CFG

VOIE_CFG is a first linked list address register.

Offset Address	Register Name	Total Reset Value
0x0028	VOIE_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AddrOfFirstLLI																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	AddrOfFirstLLI	Address for the first linked list for storing the current audio frame. Note: The address must be configured before encoding and must be 128-bit-aligned.

VOIE_LLICFG0

VOIE_LLICFG0 is a linked list member register (SrcPhyAddr).

Offset Address	Register Name	Total Reset Value
0x0030	VOIE_LLICFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SrcPhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	SrcPhyAddr	Start physical address for storing the voice frame data to be encoded in the DDR. The address must be 128-bit-aligned. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.

VOIE_LLICFG1

VOIE_LLICFG1 is a linked list member register (DstPhyAddr).

Offset Address	Register Name	Total Reset Value
0x0034	VOIE_LLICFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DstPhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DstPhyAddr	The physical address of streams output to the DDR after encoding. The 128-bit address must be aligned. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.

VOIE_LLICFG2

VOIE_LLICFG2 is a linked list member register (StatePhyAddr).

Offset Address	Register Name	Total Reset Value
0x0038	VOIE_LLICFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	StatePhyAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	StatePhyAddr	The physical address for storing the voice frame data to be encoded in the DDR. The address must be 128-bit aligned. This address must be configured during the G726 encoding and ADPCM encoding. As channel variables are not used during the G711 encoding, this register can be ignored. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus. Note: This register is provided only for readback during debugging.

VOIE_LLICFG3

VOIE_LLICFG3 is a linked list member register (NextLLiAddr).

Offset Address	Register Name	Total Reset Value
0x003C	VOIE_LLICFG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NextLLiAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	NextLLiAddr	Memory address of the next channel linked list. The address must be 128-bit aligned. If the current channel is the last channel of this frame, set the next linked list address to 0x00000000; otherwise, the next linked list address cannot be set to 0. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.

VOIE_LLICFG4

VOIE_LLICFG4 is a linked list member register (StCtrl, encoding control).

Offset Address	Register Name	Total Reset Value
0x0040	VOIE_LLICFG4	0x0000_0081

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6 5 4	3 2 1 0
Name	SamplesPerFrame				Codec		hisi_head	reserved	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1	0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:16]	RO	SamplesPerFrame	Number of audio sampling points in the current voice frame. The values range is 80–2880 and the value must an integral multiple of 80. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.

[15:8]	RO	Codec	Encoding type configuration. 0x01: G711 Alaw 0x02: G711 Ulaw 0x03: ADPCM_DIV4 0x04: G726_16 kbps 0x05: G726_24 kbps 0x06: G726_32 kbps 0x07: G726_40 kbps 0x24: MEDIA_G726_16 kbps 0x25: MEDIA_G726_24 kbps 0x26: MEDIA_G726_32 kbps 0x27: MEDIA_G726_40 kbps 0x43: ADPCM_ORG_DIV4 Other values: invalid configuration. If the VOIE receives other configurations, a configuration error interrupt is reported. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.
[7]	RW	hisi_head	Output stream HiSilicon frame header enable. 0: exclude HiSilicon frame header 1: include HiSilicon frame header This bit is set to 0x1 by default. The address is written to the corresponding linked list DDR addresses by the software before encoding and is loaded by the AXI bus after encoding starts. Note: This register is provided only for readback during debugging.
[6:0]	RO	reserved	Reserved.

VOIE_LLISTATE0

VOIE_LLISTATE0 is G726 encoding channel variable register 0.

Offset Address	Register Name	Total Reset Value
0x0050	VOIE_LLISTATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A1																A2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	A1	G726 encoding channel variable. Two-tap pole predictor coefficient 1.
[15:0]	RO	A2	G726 encoding channel variable. Two-tap pole predictor coefficient 2.

VOIE_LLISTATE1

VOIE_LLISTATE1 is G726 encoding channel variable register 1.

Offset Address	Register Name	Total Reset Value
0x0054	VOIE_LLISTATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AP												reserved				PK1	PK2	reserved													TD
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	AP	G726 encoding channel variable. Delay speed control.
[21:16]	RO	reserved	Reserved.
[15]	RO	PK1	G726 encoding channel variable. DQ+SEZ signed bit when the delay is 1.
[14]	RO	PK2	G726 encoding channel variable. DQ+SEZ signed bit when the delay is 2.
[13:1]	RO	reserved	Reserved.
[0]	RO	TD	G726 encoding channel variable. Single audio detection signal.

VOIE_LLISTATE2

VOIE_LLISTATE2 is G726 encoding channel variable register 2.

Offset Address	Register Name	Total Reset Value
0x0058	VOIE_LLISTATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	B1																B2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	B1	G726 encoding channel variable. Six-tap pole predictor coefficient 1.
[15:0]	RO	B2	G726 encoding channel variable. Six-tap pole predictor coefficient 2.

VOIE_LLISTATE3

VOIE_LLISTATE3 is G726 encoding channel variable register 3.

Offset Address	Register Name	Total Reset Value
0x005C	VOIE_LLISTATE3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	B3																B4															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	B3	G726 encoding channel variable. Six-tap pole predictor coefficient 3.
[15:0]	RO	B4	G726 encoding channel variable. Six-tap pole predictor coefficient 4.

VOIE_LLISTATE4

VOIE_LLISTATE4 is G726 encoding channel variable register 4.

Offset Address	Register Name	Total Reset Value
0x0060	VOIE_LLISTATE4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	B5																B6															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	B5	G726 encoding channel variable. Six-tap pole predictor coefficient 5.
[15:0]	RO	B6	G726 encoding channel variable. Six-tap pole predictor coefficient 6.

VOIE_LLISTATE5

VOIE_LLISTATE5 is G726 encoding channel variable register 5.

Offset Address	Register Name	Total Reset Value
0x0064	VOIE_LLISTATE5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DML														reserved		DMS								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	DML	G726 encoding channel variable. F (I) long-term average value of the delay.
[17:16]	RO	reserved	Reserved.
[15:4]	RO	DMS	G726 encoding channel variable. F (I) short-term average value of the delay.
[3:0]	RO	reserved	Reserved.

VOIE_LLISTATE6

VOIE_LLISTATE6 is G726 encoding channel variable register 6.

Offset Address	Register Name	Total Reset Value
0x0068	VOIE_LLISTATE6	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ1												reserved				DQ2												reserved			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	DQ1	G726 encoding channel variable. Quantization difference signal when the delay is 1.
[20:16]	RO	reserved	Reserved.
[15:5]	RO	DQ2	G726 encoding channel variable. Quantization difference signal when the delay is 2.
[4:0]	RO	reserved	Reserved.

VOIE_LLISTATE7

VOIE_LLISTATE7 is G726 encoding channel variable register 7.

Offset Address	Register Name	Total Reset Value
0x006C	VOIE_LLISTATE7	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ3												reserved				DQ4												reserved			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	DQ3	G726 encoding channel variable. Quantization difference signal when the delay is 3.
[20:16]	RO	reserved	Reserved.
[15:5]	RO	DQ4	G726 encoding channel variable. Quantization difference signal when the delay is 4.
[4:0]	RO	reserved	Reserved.

VOIE_LLISTATE8

VOIE_LLISTATE8 is G726 encoding channel variable register 8.

Offset Address	Register Name	Total Reset Value
0x0070	VOIE_LLISTATE8	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DQ5												reserved				DQ6												reserved			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	DQ5	G726 encoding channel variable. Quantization difference signal when the delay is 5.
[20:16]	RO	reserved	Reserved.
[15:5]	RO	DQ6	G726 encoding channel variable. Quantization difference signal when the delay is 6.
[4:0]	RO	reserved	Reserved.

VOIE_LLISTATE9

VOIE_LLISTATE9 is G726 encoding channel variable register 9.

Offset Address	Register Name	Total Reset Value
0x0074	VOIE_LLISTATE9	0x0400_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SR1												reserved				SR2												reserved			
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	SR1	G726 encoding channel variable. Reconstruction signal when the delay is 1.
[20:16]	RO	reserved	Reserved.
[15:5]	RO	SR2	G726 encoding channel variable. Reconstruction signal when the delay is 2.
[4:0]	RO	reserved	Reserved.

VOIE_LLISTATE10

VOIE_LLISTATE10 is G726 encoding channel variable register 10.

Offset Address	Register Name	Total Reset Value
0x0078	VOIE_LLISTATE10	0x1100_0220

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	YL																				YU											
Reset	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	YL	G726 encoding channel variable. Low-speed quantization scaling factor.
[12:0]	RO	YU	G726 encoding channel variable. High-speed quantization scaling factor.

VOIE_STATE_CHK0

VOIE_STATE_CHK0 is a G726 channel variable check register.

Offset Address	Register Name	Total Reset Value
0x007C	VOIE_STATE_CHK0	0x2100_1220

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	g726_check																															
Reset	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	g726_check	G726 channel variable check result.

VOIE_LLISTATE11

VOIE_LLISTATE11 is ADPCM encoding channel variable register 11.

Offset Address	Register Name	Total Reset Value
0x0080	VOIE_LLISTATE11	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	valprev				reserved		index	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	valprev	ADPCM encoding channel variable, indicating the reconstruction value of the previous audio point.
[15:8]	RO	reserved	Reserved.
[7:0]	RO	index	ADPCM encoding channel variable, indicating the index value of the quantization table.

VOIE_STATE_CHK1

VOIE_STATE_CHK1 is an ADPCM channel variable check register.

Offset Address	Register Name	Total Reset Value
0x0084	VOIE_STATE_CHK1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	adpcm_check							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	adpcm_check	ADPCM channel variable check result.

11.7 Linked List Structure

Figure 11-2 shows the structure and arrangement mode of the linked list in the DDR. The linked list must be written to the DDR, and the first linked list address must be written to the VOIE_CFG register whose base address is 0x2064_0028.

The structure of the linked list is as follows:

```
typedef struct hiVOICE_ENGINE_LLI_STATE
{
    HI_U32          u32SrcPhyAddr;
    HI_U32          u32DstPhyAddr;
```

```
    HI_U32          u32StatePhyAddr;
    HI_U32          u32NextLLiAddr;
    VOICE_ENGINE_Ctrl stCtrl;
    HI_U32          u32Reserved0;
    HI_U32          u32Reserved1;
    HI_U32          u32Reserved2;
} VOICE_ENGINE_LLI_STATE;
```

Figure 11-2 Structure of the corresponding linked list

Address increment

Number of Bits	Storage Content	Description
32	SrcPhyAddr	Physical address of the memory for storing the encoding input data. The address must be 128-bit aligned.
32	DstPhyAddr	Physical address of the memory for storing the encoding output data. The address must be 128-bit aligned.
32	StatePhyAddr	Physical address of the memory for storing the encoding channel variables . The address must be 128-bit aligned.
32	NextLLiAddr	Address of the next encoding linked list. The address must be 128-bit aligned.
32	StCtrl	Encoding control architecture
32	Reserved0	Reserved for expansion
32	Reserved1	Reserved for expansion
32	Reserved2	Reserved for expansion

Figure 11-3 Storage structure of the StCrtl

Content	Reserved	hisi_head	Codec	Samples per frame
Bit Allocation	6:0	7	15:8	31:16

Figure 11-4 Channel variable structure of the G726

Reserved to 0

Number of Bits	Storage Content	Description
32	A1[15:0] A2[15:0]	[31:16] [15:0]
32	AP[9:0] PK1 PK2 TD	[31:22] [15] [14] [0]
32	B1[15:0] B2[15:0]	[31:16] [15:0]
32	B3[15:0] B4[15:0]	[31:16] [15:0]
32	B5[15:0] B6[15:0]	[31:16] [15:0]
32	DML[13:0] DMS[11:0]	[31:18] [15:4]
32	DQ1[10:0] DQ2[10:0]	[31:21] [15:5]
32	DQ3[10:0] DQ4[10:0]	[31:21] [15:5]
32	DQ5[10:0] DQ6[10:0]	[31:21] [15:5]
32	SR1[10:0] SR2[10:0]	[31:21] [15:5]
32	YL[18:0] YU[12:0]	[31:13] [12:0]
32	G726_check	[31:0]

Address increment

Figure 11-5 Channel variable structure of the ADPCM

Reserved to 0

Number of Bit	Storage Content	Description
32	valprev[15:0] index[7:0]	[31:16] [7:0]
32	adpcm_check	[31:0]

Address decrement

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12 Audio Interfaces

12.1 AIAO

12.1.1 Overview

The audio input/ audio output (AIAO) interface is used to connect to the off-chip audio CODEC to input and output audio data, implementing the recording, talkback, and playback functions. The Hi3521A has an integrated AIAO interface that includes two audio input ports (AIPs) and two audio output ports (AOPs). AIP0 or AIP1 supports 2-, 4-, 8-, or 16-channel 8-bit or 16-bit audio inputs in time division multiplexing (TDM) mode, 2-channel 16-bit or 24-bit inter-IC sound (I^2S) audio inputs in non-TDM mode, and 2-channel 8-bit or 16-bit pulse code modulation (PCM) audio inputs in non-TDM mode. AOP0 or AOP1 supports 1- or 2-channel 16-bit or 24-bit audio outputs. AOP1 connects to the internal high definition multimedia interface (HDMI) over the I^2S interface.

NOTE

- AOP0 corresponds to audio TX channel 0 and AOP1 corresponds to audio TX channel 1.
- AIP0 corresponds to audio RX channel 0 and AIP1 corresponds to audio RX channel 1.

12.1.2 Features

The AIAO interface supports the PCM mode and I^2S mode. The AIAO interface reads data from or writes data to the memory in DMA mode.

I²S Interfaces

The I^2S interfaces have the following features:

- Support the master/slave mode.
- Transmit or receive 16- or 24-bit data of the audio-left and audio-right channels in non-TDM mode.
- Receive 8- or 16-bit data from two, four, eight, or 16 channels in TDM mode.
- Support the sampling rate ranging from 8 kHz to 192 kHz.
- Separately enable or disable the input (AIP0/AIP1) and output (AOP0/AOP1).
- Support DMA for the input (AIP0/AIP1) and output (AOP0/AOP1). The AIAO reads data from and writes data to a cyclic buffer created by using software. The cyclic buffer size and threshold are adjustable.

PCM Interfaces

The PCM interfaces have the following features:

- Support the master/slave mode.
- Transmit/receive the 8- or 16-bit linear PCM code from a channel.
- Receive 8- or 16-bit data from two, four, eight or sixteen channels.
- Support the bit stream clocks and frame sync signals internally generated and external clocks and sync signals.
- Support only short pulse sync signals in frame sync signals (the duration of those sync signals is one clock cycle). The PCM interfaces can work in both the standard mode and customized mode.
- Separately enable or disable the input (AIP0/AIP1) and output (AOP0/AOP1).
- Support DMA for the input (AIP0/AIP1) and output (AOP0/AOP1). The AIAO reads data from and writes data to a cyclic buffer created by using software. The cyclic buffer size and threshold are adjustable.

12.1.3 Function Description

Typical Application

The Hi3521A provides two AIPs and two AOPs, as shown in Figure 12-1. Their functions are as follows:

- AIP0 or AIP1 is used for receiving 8- or 16-bit data from two, four, eight, or 16 channels.
- AIP0 or AIP1 is used for receiving 16- or 24-bit data from two channels.
- AOP0 is used for playing 16- or 24-bit audio data from two channels.
- AOP1 is used for interconnecting with the HDMI over the I^2S interface in master mode. Figure 12-2 shows the interconnection between AOP1 and the HDMI.

Figure 12-1 I^2S channel connection over the AIP and AOPs

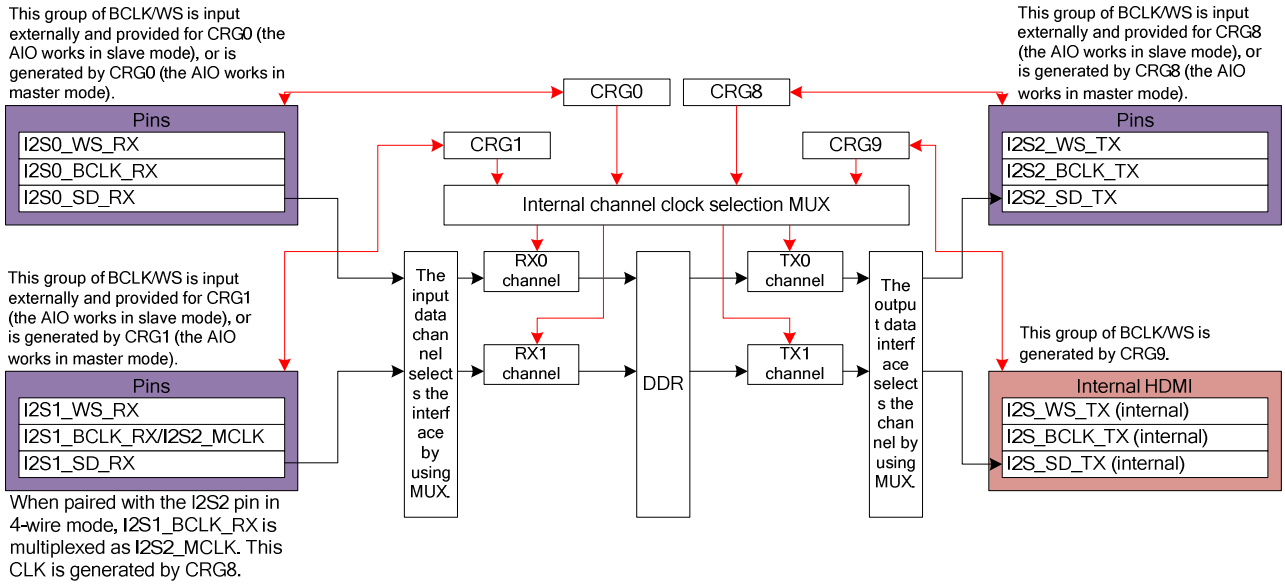
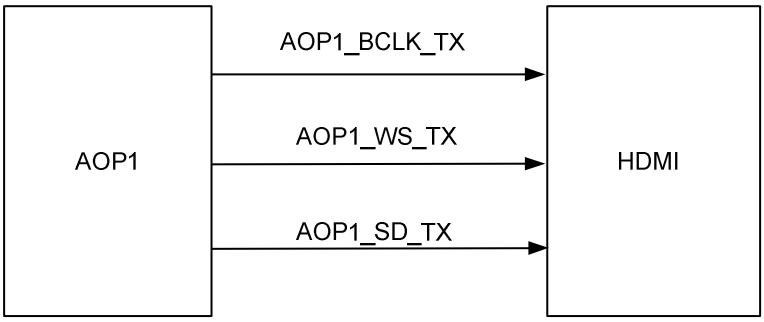


Figure 12-2 Connection between AOP1 and the HDMI



AIP0, AIP1 and AOP0 support both the master and slave modes. The following describes the typical connections over the I^{2}S/PCM interface in master or slave mode.

Figure 12-3 and Figure 12-4 show the typical connections over the I^{2}S/PCM interface in master mode.

NOTE

- In Figure 12-3, AIP1 and AOP0connect to the I2S interface of the audio CODEC in 6-wire mode. The 6-wire mode means that the TX and RX have independent bit stream clock (BCLK) and audio channel select signal (WS).
- In Figure 12-4, AIP1 and AOP0 connect to the I2S interface of the audio CODEC in 4-wire mode. The 4-wire mode means that the TX and RX share the BCLK and WS.
- In master mode, the BCLK and WS (sync signal in PCM mode) are sent to the audio CODEC by the AIAO module.

Figure 12-3 Connection diagram over the 6-wire I^{2}S/PCM interface in master mode

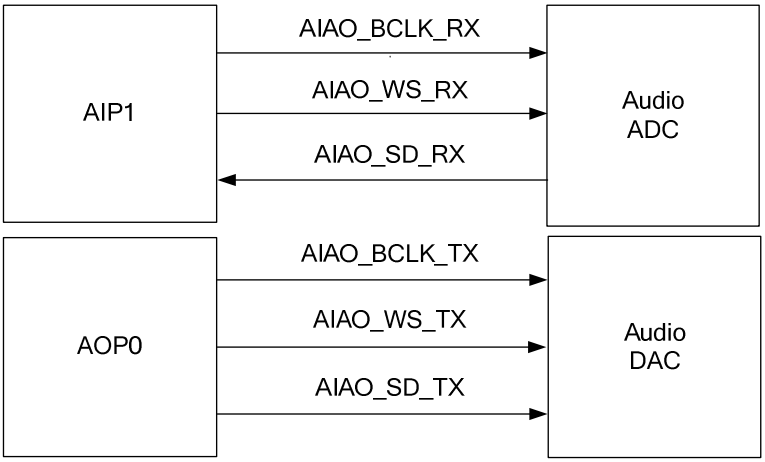


Figure 12-4 Connection diagram over the 4-wire I²S/PCM interface in master mode

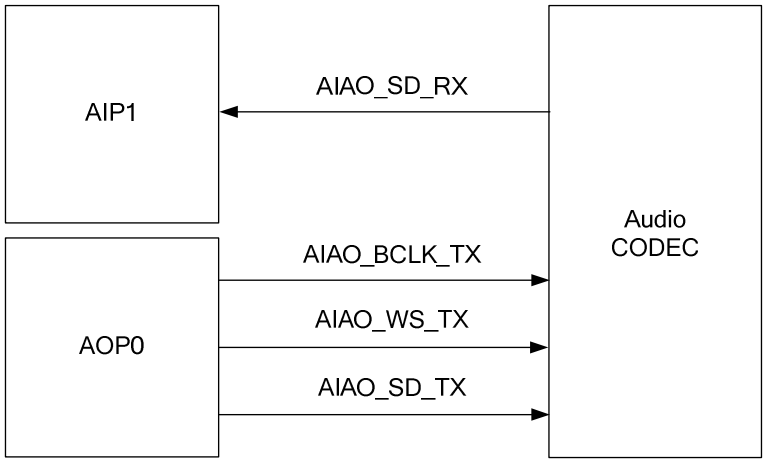


Figure 12-5 and Figure 12-6 show the typical connections over the I²S/PCM interface in slave mode.

NOTE

- In Figure 12-5, AIP1 and AOP0 connect to the I2S interface of the audio CODEC in 6-wire mode. The 6-wire mode means that the TX and RX have independent BCLK and WS.
- In Figure 12-6, AIP1 and AOP0 connect to the I2S interface of the audio CODEC in 4-wire mode. The 4-wire mode means that the TX and RX share the BCLK and WS.
- In slave mode, the BCLK and WS (sync signal in PCM mode) are sent to the AIAO module by the audio CODEC. The working clock of the external audio CODEC is provided by the AIAO_MCLK output by the Hi3521A or provided by the external crystal oscillator.

Figure 12-5 Connection diagram over the 6-wire I²S/PCM interface in slave mode

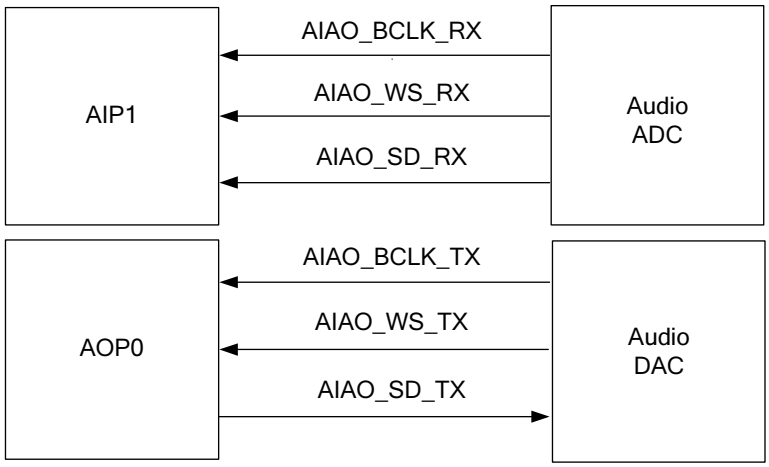
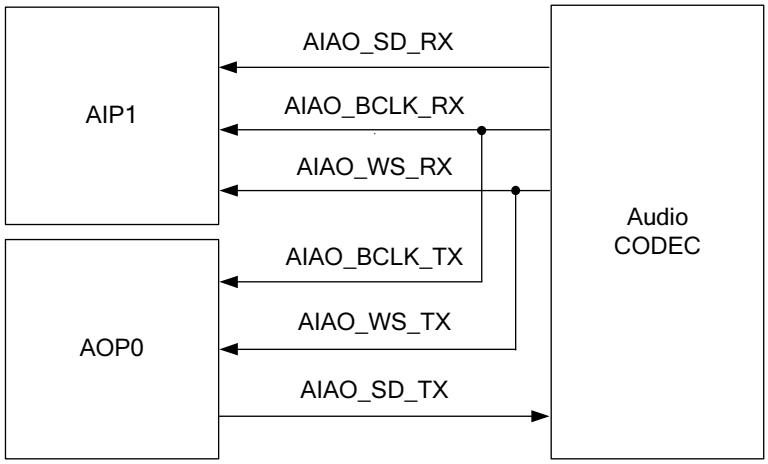


Figure 12-6 Connection diagram over the 4-wire I²S/PCM interface in slave mode



Function Principle

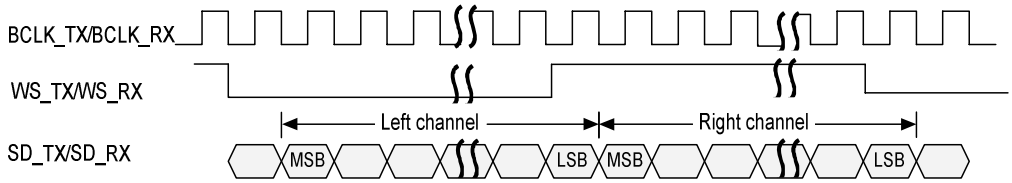
The AIP1 receives the audio data after the analog-to-digital (AD) conversion performed by the audio CODEC over the I²S or PCM interface and stores the data into the cyclic FIFO created for the AIP1. Then, the CPU fetches the data and stores it. In this way, audio recording is complete.

AOP0 reads audio data from the cyclic buffer and sends the audio data to the interconnected audio CODEC over the I²S or PCM interface at a specified sampling rate. The audio CODEC performs digital-to-analog (DA) conversion on the audio data and plays the audio.

The data transferred over the I²S interface consists of the audio-left channel data and audio-right channel data, which is distinguished by the levels of the WS_TX and WS_RX signals, as shown in Figure 12-7. Data is sampled on the rising edge and transmitted on the falling edge of the BCLK_TX/BCLK_RX clock according to the protocol. The most significant bit (MSB) is valid in the next clock cycle of WS_TX/WS_RX. The data is transferred from the MSB to the LSB.

Figure 12-7 shows the timing of the I²S interface.

Figure 12-7 I²S interface timing



The data transferred over the PCM interface is the single-channel data. WS_TX/WS_RX identifies the start position of the data. The MSB is transmitted or received first. Data is sampled on the rising edge and transmitted on the falling edge. Data can also be sampled on the falling edge and transmitted on the rising edge if the BCLK clock is inversed through register configuration. In standard timing mode, the MSB is valid in the next cycle after the high-level pulse of WS_TX/WS_RX. In customized timing mode, the position of the MSB

can be configured based on PCM_OFFSET. When PCM_OFFSET is 0, the MSB is aligned with the high-level pulse of WS_TX/WS_RX.

Figure 12-8 shows the timing of the PCM interface in standard mode.

Figure 12-8 Timing of the PCM interface in standard mode

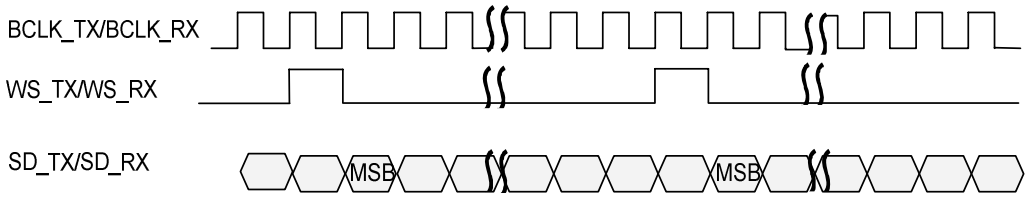
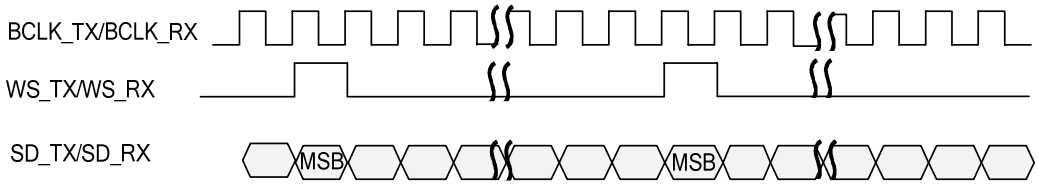


Figure 12-9 shows the timing of the PCM interface in customized mode when PCM_OFFSET is 0.

Figure 12-9 Timing of the PCM interface in customized mode (PCM_OFFSET = 0)



When receiving 2-/4-/8-/16-channel 8-/16-bit data, the I^2S interface stores the data into the left and right channels respectively, as shown in Figure 12-10.

Figure 12-10 Receiving 2-/4-/8-/16-channel data over the I^2S interface

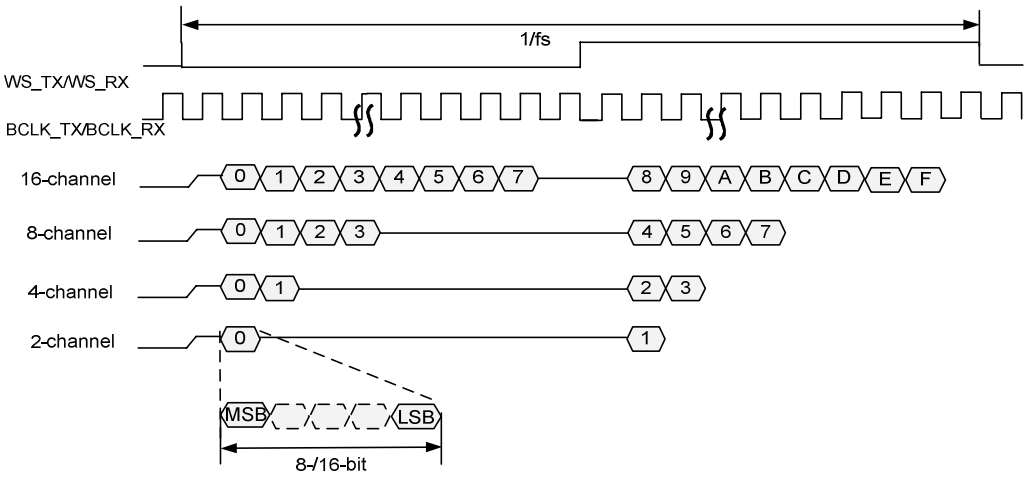
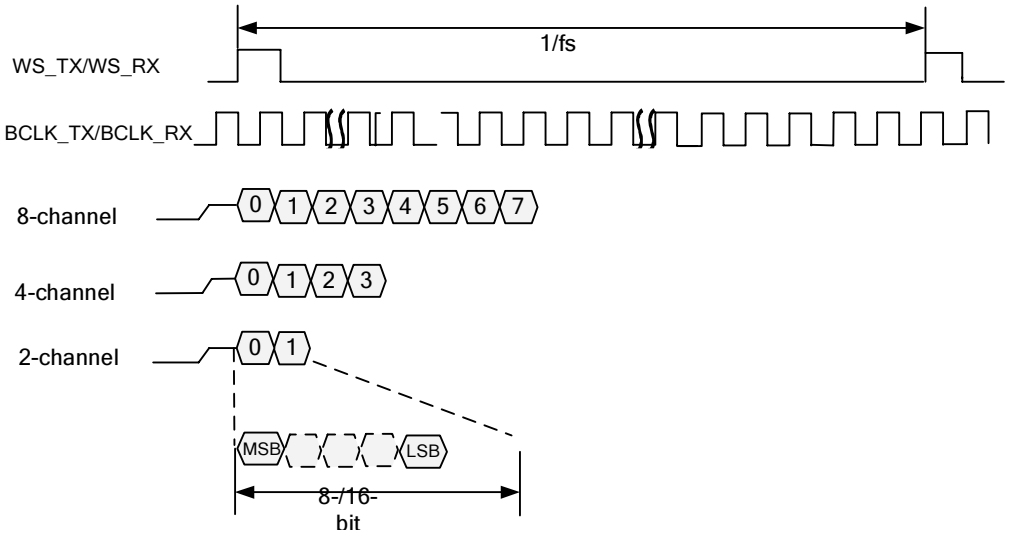


Figure 12-11 shows how data from multiple channels is received in PCM mode. Both the standard and customized PCM modes are supported. The AIAO interface can receive data on the rising edge or falling edging. Figure 12-11 shows how the AIAO interface receives data on the rising edge in PCM mode.

Figure 12-11 Receiving 2-/4-/8-/16-channel data over the PCM interface



12.1.4 Operating Mode

Clock Gating and Configuration

Before enabling the AIAO interface for audio recording or playback, you must enable the clock gating of related channels (AIP0, AIP1, AOP0 and AOP1). The typical configuration is as follows:

- If AOP1 connects to the HDMI audio interface, AOP1 must work in master mode. That is, AOP1 is enabled only after I2S_CRG_CFG0_09 and I2S_CRG_CFG1_09 are configured.
- If AIP1 is used for audio recording and AOP0 is used for audio playback and they connect to an external CODEC in 4-wire mode, their working mode can be set to master or slave mode. BCLK8 is used as the RX and TX channels of the external CODEC. AIP1 and AOP0 are enabled only after I2S_CRG_CFG0_08 and I2S_CRG_CFG1_08 are configured.
- If AIP1 is used for audio recording and AOP0 is used for audio playback and they connect to an external CODEC in 6-wire mode, their working mode can be set to master or slave mode. BCLK0 and BCLK8 are used as the RX channel and TX channel of the external CODEC respectively. AIP1 and AOP0 are enabled only after I2S_CRG_CFG0_00, I2S_CRG_CFG1_00, I2S_CRG_CFG0_08, and I2S_CRG_CFG1_08 are configured.

Soft Reset

The internal channels (AIP0, AIP1, AOP0 and AOP1) of the AIAO module do not support separate soft reset. When the AIAO module is reset, the four channels are reset at the same time.

Recording Process

The following example assumes that the audio channels are stereo channels in I^2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits, the AIAO PLL clock source is a

500 MHz clock, and the AIAO clock of the system controller is enabled. To record data, perform the following steps:

Step 1 Set I2S_CRG_CFG0_08 to 0x003254E7 to set the channel-8 MCLK to 12.288 MHz.

Step 2 Set I2S_CRG_CFG1_08 to 0x00000133 to enable the channel-8 clock, set the BCLK to the divide-by-4 clock of the MCLK, and set the FCLK to the divide-by-64 clock of the BCLK. The FCLK is 48 kHz.

Step 3 Set AIAO_SWITCH_RX_BCLK to 0x00000008 to set the working clock of the RX channel to channel-8 clock.

Step 4 Set RX_IF_ATTRI to 0xe4800005 to set the operating mode of the RX channel to I^2S stereo mode and sampling precision to 16 bits.

Step 5 Configure RX_BUFF_SADDR to set a 24-bit start address for the allocated DDR (for example, 0x0085fe81), set RX_BUFF_SIZE to the size of the allocated DDR buffer (for example, 0x0000f000), set RX_BUFF_WPTR and RX_BUFF_RPTR to 0x0 to initialize the write and read pointers, and set RX_TRANS_SIZE to the data transfer length (for example, 0x00000f00).

Step 6 Configure RX_INT_ENA to enable the corresponding interrupt of the RX channel as required. For example, set RX_INT_ENA to 0x00000001 to enable the trans_int interrupt.

Step 7 Set RX_DSP_CTRL to 0x10000000 to enable the RX channel. Then the RX channel starts recording.

Step 8 Read RX_BUFF_WPTR and RX_BUFF_RPTR to check the empty/full status of the cyclic buffer and the valid data amount.

Ensure that data is fetched before the cyclic buffer is full and the updated read address for the cyclic buffer is written to RX_BUFF_RPTR. Otherwise, overflow occurs in the cyclic buffer and the audio is discontinuous.

Step 9 After recording, write 0x00000000 to RX_DSP_CTRL and query RX_DSP_CTRL until its value is 0x20000000, which indicates that the RX channel stops working.

----End

CAUTION

Configure the AIP0/AIP1 clock before starting the AIP0/AIP1, ensuring that AIAO_BCLK_RX and AIAO_WS_RX are normal.

Playback Process

The playback processes for the AOP0 and AOP1 are the same. The following uses AOP0 as an example and assumes that the audio channels are stereo channels in I^2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits, the AIAO PLL clock source is a 500 MHz clock, and the AIAO clock of the system controller is enabled. To play data, perform the following steps:

Step 1 Set I2S_CRG_CFG0_08 to 0x003254E7 to set the channel-8 MCLK to 12.288 MHz.

Step 2 Set I2S_CRG_CFG1_08 to 0x00000133 to enable the channel-8 clock, set the BCLK to the divide-by-4 clock of the MCLK, and set the FCLK to the divide-by-64 clock of the BCLK. The FCLK is 48 kHz.

Step 3 Set AIAO_SWITCH_TX_BCLK to 0x00000008 to set the working clock of the RX channel to channel-8 clock.

Step 4 Set TX_IF_ATTRI to 0xe4000005 to set the operating mode of the RX channel to I^2S stereo mode and sampling precision to 16 bits.

Step 5 Set TX_BUFF_SADDR to the start address for the allocated buffer (for example, 0x00452548), set TX_BUFF_SIZE to the size of the allocated buffer, set TX_BUFF_WPTR and TX_BUFF_RPTR to 0x0, and set TX_TRANS_SIZE to the data transfer length. For details, see step 5 in the "Recording Process" section.

Step 6 Configure TX_INT_ENA to enable the corresponding interrupt of the RX channel as required. For example, set TX_INT_ENA to 0x00000001 to enable the trans_int interrupt.

Step 7 Set TX_DSP_CTRL to 0x10000000 to enable the playback channel.

Step 8 Read TX_BUFF_WPTR and TX_BUFF_RPTR to check the empty/full status of the cyclic buffer and the valid data amount.

Ensure that new audio data is stuffed before the cyclic buffer is empty and the updated write address for the cyclic buffer is written to TX_BUFF_WPTR. Otherwise, an underflow occurs in the cyclic buffer and the audio is discontinuous.

Step 9 After playback, write 0x00000000 to TX_DSP_CTRL to stop the playback channel and query TX_DSP_CTRL until its value is 0x20000000, which indicates that the playback channel stops working.

----End

CAUTION

- Configure AOP0 clock before starting AOP0, ensuring that AIAO_BCLK_TX and AIAO_WS_TX are normal. This requirement also applies to AOP1.
- Ensure that the available space of the AOP0 cyclic buffer is greater than or equal to 32 bytes when writing data to the cyclic buffer and updating TX_BUFF_WPTR. This requirement also applies to AOP1.

12.1.5 Register Summary

Table 12-1 describes the value ranges and meanings of variables in the offset addresses for AIAO registers.

Table 12-1 Variables in the offset addresses for AIAO register

Variable	Value Range	Description
m	0 or 1	TX channel ID
n	0 or 1	RX channel ID

Table 12-2 describes AIAO registers.

Table 12-2 Summary of AIAO registers (base address: 0x1314_0000)

Offset Address	Register	Description	Page
0x0000	AIAO_INT_ENA	AIAO interrupt enable register	12-12
0x0004	AIAO_INT_STATUS	AIAO interrupt status register	12-13
0x0008	AIAO_INT_RAW	AIAO raw interrupt register	12-14
0x0028	AIAO_SWITCH_RX_BCLK	AIAO I^2S RX BCLK switch configuration register	12-14
0x002C	AIAO_SWITCH_TX_BCLK	AIAO I^2S TX BCLK switch configuration register	12-15
0x0030	AIAO_STATUS	AIAO status register	12-16
0x0034	VHB_OUTSTANDING	VHB outstanding configuration register	12-16
0x0100	I2S_CRG_CFG0_00	I^2S00 CRG configuration register 0	12-17
0x0104	I2S_CRG_CFG1_00	I^2S00 CRG configuration register 1	12-17
0x0108	I2S_CRG_CFG0_01	I^2S01 CRG configuration register 0	12-19
0x010C	I2S_CRG_CFG1_01	I^2S01 CRG configuration register 1	12-20
0x0140	I2S_CRG_CFG0_08	I^2S08 CRG configuration register 0	12-21
0x0144	I2S_CRG_CFG1_08	I^2S08 CRG configuration register 1	12-22
0x0148	I2S_CRG_CFG0_09	I^2S09 CRG configuration register 0	12-23
0x014C	I2S_CRG_CFG1_09	I^2S09 CRG configuration register 1	12-24
0x1000 + 0x100 x *n*	RX_IF_ATTRI	Interface attribute configuration register for the RX channel	12-26
0x1004 + 0x100 x *n*	RX_DSP_CTRL	RX channel control register	12-28
0x1080 + 0x100 x *n*	RX_BUFF_SADDR	DDR buffer start address register for the RX channel	12-28
0x1084 + 0x100 x *n*	RX_BUFF_SIZE	DDR buffer size register for the RX channel	12-29
0x1088 + 0x100 x *n*	RX_BUFF_WPTR	DDR buffer write address register for the RX channel	12-29
0x108C + 0x100 x *n*	RX_BUFF_RPTR	DDR buffer read address register for the RX channel	12-30

Offset Address	Register	Description	Page
0x1090 + 0x100 x *n*	RX_BUFF_ALFULL_TH	DDR buffer almost full threshold register for the RX channel	12-30
0x1094 + 0x100 x *n*	RX_TRANS_SIZE	Data transfer length register for the RX channel	12-31
0x1098 + 0x100 x *n*	RX_WPTR_TMP	Write address storage register for the RX channel upon reporting of the transfer completion interrupt	12-31
0x10A0 + 0x100 x *n*	RX_INT_ENA	Interrupt enable register for the RX channel	12-32
0x10A4 + 0x100 x *n*	RX_INT_RAW	Raw interrupt register for the RX channel	12-33
0x10A8 + 0x100 x *n*	RX_INT_STATUS	Interrupt status register for the RX channel	12-34
0x10AC + 0x100 x *n*	RX_INT_CLR	Interrupt clear register for the RX channel	12-35
0x2000 + 0x100 x *m*	TX_IF_ATTRI	Interface attribute configuration register for the TX channel	12-36
0x2004 + 0x100 x *m*	TX_DSP_CTRL	TX channel control register	12-38
0x2010 + 0x100 x *m*	TX_DMAR_STATUS	TX DMAW status register	12-40
0x2020 + 0x100 x *m*	TX_WS_CNT	WS cyclic count status register for the TX channel	12-41
0x2024 + 0x100 x *m*	TX_BCLK_CNT	BCLK cyclic count status register for the TX channel	12-41
0x2080 + 0x100 x *m*	TX_BUFF_SADDR	DDR buffer start address register for the TX channel	12-42
0x2084 + 0x100 x *m*	TX_BUFF_SIZE	DDR buffer size register for the TX channel	12-42
0x2088 + 0x100 x *m*	TX_BUFF_WPTR	DDR buffer write address register for the TX channel	12-42
0x208C + 0x100 x *m*	TX_BUFF_RPTR	DDR buffer read address register for the TX channel	12-43
0x2090 + 0x100 x *m*	TX_BUFF_ALEMPTY_TH	DDR buffer almost empty threshold register for the TX channel	12-44
0x2094 + 0x100 x *m*	TX_TRANS_SIZE	Data transfer length register for the TX channel	12-44

Offset Address	Register	Description	Page
0x2098 + 0x100 x *m*	TX_RPTR_TMP	Read address storage register for the TX channel upon reporting of the transfer completion interrupt	12-45
0x20A0 + 0x100 x *m*	TX_INT_ENA	Interrupt enable register for the TX channel	12-45
0x20A4 + 0x100 x *m*	TX_INT_RAW	Raw interrupt register for the TX channel	12-46
0x20A8 + 0x100 x *m*	TX_INT_STATUS	Interrupt status register for the TX channel	12-47
0x20AC + 0x100 x *m*	TX_INT_CLR	Interrupt clear register for the TX channel	12-49

12.1.6 Register Description

AIAO_INT_ENA

AIAO_INT_ENA is an AIAO interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0000	AIAO_INT_ENA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18	17	16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved				tx_ch1_int_ena	tx_ch0_int_ena	reserved				rx_ch1_int_ena	rx_ch0_int_ena
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	tx_ch1_int_ena	TX channel 1 interrupt enable 0: disabled 1: enabled
[16]	RW	tx_ch0_int_ena	TX channel 0 interrupt enable 0: disabled 1: enabled
[15:2]	RW	reserved	Reserved

[1]	RW	rx_ch1_int_ena	RX channel 1 interrupt enable 0: disabled 1: enabled
[0]	RW	rx_ch0_int_ena	RX channel 0 interrupt enable 0: disabled 1: enabled

AIAO_INT_STATUS

AIAO_INT_STATUS is an AIAO interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	AIAO_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														tx_ch1_int_status	tx_ch0_int_status	reserved														rx_ch1_int_ena	rx_ch0_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	tx_ch1_int_status	Interrupt status of TX channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	tx_ch0_int_status	Interrupt status of TX channel 0 0: No interrupt is generated. 1: An interrupt is generated.
[15:2]	RO	reserved	Reserved
[0]	RO	rx_ch1_int_status	Interrupt status of RX channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_ch0_int_status	Interrupt status of RX channel 0 0: No interrupt is generated. 1: An interrupt is generated.

AIAO_INT_RAW

AIAO_INT_RAW is an AIAO raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	AIAO_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														tx_ch1_int_status	tx_ch0_int_status	reserved														rx_ch1_int_ena	rx_ch0_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	tx_ch1_int_raw	Raw interrupt of TX channel 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	RO	tx_ch0_int_raw	Raw interrupt of TX channel 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:2]	RO	reserved	Reserved
[1]	RO	rx_ch1_int_raw	Raw interrupt of RX channel 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	rx_ch0_int_raw	Raw interrupt of RX channel 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.

AIAO_SWITCH_RX_BCLK

AIAO_SWITCH_RX_BCLK is an AIAO I^2S RX BCLK switch configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	AIAO_SWITCH_RX_BCLK	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								inner_bclk_ws_sel_rx_01				inner_bclk_ws_sel_rx_00			

Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	inner_bclk_ws_sel_rx_01	Internal BCLK select for the RX channel 1 0000: BCLK0 0001: BCLK1 1000: BCLK8 1001: BCLK9 Other values: reserved
[3:0]	RW	inner_bclk_ws_sel_rx_00	Internal BCLK select for the RX channel 0 0000: BCLK0 0001: BCLK1 1000: BCLK8 1001: BCLK9 Other values: reserved

AIAO_SWITCH_TX_BCLK

AIAO_SWITCH_TX_BCLK is an AIAO I^2S TX BCLK switch configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	AIAO_SWITCH_TX_BCLK	0x7654_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								inner_bclk_ws_sel_tx_01				inner_bclk_ws_sel_tx_00			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	inner_bclk_ws_sel_tx_01	Internal BCLK select for TX channel 1 0000: BCLK0 0001: BCLK1 1000: BCLK8 1001: BCLK9 Other values: reserved

[3:0]	RW	inner_bclk_ws_sel_tx_00	Internal BCLK select for TX channel 0 0000: BCLK0 0001: BCLK1 1000: BCLK8 1001: BCLK9 Other values: reserved

AIAO_STATUS

AIAO_STATUS is an AIAO status register.

Offset Address	Register Name	Total Reset Value
0x0030	AIAO_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															srst_rdy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	srst_rdy	Soft reset status 0: resetting 1: reset completed

VHB_OUTSTANDING

VHB_OUTSTANDING is a VHB outstanding configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	VHB_OUTSTANDING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														vhb_outst_num	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	WO	vhb_outst_num	Number of VHB outstandings The recommended value is 3.

I2S_CRG_CFG0_00

I2S_CRG_CFG0_00 is I^{2}S00 CRG configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0100	I2S_CRG_CFG0_00	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				aiao_mclk_div																											
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RW	aiao_mclk_div	Clock divider of the MCLK. The configured value is calculated as follows: (Frequency of the target MCLK clock/Frequency of the MCLK PLL source clock) x 2^27. For details about the frequency of the MCLK PLL source clock, see section 3.2 "Clock" in chapter 3 "System."

I2S_CRG_CFG1_00

I2S_CRG_CFG1_00 is I^{2}S00 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0104	I2S_CRG_CFG1_00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		aiao_bclkout_pctrl	aiao_bclkin_pctrl	aiao_bclk_sel	aiao_bclk_oen	aiao_srst_req	aiao_cken	reserved	aiao_fsclk_div			aiao_bclk_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	aiao_bclkout_pctrl	BCLKOUT polarity 0: positive 1: negative
[12]	RW	aiao_bclkin_pctrl	BCLKIN polarity 0: positive 1: negative
[11]	RW	aiao_bclk_sel	BCLK/FCLK select 0: Clocks are internally generated. 1: Clocks are input from the external audio DAC.
[10]	RW	aiao_bclk_oen	BCLK/FCLK I/O OEN control 0: The BCLK/FCLK I/O is output. 1: The BCLK/FCLK I/O is input. Note: This field needs to work with aiao_bclk_sel to select the master/slave mode of the I^2S interface.
[9]	RW	aiao_srst_req	Soft reset request 0: deassert reset 1: reset
[8]	RW	aiao_cken	Clock status 0: disabled 1: enabled
[7]	RO	reserved	Reserved

[6:4]	RW	aiao_fsclk_div	Frequency division relationship between the bit clock BCLK and the sampling clock FS 000: The FS is obtained by dividing the BCLK by 16. 001: The FS is obtained by dividing the BCLK by 32. 010: The FS is obtained by dividing the BCLK by 48. 011: The FS is obtained by dividing the BCLK by 64. 100: The FS is obtained by dividing the BCLK by 128. 101: The FS is obtained by dividing the BCLK by 256. Other values: The FS is obtained by dividing the BCLK by 8.
[3:0]	RW	aiao_bclk_div	Frequency division relationship between the main clock MCLK and the bit clock BCLK 0000: The BCLK is obtained by dividing the MCLK by 1. 0001: The BCLK is obtained by dividing the MCLK by 3. 0010: The BCLK is obtained by dividing the MCLK by 2. 0011: The BCLK is obtained by dividing the MCLK by 4. 0100: The BCLK is obtained by dividing the MCLK by 6. 0101: The BCLK is obtained by dividing the MCLK by 8. 0110: The BCLK is obtained by dividing the MCLK by 12. 0111: The BCLK is obtained by dividing the MCLK by 16. 1000: The BCLK is obtained by dividing the MCLK by 24. 1001: The BCLK is obtained by dividing the MCLK by 32. 1010: The BCLK is obtained by dividing the MCLK by 48. 1011: The BCLK is obtained by dividing the MCLK by 64. Other values: The BCLK is obtained by dividing the MCLK by 8.

I2S_CRG_CFG0_01

I2S_CRG_CFG0_01 is I^{2}S01 CRG configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0108	I2S_CRG_CFG0_01	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								aiao_mclk_div																							
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved

[26:0]	RW	aiao_mclk_div	Clock divider of the MCLK. The configured value is calculated as follows: (Frequency of the target MCLK clock/Frequency of the MCLK PLL source clock) x 2^27. For details about the frequency of the MCLK PLL source clock, see section 3.2 "Clock" in chapter 3 "System."

I2S_CRG_CFG1_01

I2S_CRG_CFG1_01 is I^{2}S01 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x010C	I2S_CRG_CFG1_01	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		aiao_bclkout_pctrl	aiao_bclkin_pctrl	aiao_bclk_sel	aiao_bclk_oen	aiao_srst_req	aiao_cken	reserved	aiao_fsclk_div			aiao_bclk_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	aiao_bclkout_pctrl	BCLKOUT polarity 0: positive 1: negative
[12]	RW	aiao_bclkin_pctrl	BCLKIN polarity 0: positive 1: negative
[11]	RW	aiao_bclk_sel	BCLK/FCLK select 0: Clocks are internally generated. 1: Clocks are input from the external audio DAC.
[10]	RW	aiao_bclk_oen	BCLK/FCLK I/O OEN control 0: The BCLK/FCLK I/O is output. 1: The BCLK/FCLK I/O is input. Note: This field needs to work with aiao_bclk_sel to select the master/slave mode of the I^{2}S interface.

[9]	RW	aiao_srst_req	Soft reset request 0: deassert reset 1: reset
[8]	RW	aiao_cken	Clock status 0: disabled 1: enabled
[7]	RO	reserved	Reserved
[6:4]	RW	aiao_fsclk_div	Frequency division relationship between the bit clock BCLK and the sampling clock FS 000: The FS is obtained by dividing the BCLK by 16. 001: The FS is obtained by dividing the BCLK by 32. 010: The FS is obtained by dividing the BCLK by 48. 011: The FS is obtained by dividing the BCLK by 64. 100: The FS is obtained by dividing the BCLK by 128. 101: The FS is obtained by dividing the BCLK by 256. Other values: The FS is obtained by dividing the BCLK by 8.
[3:0]	RW	aiao_bclk_div	Frequency division relationship between the main clock MCLK and the bit clock BCLK 0000: The BCLK is obtained by dividing the MCLK by 1. 0001: The BCLK is obtained by dividing the MCLK by 3. 0010: The BCLK is obtained by dividing the MCLK by 2. 0011: The BCLK is obtained by dividing the MCLK by 4. 0100: The BCLK is obtained by dividing the MCLK by 6. 0101: The BCLK is obtained by dividing the MCLK by 8. 0110: The BCLK is obtained by dividing the MCLK by 12. 0111: The BCLK is obtained by dividing the MCLK by 16. 1000: The BCLK is obtained by dividing the MCLK by 24. 1001: The BCLK is obtained by dividing the MCLK by 32. 1010: The BCLK is obtained by dividing the MCLK by 48. 1011: The BCLK is obtained by dividing the MCLK by 64. Other values: The BCLK is obtained by dividing the MCLK by 8.

I2S_CRG_CFG0_08

I2S_CRG_CFG0_08 is I^2S08 CRG configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0140	I2S_CRG_CFG0_08	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				aiao_mclk_div																											
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RW	aiao_mclk_div	Clock divider of the MCLK. The configured value is calculated as follows: (Frequency of the target MCLK clock/Frequency of the MCLK PLL source clock) x 2^27. For details about the frequency of the MCLK PLL source clock, see section 3.2 "Clock" in chapter 3 "System."

I2S_CRG_CFG1_08

I2S_CRG_CFG1_08 is I^{2}S08 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0144	I2S_CRG_CFG1_08	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		aiao_bclkout_pctrl	aiao_bclkin_pctrl	aiao_bclk_sel	aiao_bclk_oen	aiao_srst_req	aiao_cken	reserved	aiao_fsclk_div			aiao_bclk_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	aiao_bclkout_pctrl	BCLKOUT polarity 0: positive 1: negative
[12]	RW	aiao_bclkin_pctrl	BCLKIN polarity 0: positive 1: negative
[11]	RW	aiao_bclk_sel	BCLK/FCLK select 0: Clocks are internally generated. 1: Clocks are input from the external audio DAC.

[10]	RW	aiao_bclk_oen	BCLK/FCLK I/O OEN control 0: The BCLK/FCLK I/O is output. 1: The BCLK/FCLK I/O is input. Note: This field needs to work with aiao_bclk_sel to select the master/slave mode of the I^2S interface.
[9]	RW	aiao_srst_req	Soft reset request 0: deassert reset 1: reset
[8]	RW	aiao_cken	Clock status 0: disabled 1: enabled
[7]	RO	reserved	Reserved
[6:4]	RW	aiao_fsclk_div	Frequency division relationship between the bit clock BCLK and the sampling clock FS 000: The FS is obtained by dividing the BCLK by 16. 001: The FS is obtained by dividing the BCLK by 32. 010: The FS is obtained by dividing the BCLK by 48. 011: The FS is obtained by dividing the BCLK by 64. 100: The FS is obtained by dividing the BCLK by 128. 101: The FS is obtained by dividing the BCLK by 256. Other values: The FS is obtained by dividing the BCLK by 8.
[3:0]	RW	aiao_bclk_div	Frequency division relationship between the main clock MCLK and the bit clock BCLK 0000: The BCLK is obtained by dividing the MCLK by 1. 0001: The BCLK is obtained by dividing the MCLK by 3. 0010: The BCLK is obtained by dividing the MCLK by 2. 0011: The BCLK is obtained by dividing the MCLK by 4. 0100: The BCLK is obtained by dividing the MCLK by 6. 0101: The BCLK is obtained by dividing the MCLK by 8. 0110: The BCLK is obtained by dividing the MCLK by 12. 0111: The BCLK is obtained by dividing the MCLK by 16. 1000: The BCLK is obtained by dividing the MCLK by 24. 1001: The BCLK is obtained by dividing the MCLK by 32. 1010: The BCLK is obtained by dividing the MCLK by 48. 1011: The BCLK is obtained by dividing the MCLK by 64. Other values: The BCLK is obtained by dividing the MCLK by 8.

I2S_CRG_CFG0_09

I2S_CRG_CFG0_09 is I^2S09 CRG configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0148	I2S_CRG_CFG0_09	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				aiao_mclk_div																											
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RW	aiao_mclk_div	Clock divider of the MCLK. The configured value is calculated as follows: (Frequency of the target MCLK clock/Frequency of the MCLK PLL source clock) x 2^27. For details about the frequency of the MCLK PLL source clock, see section 3.2 "Clock" in chapter 3 "System."

I2S_CRG_CFG1_09

I2S_CRG_CFG1_09 is I^{2}S09 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x014C	I2S_CRG_CFG1_09	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		aiao_bclkout_pctrl	aiao_bclkin_pctrl	aiao_bclk_sel	aiao_bclk_oen	aiao_srst_req	aiao_cken	reserved	aiao_fsclk_div			aiao_bclk_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	aiao_bclkout_pctrl	BCLKOUT polarity 0: positive 1: negative
[12]	RW	aiao_bclkin_pctrl	BCLKIN polarity 0: positive 1: negative

[11]	RW	aiao_bclk_sel	BCLK/FCLK select 0: Clocks are internally generated. 1: Clocks are input from the external audio DAC.
[10]	RW	aiao_bclk_oen	BCLK/FCLK I/O OEN control 0: The BCLK/FCLK I/O is output. 1: The BCLK/FCLK I/O is input. Note: This field needs to work with aiao_bclk_sel to select the master/slave mode of the I^2S interface.
[9]	RW	aiao_srst_req	Soft reset request 0: deassert reset 1: reset
[8]	RW	aiao_cken	Clock status 0: disabled 1: enabled
[7]	RO	reserved	Reserved
[6:4]	RW	aiao_fsclk_div	Frequency division relationship between the bit clock BCLK and the sampling clock FS 000: The FS is obtained by dividing the BCLK by 16. 001: The FS is obtained by dividing the BCLK by 32. 010: The FS is obtained by dividing the BCLK by 48. 011: The FS is obtained by dividing the BCLK by 64. 100: The FS is obtained by dividing the BCLK by 128. 101: The FS is obtained by dividing the BCLK by 256. Other values: The FS is obtained by dividing the BCLK by 8.
[3:0]	RW	aiao_bclk_div	Frequency division relationship between the main clock MCLK and the bit clock BCLK 0000: The BCLK is obtained by dividing the MCLK by 1. 0001: The BCLK is obtained by dividing the MCLK by 3. 0010: The BCLK is obtained by dividing the MCLK by 2. 0011: The BCLK is obtained by dividing the MCLK by 4. 0100: The BCLK is obtained by dividing the MCLK by 6. 0101: The BCLK is obtained by dividing the MCLK by 8. 0110: The BCLK is obtained by dividing the MCLK by 12. 0111: The BCLK is obtained by dividing the MCLK by 16. 1000: The BCLK is obtained by dividing the MCLK by 24. 1001: The BCLK is obtained by dividing the MCLK by 32. 1010: The BCLK is obtained by dividing the MCLK by 48. 1011: The BCLK is obtained by dividing the MCLK by 64. Other values: The BCLK is obtained by dividing the MCLK by 8.

RX_IF_ATTRI

RX_IF_ATTRI is an interface attribute configuration register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1000 + 0x100 x *n* (*n* = 0–1)	RX_IF_ATTRI	0xE400_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						rx_sd0_sel		rx_sd_source_sel				reserved	rx_trackmode			rx_sd_offset								rx_multislot_en	reserved		rx_ch_num	rx_i2s_precision		rx_mode	
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:24]	RW	rx_sd0_sel	SD0 select. This field must be fixed at 0.
[23:20]	RW	rx_sd_source_sel	Input interface source select for the RX channel 0x0: I^2S TX0 0x1: I^2S TX1 0x8: I^2S RX0 0x9: I^2S RX1 Other values: reserved Note: If TX0 or TX1 is selected as the input interface source, the TX0 or TX1 data can be looped back.
[19]	RO	reserved	Reserved
[18:16]	RW	rx_trackmode	Audio-left and audio-right channel mode in I^2S mode 000: The sound is not processed. 001: The sounds in two channels are audio-left channel sounds. 010: The sounds in two channels are audio-right channel sounds. 011: The sounds in two channels are exchanged. 100: The sounds of two channels are added and then output. 101: The audio-left channel is muted, and the sound of the audio-right channel is from the original audio-right channel. 110: The audio-right channel is muted, and the sound of the audio-left channel is from the original audio-left channel. 111: The audio-left and audio-right channels are muted. Note: trackmode is still valid in 1-channel RX mode.

[15:8]	RW	rx_sd_offset	Number of BCLK clocks delayed for data relative to the frame sync signal in PCM mode 0x00: 0 bit clocks 0x01: 1 bit clock 0x02: 2 bit clocks … 0xFE: 254 bit clocks 0xFF: 255 bit clocks
[7]	RW	rx_multislot_en	Time-division multiplexing validity indicator 0: invalid (normal mode) 1: valid
[6]	RO	reserved	Reserved
[5:4]	RW	rx_ch_num	Number of RX channels rx_multislot_en = 0 00: 1-channel RX (SD0 data line) 01: 2-channel RX (PCM does not support this mode) Other values: reserved rx_multislot_en = 1 Number of RX channels in time-division multiplexing mode. 00: 2-channel RX 01: 4-channel RX 10: 8-channel RX 11: 16-channel RX
[3:2]	RW	rx_i2s_precision	Data sampling precision rx_multislot_en = 0 I^2S non-TDM mode mode: 00: reserved 01: 16 bits 10: 24 bits 11: reserved PCM non-TDM mode mode: 00: 8 bits 01: 16 bits Other values: reserved rx_multislot_en = 1 I^2S/PCM mode: 00: 8 bits 01: 16 bits Other values: reserved

[1:0]	RW	rx_mode	Interface mode of the RX channel 00: I^2S mode 01: PCM mode Other values: reserved

RX_DSP_CTRL

RX_DSP_CTRL is an RX channel control register.

Offset Address	Register Name	Total Reset Value
0x1004 + 0x100 x *n* (*n* = 0−1)	RX_DSP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		disable_done	rx_enable	bypass_en	reserved																										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	disable_done	RX channel stop/complete indicator 0: The RX channel stops but the operation is not complete. 1: The RX channel stops and the operation is complete.
[28]	RW	rx_enable	RX channel start/stop control 0: stop 1: start
[27]	RW	bypass_en	Operation bypass enable (the control function still takes effect) 0: disabled 1: enabled (trackmode is bypassed)
[26:0]	RO	reserved	Reserved

RX_BUFF_SADDR

RX_BUFF_SADDR is a DDR buffer start address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1080 + 0x100 x *n* (*n* = 0–1)	RX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rx_buff_saddr	Start address for the DDR buffer of RX channel 0. Its unit is byte. Note: The start address must be 128x2-bit-aligned.

RX_BUFF_SIZE

RX_BUFF_SIZE is a DDR buffer size register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1084 + 0x100 x *n* (*n* = 0–1)	RX_BUFF_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_size	DDR buffer size of the RX channel. Its unit is byte. Note: The buffer size must be an integral multiple of 32 bytes.

RX_BUFF_WPTR

RX_BUFF_WPTR is a DDR buffer write address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1088 + 0x100 x *n* (*n* = 0–1)	RX_BUFF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_wptr																							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_wptr	Write address for the DDR buffer of the RX channel. Its unit is byte. Note: • The write address in the RX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The write address must be 128x2-bit-aligned.

RX_BUFF_RPTR

RX_BUFF_RPTR is a DDR buffer read address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x108C + 0x100 x *n* (*n* = 0−1)	RX_BUFF_RPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_rptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_rptr	Read address for the DDR buffer of the RX channel. Its unit is byte. Note: • The read address in the RX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The software operation is performed by byte, and the hardware operation is performed by 32 bytes.

RX_BUFF_ALFULL_TH

RX_BUFF_ALFULL_TH is a DDR buffer almost full threshold register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1090 + 0x100 x *n* (*n* = 0–1)	RX_BUFF_ALFULL_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_alfull_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_alfull_th	Almost full threshold for the DDR buffer of the RX channel. Its unit is byte. If the available space of the DDR buffer is below the almost full threshold, the almost full raw interrupt is generated. Note: If the rx_alfull_int interrupt is used, the field value must be an integral multiple of 16 bytes and greater than or equal to 0x40.

RX_TRANS_SIZE

RX_TRANS_SIZE is data transfer length register for the RX interrupt.

Offset Address	Register Name	Total Reset Value
0x1094 + 0x100 x *n* (*n* = 0–1)	RX_TRANS_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_trans_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_trans_size	After the RX channel receives the audio data with the length of rx_trans_size (in byte), a transfer completion interrupt is generated.

RX_WPTR_TMP

RX_WPTR_TMP is a write address storage register for the RX channel upon reporting of the transfer completion interrupt.

Offset Address	Register Name	Total Reset Value
0x1098 + 0x100 x *n* (*n* = 0–1)	RX_WPTR_TMP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_wptr_tmp																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RO	rx_wptr_tmp	This field is used to save the write address for the RX channel when the transfer completion interrupt is reported.

RX_INT_ENA

RX_INT_ENA is an interrupt enable register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A0 + 0x100 x *n* (*n* = 0–1)	RX_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_fifo_lost_int_ena	reserved	rx_stop_int_ena	rx_ififo_full_int_ena	rx_bfifo_full_int_ena	rx_alfull_int_ena	rx_full_int_ena	rx_trans_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	rx_fifo_lost_int_ena	Frame loss interrupt enable for the RX channel 0: disabled 1: enabled
[6]	RO	reserved	Reserved
[5]	RW	rx_stop_int_ena	Stop interrupt enable for the RX channel 0: disabled 1: enabled

[4]	RW	rx_ififo_full_int_ena	Interface FIFO overflow interrupt enable for the RX channel 0: disabled 1: enabled
[3]	RW	rx_bfifo_full_int_ena	Bus FIFO overflow interrupt enable for the RX channel 0: disabled 1: enabled
[2]	RW	rx_alfull_int_ena	DDR buffer almost full interrupt enable for the RX channel 0: disabled 1: enabled
[1]	RW	rx_full_int_ena	DDR buffer full interrupt for the RX channel 0: disabled 1: enabled
[0]	RW	rx_trans_int_ena	Transfer completion interrupt enable for the RX channel 0: disabled 1: enabled

RX_INT_RAW

RX_INT_RAW is a raw interrupt register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A4 + 0x100 x *n* (*n* = 0–1)	RX_INT_RAW	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved						rx_fifo_lost_int_raw	reserved	rx_stop_int_raw	reserved	rx_fifo_full_int_raw	rx_alfull_int_raw	rx_full_int_raw	rx_trans_int_raw
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	rx_fifo_lost_int_raw	Data full lost raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RO	reserved	Reserved

[5]	RO	rx_stop_int_raw	Stop raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RO	reserved	Reserved
[3]	RO	rx_fifo_full_int_raw	Bus FIFO overflow raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RO	rx_alfull_int_raw	DDR buffer almost full raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	rx_full_int_raw	DDR buffer full raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	rx_trans_int_raw	Transfer completion raw interrupt of the RX interrupt 0: No raw interrupt is generated. 1: A raw interrupt is generated.

RX_INT_STATUS

RX_INT_STATUS is an interrupt status register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A8 + 0x100 x *n* (*n* = 0–1)	RX_INT_STATUS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved						rx_ffifo_lost_int_status	reserved	rx_stop_int_status	reserved	rx_bfifo_full_int_status	rx_alfull_int_status	rx_full_int_status	rx_trans_int_status
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	rx_fifo_lost_int_status	Status of the data full loss interrupt of the RX channel 0: No interrupt is generated. 1: An interrupt is generated.

[6]	RO	reserved	Reserved
[5]	RO	rx_stop_int_status	Status of the stop interrupt of the RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	reserved	Reserved
[3]	RO	rx_bfifo_full_int_status	Status of the bus FIFO overflow interrupt of the RX channel 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_alfull_int_status	Status of the DDR buffer almost full interrupt of the RX channel 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	rx_full_int_status	Status of the DDR buffer full interrupt of the RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_trans_int_status	Status of the transfer completion interrupt of the RX channel 0: No interrupt is generated. 1: An interrupt is generated.

RX_INT_CLR

RX_INT_CLR is an interrupt clear register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10AC + 0x100 x *n* (*n* = 0–1)	RX_INT_CLR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved						rx_fifo_lost_int_clear	reserved	rx_stop_int_clear	rx_ififo_full_int_clear	rx_bfifo_full_int_clear	rx_alfull_int_clear	rx_full_int_clear	rx_trans_int_clear
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved

[7]	WC	rx_fifo_lost_int_clear	Data full loss interrupt clear for the RX channel 0: not cleared 1: cleared
[6]	RO	reserved	Reserved
[5]	WC	rx_stop_int_clear	Stop interrupt clear for the RX channel 0: not cleared 1: cleared
[4]	WC	rx_ififo_full_int_clear	Interface FIFO overflow interrupt clear for the RX channel 0: not cleared 1: cleared
[3]	WC	rx_bfifo_full_int_clear	Bus FIFO overflow interrupt clear for the RX channel 0: not cleared 1: cleared
[2]	WC	rx_alfull_int_clear	DDR buffer almost full interrupt clear for the RX channel 0: not cleared 1: cleared
[1]	WC	rx_full_int_clear	DDR buffer full interrupt clear for the RX channel 0: not cleared 1: cleared
[0]	WO	rx_trans_int_clear	Transfer completion interrupt clear for the RX interrupt 0: not cleared 1: cleared

TX_IF_ATTRI

TX_IF_ATTRI is an interface attribute configuration register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2000 + 0x100 x *m* (*m* = 0−1)	TX_IF_ATTRI	0xE400_0004

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	reserved	tx_sd0_sel	tx_sd_source_sel	reserved	tx_trackmode	tx_sd_offset	reserved	tx_ch_num	tx_i2s_precision	tx_mode

Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:24]	RW	tx_sd0_sel	SD0 select. This field must be fixed at 0. Note: Select the channel and data line in sequence.
[23:20]	RW	tx_sd_source_sel	Source select for SD0, SD1, SD2, and SD3 0000: I^2S TX0 0001: I^2S TX1 1000: I^2S RX0 1001: I^2S RX1 Other values: reserved
[19]	RO	reserved	Reserved
[18:16]	RW	tx_trackmode	Audio-left and audio-right channel mode in I^2S mode 000: The sound is not processed. 001: The sounds in two channels are audio-left channel sounds. 010: The sounds in two channels are audio-right channel sounds. 011: The sounds in two channels are exchanged. 100: The sounds of two channels are added and then output. 101: The audio-left channel is muted, and the sound of the audio-right channel is from the original audio-right channel. 110: The audio-right channel is muted, and the sound of the audio-left channel is from the original audio-left channel. 111: The audio-left and audio-right channels are muted. Note: trackmode is still valid in 1-channel TX mode.
[15:8]	RW	tx_sd_offset	Number of BCLK clocks delayed for data relative to the frame sync signal in PCM mode 0x00: 0 bit clocks 0x01: 1 bit clock 0x02: 2 bit clocks … 0xFE: 254 bit clocks 0xFF: 255 bit clocks
[7:6]	RO	reserved	Reserved

[5:4]	RW	tx_ch_num	Number of TX channels tx_multislot_en = 0 00: 1-channel TX 01: 2-channel TX Other values: reserved tx_multislot_en = 1 Number of TX channels in time-division multiplexing mode 00: 2-channel TX 01: 4-channel TX 10: 8-channel TX 11: 16-channel TX Note: • The data line must be SD0 for multi-channel TX. • The time-division multiplexing mode is not supported during transmission.
[3:2]	RW	tx_i2s_precision	Data sampling precision I^2S normal mode: 00: reserved 01: 16 bits 10: 24 bits 11: reserved PCM normal mode: 00: 8 bits 01: 16 bits Other values: reserved
[1:0]	RW	tx_mode	Interface mode of the TX channel 00: I^2S mode 01: PCM mode Other values: reserved

TX_DSP_CTRL

TX_DSP_CTRL is a TX channel control register.

Offset Address	Register Name	Total Reset Value
0x2004 + 0x100 x *m* (*m* = 0–1)	TX_DSP_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		tx_disable_done	tx_enable	bypass_en	reserved			fade_out_rate				fade_in_rate				reserved	volume							reserved						mute_fade_en	mute_en
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RO	tx_disable_done	TX channel stop/complete identifier 0: not complete 1: complete
[28]	RW	tx_enable	TX channel start/stop control 0: stop 1: start
[27]	RW	bypass_en	Operation bypass enable (the control function still takes effect) 0: disabled 1: enabled (the functions such as volume control, trackmode, and fade-in/fade-out are bypassed)
[26:24]	RO	reserved	Reserved
[23:20]	RW	fade_out_rate	Fade-out rate register 0x0: The fade-out rate changes every one sampling point. 0x1: The fade-out rate changes every two sampling points. 0x2: The fade-out rate changes every four sampling points. 0x3: The fade-out rate changes every eight sampling points. 0x4: The fade-out rate changes every 16 sampling points. 0x5: The fade-out rate changes every 32 sampling points. 0x6: The fade-out rate changes every 64 sampling points. 0x7: The fade-out rate changes every 128 sampling points. Other values: reserved

[19:16]	RW	fade_in_rate	Fade-in rate register. 0x0: The fade-in rate changes every one sampling point. 0x1: The fade-in rate changes every two sampling points. 0x2: The fade-in rate changes every four sampling points. 0x3: The fade-in rate changes every eight sampling points. 0x4: The fade-in rate changes every 16 sampling points. 0x5: The fade-in rate changes every 32 sampling points. 0x6: The fade-in rate changes every 64 sampling points. 0x7: The fade-in rate changes every 128 sampling points. Other values: reserved
[15]	RO	reserved	Reserved
[14:8]	RW	volume	Volume 0x00−0x28: mute 0x29: −80 dB … 0x7E: +5 dB 0x7F: +6 dB
[7:2]	RW	reserved	Reserved.
[1]	RW	mute_fade_en	Mute fade-in/fade-out control 0: disabled 1: enabled
[0]	RW	mute_en	Mute control 0: unmuted 1: muted

TX_DMAR_STATUS

TX_DMAR_STATUS is a TX DMAW status register.

Offset Address	Register Name	Total Reset Value
0x2010 + 0x100 x *m* (*m* = 0−1)	TX_DMAR_STATUS	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				tx_fifo_raddr				reserved				tx_fifo_waddr				reserved	tx_fifo_full	state_clr_end	trans_finish_ind	vcmdready	vtrans	tx_buf_empty	tx_fifo_afull	reserved							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RO	tx_buf_empty	Buffer empty status 0: not empty 1: empty
[8:0]	RO	reserved	Reserved

TX_WS_CNT

TX_WS_CNT is a WS cyclic count status register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2020 + 0x100 x *m* (*m* = 0–1)	TX_WS_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ws_count																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RO	ws_count	FSCLK cyclic count register The unit is FSCLK.

TX_BCLK_CNT

TX_BCLK_CNT is a BCLK cyclic count status register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2024 + 0x100 x *m* (*m* = 0–1)	TX_BCLK_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bclk_count																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:0]	RO	bclk_count	BCLK cyclic count register The unit is BCLK.

TX_BUFF_SADDR

TX_BUFF_SADDR is a DDR buffer start address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2080 + 0x100 x *m* (*m* = 0–1)	TX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_buff_saddr	Start address for the DDR buffer of the TX channel. Its unit is byte. Note: The start address must be 128x2-bit-aligned.

TX_BUFF_SIZE

TX_BUFF_SIZE is a DDR buffer size register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2084 + 0x100 x *m* (*m* = 0–1)	TX_BUFF_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_size	DDR buffer size of the TX channel. Its unit is byte. Note: The buffer size must be an integral multiple of 32 bytes.

TX_BUFF_WPTR

TX_BUFF_WPTR is a DDR buffer write address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2088 + 0x100 x *m* (*m* = 0–1)	TX_BUFF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_wptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_wptr	Write address for the DDR buffer of the TX channel Note: • The write address in the TX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The available space of the TX buffer must be greater than or equal to 32 bytes. • The software operation is performed by byte, and the hardware operation is performed by 32 bytes.

TX_BUFF_RPTR

TX_BUFF_RPTR is a DDR buffer read address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x208C + 0x100 x *m* (*m* = 0–1)	TX_BUFF_RPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_rptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_rptr	Read address for the DDR buffer of the TX channel Note: • The read address in the TX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The address must be 128x2-bit-aligned.

TX_BUFF_ALEMPTY_TH

TX_BUFF_ALEMPTY_TH is a DDR buffer almost empty threshold register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2090 + 0x100 x *m* (*m* = 0–1)	TX_BUFF_ALEMPTY_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_alempty_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_alempty_th	Almost empty threshold for the DDR buffer of the TX channel. Its unit is byte. If the available space of the DDR buffer is below the almost empty threshold, the almost empty raw interrupt is generated. Note: If the tx_alempty_int interrupt is used, the field value must be an integral multiple of 16 bytes and greater than or equal to 0x20.

TX_TRANS_SIZE

TX_TRANS_SIZE is a data transfer length register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2094 + 0x100 x *m* (*m* = 0–1)	TX_TRANS_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_trans_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_trans_size	After the TX channel transmits the audio data with the length of tx_trans_size (in byte), a transfer completion interrupt is generated.

TX_RPTR_TMP

TX_RPTR_TMP is a read address storage register for the TX channel upon reporting of the transfer completion interrupt.

Offset Address	Register Name	Total Reset Value
0x2098 + 0x100 x *m* (*m* = 0–1)	TX_RPTR_TMP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_rptr_tmp																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RO	tx_rptr_tmp	This field is used to save the read address for the TX channel when the transfer completion interrupt is reported.

TX_INT_ENA

TX_INT_ENA is an interrupt enable register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A0 + 0x100 x *m* (*m* = 0–1)	TX_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_ena	tx_mfade_int_ena	tx_stop_int_ena	tx_ififo_empty_int_ena	tx_bfifo_empty_int_ena	tx_alempty_int_ena	tx_empty_int_ena	tx_trans_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	tx_dat_break_int_ena	Interface data break interrupt enable for the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[6]	RW	tx_mfade_int_ena	Mute fade-in/fade-output completion interrupt enable for the TX channel 0: disabled 1: enabled
[5]	RW	tx_stop_int_ena	Stop interrupt enable for the TX channel 0: disabled 1: enabled
[4]	RW	tx_ififo_empty_int_ena	Interface FIFO underflow interrupt enable for the TX channel 0: disabled 1: enabled
[3]	RW	tx_bfifo_empty_int_ena	Bus FIFO underflow interrupt enable for the TX channel 0: disabled 1: enabled
[2]	RW	tx_alempty_int_ena	DDR buffer almost empty interrupt enable for the TX channel 0: disabled 1: enabled
[1]	RW	tx_empty_int_ena	DDR buffer empty interrupt for the TX channel 0: disabled 1: enabled
[0]	RW	tx_trans_int_ena	Transfer completion interrupt enable for the TX channel 0: disabled 1: enabled

TX_INT_RAW

TX_INT_RAW is a raw interrupt register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A4 + 0x100 x *m* (*m* = 0−1)	TX_INT_RAW	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved						tx_dat_break_int_raw	tx_mfade_int_raw	tx_stop_int_raw	tx_ififo_empty_int_raw	tx_bfifo_empty_int_raw	tx_alempty_int_raw	tx_empty_int_raw	tx_trans_int_raw

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_dat_break_int_raw	Interface data break raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RO	tx_mfade_int_raw	Mute fade-in/fade-output completion raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	RO	tx_stop_int_raw	Stop raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RO	tx_ififo_empty_int_raw	Interface FIFO underflow raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	RO	tx_bfifo_empty_int_raw	Bus FIFO underflow raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RO	tx_alempty_int_raw	DDR buffer almost empty raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	tx_empty_int_raw	DDR buffer empty raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	tx_trans_int_raw	Transfer completion raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.

TX_INT_STATUS

TX_INT_STATUS is an interrupt status register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A8 + 0x100 x *m* (*m* = 0−1)	TX_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_status	tx_mfade_int_status	tx_stop_int_status	tx_ififo_empty_int_status	tx_bfifo_empty_int_status	tx_alempty_int_status	tx_empty_int_status	tx_trans_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_dat_break_int_status	Status of the interface data break interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	tx_mfade_int_status	Status of the mute fade-in/fade-output completion interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	tx_stop_int_status	Status of the stop interrupt of the TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	tx_ififo_empty_int_status	Status of the interface FIFO underflow interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	tx_bfifo_empty_int_status	Status of the bus FIFO underflow interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	tx_alempty_int_status	DDR buffer almost empty interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	tx_empty_int_status	Status of the DDR buffer empty interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.

[0]	RO	tx_trans_int_status	Status of the transfer completion interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.

TX_INT_CLR

TX_INT_CLR is an interrupt clear register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20AC + 0x100 x *m* (*m* = 0−1)	TX_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_clear	tx_mfade_int_clear	tx_stop_int_clear	tx_ififo_empty_int_clear	tx_bfifo_empty_int_clear	tx_alempty_int_clear	tx_empty_int_clear	tx_trans_int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	WC	tx_dat_break_int_clear	Interface data break interrupt clear for the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	WC	tx_mfade_int_clear	Mute fade-in/fade-output completion interrupt clear for the TX channel 0: not cleared 1: cleared
[5]	WC	tx_stop_int_clear	Stop interrupt clear for the TX channel 0: not cleared 1: cleared
[4]	WC	tx_ififo_empty_int_clear	Interface FIFO underflow interrupt clear for the TX channel 0: not cleared 1: cleared
[3]	WC	tx_bfifo_empty_int_clear	Bus FIFO underflow interrupt clear for the TX channel 0: not cleared 1: cleared

[2]	WC	tx_alempty_int_clear	DDR buffer almost empty interrupt clear for the TX channel 0: not cleared 1: cleared
[1]	WC	tx_empty_int_clear	DDR buffer empty interrupt clear for the RX channel 0: not cleared 1: cleared
[0]	WC	tx_trans_int_clear	Transfer completion interrupt clear for the TX channel 0: not cleared 1: cleared

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13.1 I²C Controller

13.1.1 Overview

The inter-integrated circuit (I^2C) module is used to read or write to the slave device connected on the I^2C bus through the CPU. When writing data to and reading data from the slave device, the CPU configures the I^2C configuration register over the bus and transmits the control information and the data to be used to the I^2C data communication register. After parsing the commands, the I^2C module transmits the data of the data channel register to the slave device over I^2C bus and notifies the CPU of the final status to the CPU by using interrupts after transmitting the data. The CPU reads data from the slave device in the similar way.

13.1.2 Function Description

The I^2C module has the following features:

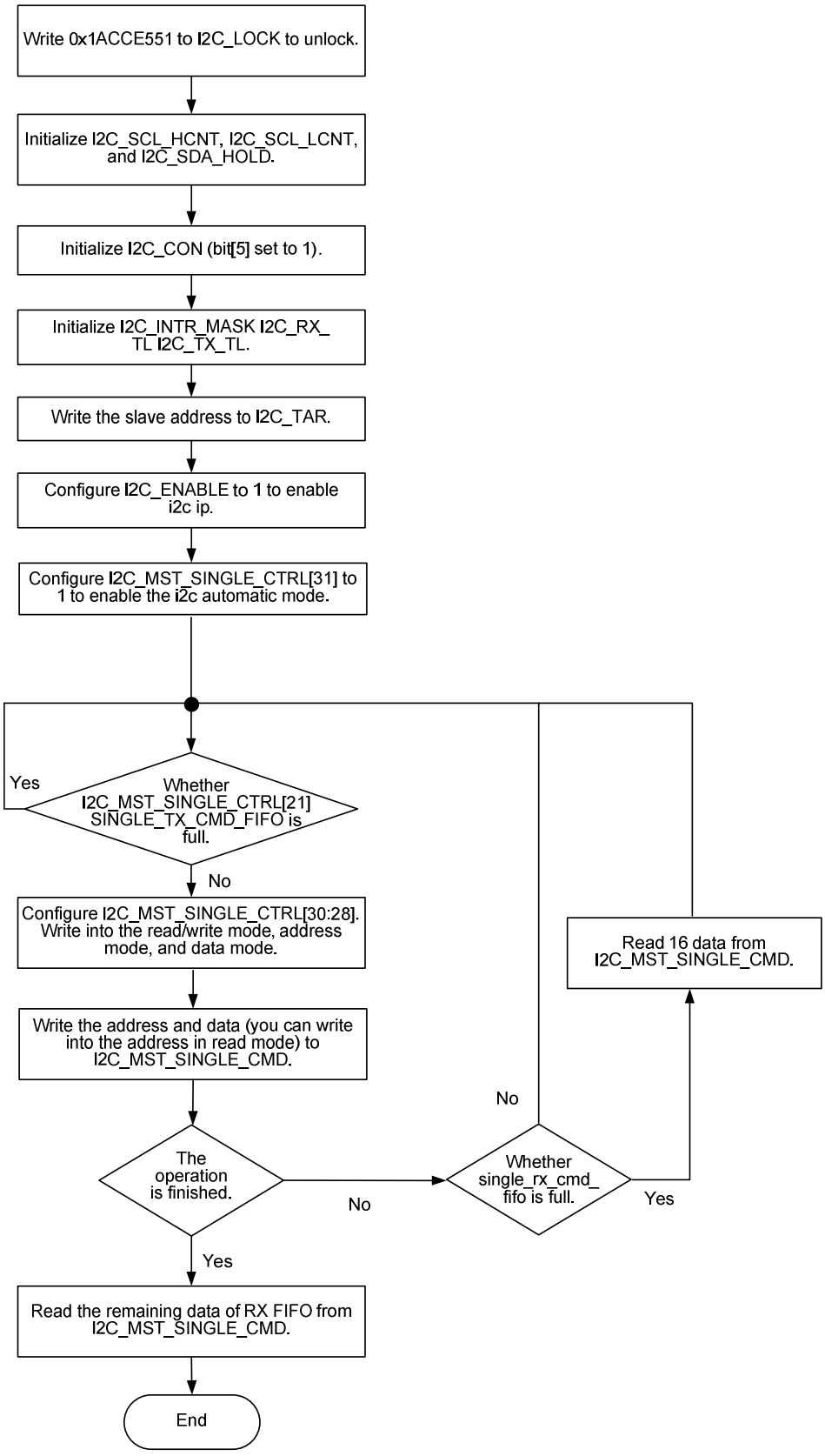
- The Hi3521A provides the master I^2C interface.
- Supports the bus arbitration in the case of multiple master devices.
- Supports clock synchronization and bit and byte waiting.
- Supports 7-bit standard address and 10-bit extended address.
- Supports standard mode (100 kbit/s) and high-speed mode (400 kbit/s).
- Supports general call and start byte.
- CBUS components are not supported.
- Supports the DMA operation.

13.1.3 Operating Mode

Process of Receiving and Transmitting Data by a Single Operation through the I²C Master

Figure 13-1 shows the process of receiving data by a single operation through the I^2C master.

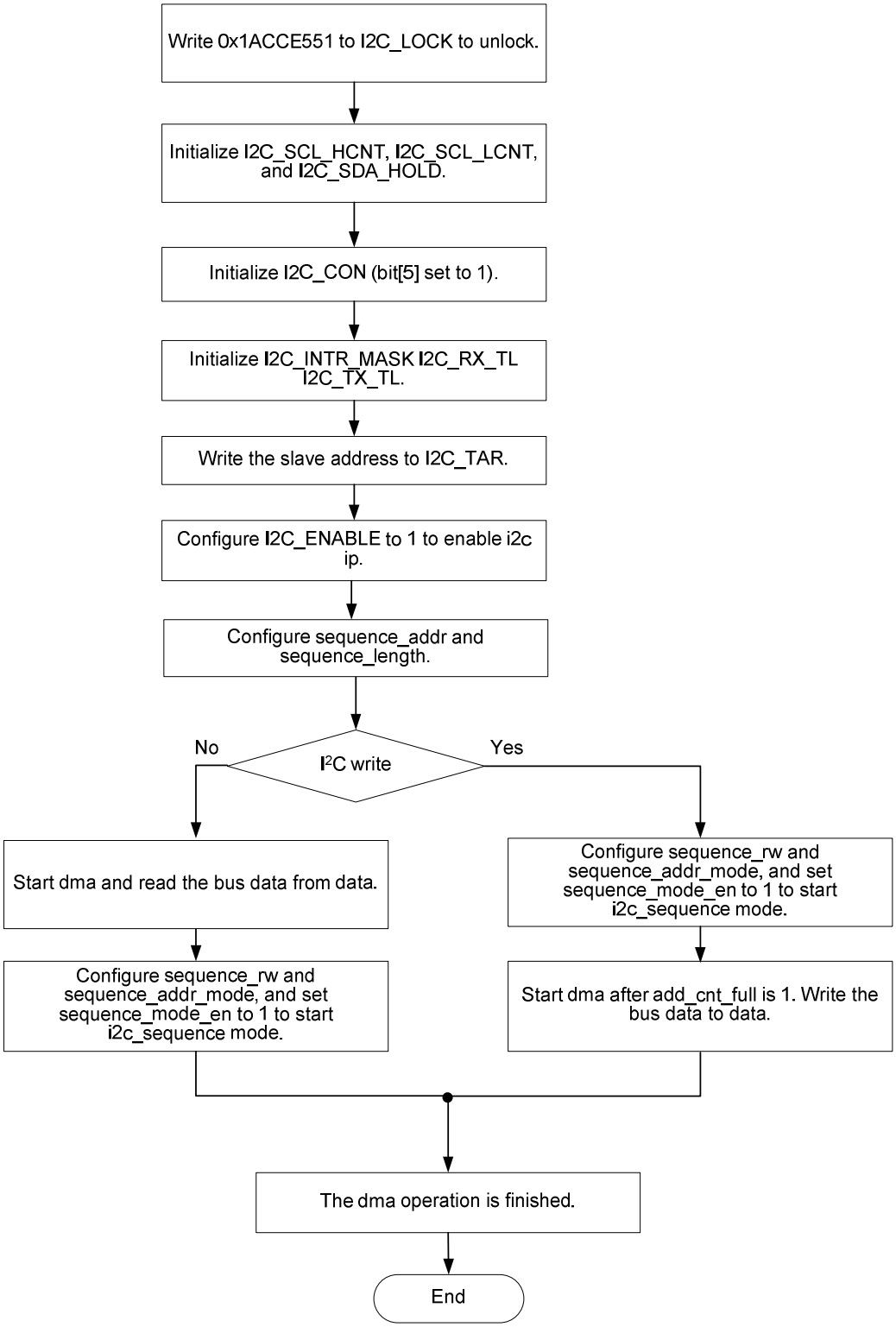
Figure 13-1 Process of receiving data by a single operation through the I²C master



Process of Continuously Receiving and Transmitting Data by the I²C Master

Figure 13-2 shows process of continuously receiving and transmitting data by the I²C master.

Figure 13-2 Process of continuously receiving and transmitting data by the I²C master



13.1.4 Register Summary

The Hi3521A contains three I²C modules and Table 13-1 describes I²C registers.

Table 13-1 Summary of I²C registers (base addresses 0x120C_0000.)

Offset Address	Register	Description	Page
0x000	I2C_CON	I²C control register	13-5
0x004	I2C_TAR	I²C access slave device address register	13-6
0x010	I2C_DATA_CMD	I²C data operation register	13-6
0x01C	I2C_SCL_HCNT	I2C_SCL high level configuration register	13-7
0x020	I2C_SCL_LCNT	I2C_SCL low level configuration register	13-7
0x02C	I2C_INTR_STAT	I²C masked interrupt status register	13-8
0x030	I2C_INTR_MASK	I²C interrupt mask register	13-9
0x034	I2C_INTR_RAW	I²C raw interrupt status register	13-11
0x038	I2C_RX_TL	RX_FIFO threshold configuration register	13-13
0x03C	I2C_TX_TL	TX_FIFO threshold configuration register	13-13
0x040	I2C_CLR_INTR	I²C interrupt clear register	13-13
0x06C	I2C_ENABLE	I²C enable register	13-14
0x070	I2C_STATUS	I²C status register	13-14
0x074	I2C_TXFLR	TX_FIFO valid data indicator register	13-16
0x078	I2C_RXFLR	RX_FIFO valid data indicator register	13-16
0x07C	I2C_SDA_HOLD	SDA hold time register	13-17
0x080	I2C_TX_ABRT_SRC	I²C TX failure interrupt source register	13-17
0x088	I2C_DMA_CR	I²C DMA interface control register	13-19
0x08C	I2C_DMA_TDLR	TX_FIFO DMA operation threshold register	13-19
0x090	I2C_DMA_RDLR	RX_FIFO DMA operation threshold register	13-20
0x0A0	I2C_SCL_SWITCH	I²C anti-suspend enable register	13-20
0x0A4	I2C_SCL_SIM	I²C anti-suspend analog register	13-21
0x0AC	I2C_LOCK	I²C lock register	13-22

Offset Address	Register	Description	Page
0x0B0	I2C_MST_SINGLE_CTRL	I2C_MST_SINGLE_CTRL register	13-22
0x0B4	I2C_MST_SINGLE_CMD	I2C_MST_SINGLE_CMD register	13-24
0x0B8	I2C_SEQUENCE_CMD0	I2C_SEQUENCE_CMD0 register	13-24
0x0BC	I2C_SEQUENCE_CMD1	I2C_SEQUENCE_CMD1 register	13-26
0x0C0	I2C_SEQUENCE_CMD2	I2C_SEQUENCE_CMD2 register	13-26

13.1.5 Register Description

I2C_CON

I2C_CON is an I^2C control register.

Offset Address	Register Name	Total Reset Value
0x000	I2C_CON	0x0000_0065

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3 2 1	0
Name	reserved							reserved	restart_en	reserved	reserved	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	1	1	0	0 1 0	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RO	reserved	Reserved
[5]	RW	restart_en	Restart command TX enable in master mode 0: disabled 1: enabled **NOTE** If the Restart function is disabled, the following functions are not supported: 1. Sending the start bit 2. High-speed mode 3. Read operation in 10-bit addressing mode 4. Combined addressing mode
[4]	RO	reserved	Reserved
[3]	RO	reserved	Reserved
[2:1]	RO	reserved	Reserved

[0]	RO	reserved	Reserved

I2C_TAR

I2C_TAR is an I²C access slave device address register.

Offset Address	Register Name	Total Reset Value
0x004	I2C_TAR	0x0000_002C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				master_10bit	special	gc_or_start	i2c_tar								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	master_10bit	Address length in master mode 0: 7 bits 1: 10 bits
[11]	RW	special	General call or start byte function enable 0: disabled 1: enabled
[10]	RW	gc_or_start	I²C command to be executed when the Special bit is 1 0: general call command (After the general call command is sent, you can perform only write operations. If you perform read operations, tx_abort interrupt is triggered. For details about the definition.) 1: start byte command
[9:0]	RW	i2c_tar	Slave address that is accessed by the I²C when I²C acts as a master device **NOTE** If the address length of the slave device is set to 7 bits, only bit [6:0] are valid.

I2C_DATA_CMD

I2C_DATA_CMD is an I²C data operation register.

Offset Address	Register Name	Total Reset Value
0x010	I2C_DATA_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							reserved	data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	reserved	Reserved
[7:0]	RW	data	Data to be transmitted or received through the I^2C bus Read: The data received from the I^2C bus is read. Write: The written data is transmitted to the I^2C.

I2C_SCL_HCNT

I2C_SCL_HCNT is an I2C_SCL high level configuration register.

Offset Address	Register Name	Total Reset Value
0x01C	I2C_SCL_HCNT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																i2c_scl_hcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	i2c_scl_hcnt	Number of SCL clock high-level cycles **NOTE** 1. The field must be configured to obtain the appropriate I/O timing before data is transmitted through the I2C bus. 2. You can perform write operations only when the I2C interface is disabled (I2C_ENABLE = 0).

I2C_SCL_LCNT

I2C_SCL_LCNT is an I2C_SCL low level configuration register.

Offset Address	Register Name	Total Reset Value
0x020	I2C_SCL_LCNT	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																i2c_scl_lcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	i2c_scl_lcnt	Number of SCL clock low-level cycles **NOTE** 1. The field must be correctly configured to obtain the appropriate I/O timing before data is transmitted through the I^2C bus. 2. You can perform write operations only when the I^2C interface is disabled (I2C_ENABLE = 0).

I2C_INTR_STAT

I2C_INTR_STAT is an interrupt status register after the I^2C is masked.

Offset Address	Register Name	Total Reset Value
0x02C	I2C_INTR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call	start_det	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RO	gen_call	Status of the interrupt indicating that a general call request is received 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	start_det	Status of the start detect interrupt indicating the I^2C bus interface has the START or RESTART condition 0: No interrupt is generated. 1: An interrupt is generated.

[9]	RO	stop_det	Status of the start detect interrupt indicating the I^{2}C bus interface has the STOP condition 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	activity	Activity interrupt status. The I^{2}C activity status is recorded until the interrupt is cleared. 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	reserved	Reserved
[6]	RO	tx_abrt	TX abort interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	reserved	Reserved
[4]	RO	tx_empty	Status of the interrupt indicating that TX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	tx_over	TX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_full	Status of the interrupt indicating that RX_FIFO reaches or is above the threshold 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	rx_over	RX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_under	Read data overflow (that is, the CPU reads the FIFO when RX_FIFO is empty) interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

I2C_INTR_MASK

I2C_INTR_MASK is an I^{2}C interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x030	I2C_INTR_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call_mask	start_det_mask	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	gen_call_mask	Interrupt mask when a general call request is received 0: not masked 1: masked
[10]	RW	start_det_mask	Start detect interrupt mask 0: not masked 1: masked
[9]	RW	stop_det	Stop detect interrupt mask 0: not masked 1: masked
[8]	RW	activity	Activity interrupt mask 0: not masked 1: masked
[7]	RO	reserved	Reserved
[6]	RW	tx_abrt	TX abort interrupt mask 0: not masked 1: masked
[5]	RO	reserved	Reserved
[4]	RW	tx_empty	Interrupt mask when TX_FIFO reaches or is below the threshold 0: not masked 1: masked
[3]	RW	tx_over	TX_FIFO overflow interrupt mask 0: not masked 1: masked
[2]	RW	rx_full	Interrupt mask when RX_FIFO reaches or is below the threshold 0: not masked 1: masked

[1]	RW	rx_over	RX_FIFO overflow interrupt mask 0: not masked 1: masked
[0]	RW	rx_under	Interrupt mask when read data overflows (The CPU reads the FIFO when RX_FIFO is empty.) 0: not masked 1: masked

I2C_INTR_RAW

I2C_INTR_RAW is an I^{2}C raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x034	I2C_INTR_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gen_call	start_det	stop_det	activity	reserved	tx_abrt	reserved	tx_empty	tx_over	rx_full	rx_over	rx_under
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RO	gen_call	Interrupt status when a general call request is received 0: No interrupt is generated. 1: The slave receives the general call. **NOTE** This bit is set to 1 only when the general call request is received and confirmed. This value is retained unless being cleared.
[10]	RO	start_det	Start detect interrupt status, indicating whether the I^{2}C bus interface has the START or RESTART condition 0: No interrupt is generated. 1: The START or RESTART condition is detected.
[9]	RO	stop_det	Stop detect interrupt status, indicating whether the I^{2}C bus interface has the STOP condition 0: No interrupt is generated. 1: The STOP condition is detected.
[8]	RO	activity	Activity interrupt status. The I^{2}C activity status is recorded until the interrupt is cleared. 0: idle 1: busy

[7]	RO	reserved	Reserved
[6]	RO	tx_abrt	TX abort interrupt status 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** When this bit is set to 1, the I2C_TX_ABRT_SRC register indicates the reason for sending the interrupt. If this bit is set to a value, the I^2C clears TX_FIFO. TX_FIFO remains in this state until the interrupt is cleared. After the interrupt is cleared, TX_FIFO reads more data over the APB interface.
[5]	RO	reserved	Reserved
[4]	RO	tx_empty	Interrupt status when TX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** When data amount of TX_FIFO is below the threshold, this interrupt is automatically cleared. If the I^2C is disabled, TX_FIFO is cleared.
[3]	RO	tx_over	TX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_full	Interrupt status when RX_FIFO reaches or is below the threshold 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** This bit is set to 1 when RX_FIFO reaches or is below the threshold set by I2C_RX_TL. When RX_FIFO is below the threshold, this interrupt is automatically cleared. If the I^2C is disabled, RX_FIFO and this interrupt are automatically cleared.
[1]	RO	rx_over	RX_FIFO overflow interrupt status 0: No interrupt is generated. 1: An interrupt is generated. **NOTE** This bit is set to 1 if RX_FIFO is full but still receives bytes from the external I^2C device. The I^2C responds to data received over the I^2C bus. However, bytes received after RX_FIFO is full are lost.
[0]	RO	rx_under	Interrupt status when read data overflows (The CPU reads the FIFO when RX_FIFO is empty.) 0: No interrupt is generated. 1: An interrupt is generated.

I2C_RX_TL

I2C_RX_TL is an RX_FIFO threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x038	I2C_RX_TL	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_tl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	rx_tl	RX_FIFO threshold NOTE Valid values: 0–15. The actual value is the configured value plus 1. An rx_full interrupt is triggered when the number of data items in RX_FIFO is greater than or equal to the value. The upper threshold is configured as the RX_FIFO depth by default if the configured value is greater than the RX_FIFO depth.

I2C_TX_TL

I2C_TX_TL is a TX_FIFO threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x03C	I2C_TX_TL	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												tx_tl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	tx_tl	TX_FIFO threshold NOTE Valid values: 0–15. The actual value is equal to the configured value. A tx_empty interrupt is triggered when the amount of data in TX_FIFO is less than or equal to the value. The upper threshold is configured as the TX_FIFO depth by default if the configured value is greater than the TX_FIFO depth.

I2C_CLR_INTR

I2C_CLR_INTR is an I^2C interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x040	I2C_CLR_INTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															clr_intr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	clr_intr	Combined interrupts, all independent interrupts, and the I2C_TX_ABRT_SRC register are cleared when 1 is written to this bit.

I2C_ENABLE

I2C_ENABLE is an I^2C enable register.

Offset Address	Register Name	Total Reset Value
0x06C	I2C_ENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	enable	I^2C enable 0: disabled 1: enabled

I2C_STATUS

I2C_STATUS is an I^2C status register.

Offset Address	Register Name	Total Reset Value
0x070	I2C_STATUS	0x0000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								reserved	mst_activity	rx_fifo_full	rx_fifo_nempty	tx_fifo_nempty	tx_fifo_full	i2c_activity	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RO	reserved	Reserved
[5]	RO	mst_activity	I^2C master activity status 0: The master enters the idle state, and the I^2C is deactivated. 1: The master does not enter the idle state, and the I^2C is activated.
[4]	RO	rx_fifo_full	RX_FIFO full flag 0: not full 1: full
[3]	RO	rx_fifo_nempty	RX_FIFO non-empty flag 0: empty 1: non-empty
[2]	RO	tx_fifo_nempty	TX_FIFO empty flag 0: non-empty 1: empty
[1]	RO	tx_fifo_full	TX_FIFO non-full flag 0: full 1: not full
[0]	RO	i2c_activity	I^2C operating status 0: idle 1: active

I2C_TXFLR

I2C_TXFLR is a TX_FIFO valid data indicator register.

Offset Address	Register Name	Total Reset Value
0x074	I2C_TXFLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												tx_flr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RO	tx_flr	Number of valid data items in TX_FIFO The register is cleared when a tx_abort interrupt is generated.

I2C_RXFLR

I2C_RXFLR is an RX_FIFO valid data indicator register.

Offset Address	Register Name	Total Reset Value
0x078	I2C_RXFLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												rx_flr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RO	rx_flr	Number of valid data items in RX_FIFO The register is cleared when a tx_abort interrupt is generated.

I2C_SDA_HOLD

I2C_SDA_HOLD is an SDA hold time register.

Offset Address	Register Name	Total Reset Value
0x07C	I2C_SDA_HOLD	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sda_hold_fs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	sda_hold_fs	SDA hold time. The unit is the I^2C working frequency i2c_clk (50 MHz in normal mode). **NOTE** This bit indicates the delay from the SCL falling edge to SDA change. The SDA changes after the SCL falling edge and the delay (value of sda_hold_fs x cycle of i2c_clk). **NOTE** This bit must be set based on the speed mode.

I2C_TX_ABRT_SRC

I2C_TX_ABRT_SRC is an I^2C TX failure interrupt source register.

Offset Address	Register Name	Total Reset Value
0x080	I2C_TX_ABRT_SRC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																reserved	reserved	reserved	arb_lost	reserved	abrt_10b_rd_norstrt	abrt_sbyte_norstrt	reserved	abrt_sbyte_ackdet	reserved	abrt_gcall_read	abrt_gcall_noack	abrt_txdata_noack	abrt_10addr2_noack	abrt_10addr1_noack	abrt_7b_addr_noack
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RO	reserved	Reserved
[14]	RO	reserved	Reserved
[13]	RO	reserved	Reserved

[12]	RO	arb_lost	Whether an error occurs after the master loses the bus control permission 0: No error occurs. 1: An error occurs.
[11]	RO	reserved	Reserved
[10]	RO	abrt_10b_rd_norstrt	Whether an error occurs after the restart is disabled (I2C_CON[restart_en] set to 0) and the master attempts to initiate a read operation in 10-bit mode 0: No error occurs. 1: An error occurs.
[9]	RO	abrt_sbyte_norstrt	Whether an error occurs after the restart is disabled (I2C_CON[restart_en] set to 0) and a user attempts to initiate a start operation 0: No error occurs. 1: An error occurs.
[8]	RO	reserved	Reserved
[7]	RO	abrt_sbyte_ackdet	Whether an error occurs when the master sends a start command and receives a response 0: No error occurs. 1: An error occurs. (The slave does not need to respond to the start command.)
[6]	RO	reserved	Reserved
[5]	RO	abrt_gcall_read	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends a common request, but the user initiates a read operation after the request.
[4]	RO	abrt_gcall_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends a common request but does not receive a response from the slave over the bus.
[3]	RO	abrt_txdata_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: After the master sends an address and receives a response from the slave, the master sends data to the slave but does not receive any response.
[2]	RO	abrt_10addr2_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends address bit[10:8] the second time but does not receive any response from the slave when the master operates in 10-bit mode.

[1]	RO	abrt_10addr1_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends address bit[7:0] the first time but does not receive any response from the slave when the master operates in 10-bit mode.
[0]	RO	abrt_7b_addr_noack	tx_abort generation cause 0: tx_abort is triggered due to a reason not defined by the bit. 1: The master sends an address but does not receive the response from any slave on the bus when the master operates in 7-bit mode.

I2C_DMA_CR

I2C_DMA_CR is an I^2C DMA interface control register.

Offset Address	Register Name	Total Reset Value
0x088	I2C_DMA_CR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								rdmae	tdmae
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	rdmae	DMA enable for the TX FIFO 0: disabled 1: enabled
[0]	RW	tdmae	DMA enable for the RX FIFO 0: disabled 1: enabled

I2C_DMA_TDLR

I2C_DMA_TDLR is a TX_FIFO DMA operation threshold register.

Offset Address	Register Name	Total Reset Value
0x08C	I2C_DMA_TDLR	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dma_txtl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	dma_txtl	TX FIFO DMA threshold. When the number of data items of the TX FIFO is less than or equal to this value, a DMA operation request is sent. The DMA moves data to the TX FIFO.

I2C_DMA_RDLR

I2C_DMA_RDLR is an RX_FIFO DMA operation threshold register.

Offset Address	Register Name	Total Reset Value
0x090	I2C_DMA_RDLR	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dma_rxtl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	dma_rxtl	RX FIFO DMA threshold. When the number of data items of the TX FIFO is greater than or equal to this value, a DMA operation request is sent. The DMA moves data of the RX FIFO to the specified destination. The actual value is equal to the configured value plus 1.

I2C_SCL_SWITCH

I2C_SCL_SWITCH is an I^2C anti-suspend enable register.

Offset Address	Register Name	Total Reset Value
0x0A0	I2C_SCL_SWITCH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															scl_switch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	scl_switch	Master simulate SCL signal enable 0: disabled 1: enabled

I2C_SCL_SIM

I2C_SCL_SIM is an I^2C anti-suspend analog register.

Offset Address	Register Name	Total Reset Value
0x0A4	I2C_SCL_SIM	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															scl_sim
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	scl_sim	SCL enable signals simulated by the master 0: The output SCL is 0. 1: The output SCL is 1.

I2C_LOCK

I2C_LOCK is an I^{2}C lock register.

Offset Address	Register Name	Total Reset Value
0x0AC	I2C_LOCK	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															i2c_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	i2c_lock	I^{2}C lock register. To unlock the register, write 1ACCE551 to the register. To lock the register, write other values. When this register is read: 0: The register is unlocked, and all registers can be configured. 1: The register is locked, and only this register can be configured.

I2C_MST_SINGLE_CTRL

I2C_MST_SINGLE_CTRL is an I2C_MST_SINGLE_CTRL register.

Offset Address	Register Name	Total Reset Value
0x0B0	I2C_MST_SINGLE_CTRL	0x0030_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	single_model_en	single_model	single_addr_model	single_data_model	single_mst_tx_abrt_clr	single_tx_cmd_fifo_over_clr	single_rx_cmd_fifo_under_clr	single_rx_cmd_fifo_over_clr	single_mst_tx_abrt	single_tx_cmd_fifo_over	single_tx_cmd_fifo_not_full	single_tx_cmd_fifo_empty	reserved				single_tx_cmd_fifo_cnt				single_rx_cmd_fifo_under	single_rx_cmd_fifo_over	single_rx_cmd_fifo_full	single_rx_cmd_fifo_not_empty	reserved				single_rx_cmd_fifo_cnt			
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	single_model_en	I^{2}C master single operation enable control 0: disabled 1: enabled

[30]	RW	single_model	I^2C master single operation mode control 0: write 1: read
[29]	RW	single_addr_model	I^2C master single operation address mode control 0: The slave register has an 8-bit address width. 1: The slave register has a 16-bit address width.
[28]	RW	single_data_model	I^2C master single operation data mode control 0: The slave register has an 8-bit data width. 1: The slave register has a 16-bit data width.
[27]	WC	single_mst_tx_abrt_clr	Transmission failure indicator clear in single-operation mode
[26]	WC	single_tx_cmd_fifo_over_clr	SINGLE_TX_FIFO overflow indicator clear
[25]	WC	single_rx_cmd_fifo_under_clr	SINGLE_RX_FIFO read data overflow indicator clear
[24]	WC	single_rx_cmd_fifo_over_clr	SINGLE_RX_FIFO overflow indicator clear
[23]	RO	single_mst_tx_abrt	Transmission failure indicator in single-operation mode 0: No transmission failures occur. 1: A transmission failure occurs.
[22]	RO	single_tx_cmd_fifo_over	SINGLE_TX_FIFO overflow indicator 0: Data in SINGLE_TX_FIFO does not overflow. 1: Data in SINGLE_TX_FIFO overflows.
[21]	RO	single_tx_cmd_fifo_not_full	SINGLE_TX_FIFO non-full indicator 0: SINGLE_TX_FIFO is full. The FIFO has at least 16 data items. 1: SINGLE_TX_FIFO is not full. The FIFO has less than 16 data items.
[20]	RO	single_tx_cmd_fifo_empty	SINGLE_TX_FIFO empty indicator 0: There is data in the FIFO. 1: There is no data in the FIFO.
[19:17]	RO	reserved	Reserved
[16:12]	RO	single_tx_cmd_fifo_cnt	Number of valid data items in SINGLE_TX_FIFO This register is cleared when the I^2C master single operation is disabled (I2C_MST_SINGLE_CTRL[31] set to 0).
[11]	RO	single_rx_cmd_fifo_under	Overflow status when read data overflows (The CPU reads the FIFO when SINGLE_RX_FIFO is empty.) 0: No read data overflows. 1: Read data overflows.

[10]	RO	single_rx_cmd_fifo_over	SINGLE_RX_FIFO overflow status 0: Data in SINGLE_RX_FIFO does not overflow. 1: Data in SINGLE_RX_FIFO overflows.
[9]	RO	single_rx_cmd_fifo_full	SINGLE_RX_FIFO full indicator 0: SINGLE_RX_FIFO is not full. The FIFO has less than 16 data items. 1: SINGLE_RX_FIFO is full. The FIFO has at least 16 data items.
[8]	RO	single_rx_cmd_fifo_not_empty	SINGLE_RX_FIFO non-empty indicator 0: There is no data in the FIFO. 1: There is data in the FIFO.
[7:5]	RO	reserved	Reserved
[4:0]	RO	single_rx_cmd_fifo_cnt	Number of valid data items in SINGLE_RX_FIFO This register is cleared when the I^2C master single operation is disabled (I2C_MST_SINGLE_CTRL[31] set to 0).

I2C_MST_SINGLE_CMD

I2C_MST_SINGLE_CMD is an I2C_MST_SINGLE_CMD register.

Offset Address	Register Name	Total Reset Value
0x0B4	I2C_MST_SINGLE_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	single_addr																single_data															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	WO	single_addr	Address of the slave register accessed using the I^2C master single operation **NOTE** The lower 8 bits are sent first, and the upper 8 bits are sent at last.
[15:0]	RW	single_data	Data of the slave register accessed using the I^2C master single operation **NOTE** The lower 8 bits are sent first, and the upper 8 bits are sent at last.

I2C_SEQUENCE_CMD0

I2C_SEQUENCE_CMD0 is an I2C_SEQUENCE_CMD0 register.

Offset Address	Register Name	Total Reset Value
0x0B8	I2C_SEQUENCE_CMD0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_mode_en	sequential_rw	sequential_addr_mode		reserved			reserved	reserved		add_cnt_full	sequential_busy	sequential_finish				sequential_tx_fifo_cnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sequential_mode_en	Sequential mode enable (This function must be used together with the DMA.) 0: disabled 1: enabled
[30]	RW	sequential_rw	Operation type in sequential mode 0: read 1: write
[29:28]	RW	sequential_addr_mode	Start address type in sequential mode 00: 8 bits 00: 16 bits 10: 24 bits 11: 32 bits
[27]	RW	reserved	Reserved
[26:24]	RO	reserved	Reserved
[23]	RW	reserved	Reserved
[22]	RO	add_cnt_full	Start address transmission completion indicator, indicating that the DMA can be started
[21]	RO	sequential_busy	Operation busy indicator in sequential mode
[20]	RO	sequential_finish	Operation completion indicator in sequential mode
[19:0]	RO	sequential_tx_fifo_cnt	Number of completed operations in sequential mode

I2C_SEQUENCE_CMD1

I2C_SEQUENCE_CMD1 is an I2C_SEQUENCE_CMD1 register.

Offset Address	Register Name	Total Reset Value
0x0BC	I2C_SEQUENCE_CMD1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sequential_addr	Start address in sequential mode **NOTE** The lower 8 bits are sent first, and the upper 8 bits are sent at last.

I2C_SEQUENCE_CMD2

I2C_SEQUENCE_CMD2 is an I2C_SEQUENCE_CMD2 register.

Offset Address	Register Name	Total Reset Value
0x0C0	I2C_SEQUENCE_CMD2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sequential_length																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sequential_length	Sequential mode length The configured value is the actual value minus 1.

13.2 UART

13.2.1 Overview

The universal asynchronous receiver transmitter (UART) is an asynchronous serial communication interface. It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals. The UART is mainly used to interconnect the Hi3521A with the UART of an external chip so that the two chips can communicate with each other.

The Hi3521A provides three UART units (UART0 to UART3).

- UART0: a 4-wire UART for debugging, generating alarms, and controlling the pan-tilt-zoom (PTZ)
- UART1: a 2-wire UART for debugging, generating alarms
- UART2: a 2-wire UART for debugging and generating alarms

13.2.2 Features

The UART unit has the following features:

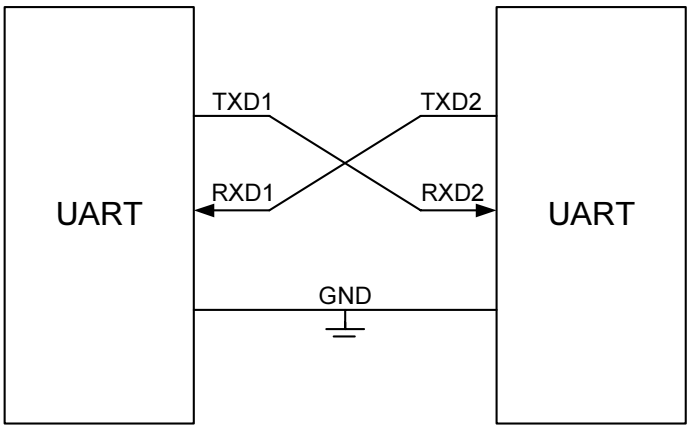
- Supports 64x8-bit transmit first-in, first-out (FIFO) and 64x12-bit RX FIFO.
- Supports programmable widths for the data bit and stop bit. The width of the data bit can be set to 5 bits, 6 bits, 7 bits, or 8 bits and width of the stop bit can be set to 1 bit or 2 bits by programming.
- Supports parity check or no check.
- Supports the programmable transfer rate.
- Supports RX FIFO interrupts, TX FIFO interrupts, RX timeout interrupts, and error interrupts.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Allows the UART or the TX/RX function of the UART to be disabled by programming to reduce power consumption.
- Allows the UART clock to be disabled to reduce power consumption.
- Supports DMA operations.

13.2.3 Function Description

Application Block Diagram

Figure 13-3 shows the typical application of the UART.

Figure 13-3 Typical application block diagram of the UART

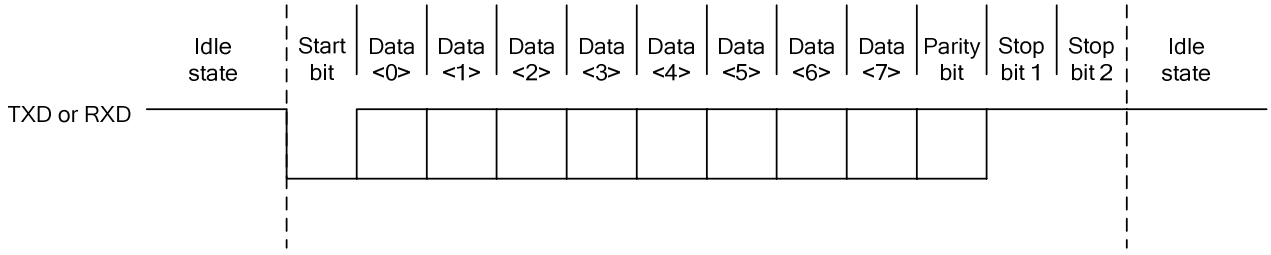


The UART serves as an asynchronous bidirectional serial bus. Through the UARTs connected by two data lines, a simplified and effective data transfer mode is implemented.

Function Principle

A frame transfer of the UART involves the start signal, data signal, parity bit, and stop signal, as shown in Figure 13-4. The data frame is output from the TXD end of one UART and then is input to the RXD end of the other UART.

Figure 13-4 Frame format of the UART



The definitions of the start signal, data signal, parity bit, and stop signal are as follows:

- Start signal (start bit)

  It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART does not transmit data, the level must remain high.

- Data signal (data bit)

  The data bit width can be set to 5 bits, 6 bits, 7 bits, or 8 bits according to the requirements in different applications.

- Parity bit

  It is a 1-bit error correction signal. The UART parity bit can be an odd parity bit, even parity bit, or stick parity bit. The UART can enable and disable the parity bit. For details, see the description of the

  UART_LCR_H register.

- Stop signal (stop bit)

  It is the stop bit of a data frame. The stop bit width can be set to 1 bit or 2 bits. The high level of TXD indicates the end of the data frame.

13.2.4 Operating Mode

13.2.4.1 Baud Rate Configuration

The operating baud rate of the UART can be set by configuring the registers UART_IBRD and UART_FBRD. The baud rate is calculated as follows:

Current baud rate = Frequency of the UART reference clock/(16 x Frequency divider). The frequency of the UART reference clock may be the APB bus clock frequency (50 MHz) or 6 MHz.

The clock frequency divider consists of the integral part and the fractional part that correspond to UART_IBRD and UART_FBRD respectively.

For example, assume that the frequency of the UART reference clock is 60 MHz. If UART_IBRD is set to 0x1E and UART_FBRD is set to 0x00, the current baud rate is calculated as follows: 60/(16 x 30) = 0.125 Mbit/s

The typical UART baud rates are 9600 bit/s, 14,400 bit/s, 19,200 bit/s, 38,400 bit/s, 57,600 bit/s, 76,800 bit/s, 115,200 bit/s, 230,400 bit/s, and 460,800 bit/s.

The following examples show how to calculate the clock divider and how to configure the clock divider register:

If the required baud rate is 230,400 bit/s and the frequency of the UART reference clock is 100 MHz, the clock divider is calculated as follows: $(100x10^6)/(16 \times 230,400) = 27.1267$. The integral part IBRD is 27 and the fractional part FBRD is 0.1267.

To calculate the value of the 6-bit UART_FBRD register, do as follows: calculate the value of *m* by using the following formula: $m = integer (FBRD \times 2^n + 0.5) = (0.1267 \times 2^6 + 0.5) = 8$(n = the width of UART_FBRD). Then set UART_IBRD to 0x001B and set UART_FBRD to 0x08.

If the fractional part of the frequency divider is set to 8, the actual divisor of the baud rate is 27 + 8/64 = 27.125, the baud rate is (100 x 16)/(16 x 27.125) = 230,414.75, and the error rate is (230,414.75 – 230,400)/230,400 x 100 = 0.006%.

The maximum error rate is 1/64 x 100 = 1.56% when the 6-bit UART_FBRD is used. If the value of *m* is 1, the total error rate is greater than 64 clock cycles.

13.2.4.2 Soft Reset

The UART controller can be separately reset by configuring the CRG registers.

- The UART0 controller can be separately reset by setting PERI_CRG33[7] to 1.
- The UART1 controller can be separately reset by setting PPERI_CRG33[8] to 1.
- The UART2 controller can be separately reset by setting PERI_CRG33[9] to 1.

NOTE

For details about reset registers, see section 3.2.7 "Register Description" in chapter 3 "System."

After reset, the configuration registers are restored to default values. Therefore, these registers must be initialized again.

13.2.4.3 Data Transfer in Interrupt or Query Mode

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to UART_CR[0] to disable the UART.

Step 2 Write to UART_IBRD and UART_FBRD to configure the transfer rate.

Step 3 Configure UART_CR and

Step 4 UART_LCR_H to set the UART operating mode.

Step 5 Configure UART_IFLS to set the thresholds of TX and RX FIFOs.

Step 6 If the driver runs in interrupt mode, set UART_IMSC to enable the corresponding interrupt; if the driver runs in query mode, disable the generation of corresponding interrupts.

Step 7 Write 1 to UART_CR[0] to enable the UART.

----End

Data Transmission

To transmit data, perform the following steps:

Step 1 Write the data to be transmitted to UART_DR and start data transmission.

Step 2 In query mode, check the TX_FIFO status by reading UART_FR[5] during the continuous data transmission. According to the TX_FIFO status, determine whether to transmit data to TX_FIFO. In interrupt mode, check the TX_FIFO status by reading the corresponding interrupt status bits and then determine whether to transmit data to TX_FIFO.

Step 3 Check whether the UART transmits all data by reading UART_FR[7]. If UART_FR[7] is 1, the UART transmits all data.

----End

Data Reception

To receive data, perform the following steps:

- In query mode, detect the RX_FIFO status by reading UART_FR[rxfe] during data reception and then determine whether to read data from the RX_FIFO according to the RX_FIFO status.
- In interrupt mode, determine whether to read data from RX_FIFO according to corresponding interrupt status bits.

13.2.4.4 Data Transfer in DMA Mode

Initialization

To initialize the UART, perform the following steps:

Step 1 Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Write values to UART_IBRD and UART_FBRD to configure the data transfer rate.

Step 3 Configure UART_CR and

Step 4 UART_LCR_H to set the UART operating mode.

Step 5 Configure UART_IFLS to set the TX and RX FIFO thresholds.

Step 6 If the driver runs in interrupt mode, set UART_IMSC to enable corresponding interrupts. If the driver runs in query mode, disable the generation of corresponding interrupts.

Step 7 Write 1 to UART_CR[uarten] to enable the UART.

----End

Data Transfer

To transmit data, perform the following steps (the following is an example using the DMA to transmit data):

Step 1 Configure the DMA data channel, including the transfer source address, transfer destination address, number of data items to be transferred, and transfer type. For details, see the description in xx "DMAC."

Step 2 Set UART_DMACR to 0x2 to enable the DMA transfer function of the UART.

Step 3 Check whether the data is transferred completely based on the interrupt report status of the DMA. If all data is transferred, disable the DMA transfer function of the UART.

----End

Data Reception

To receive data, perform the following steps (the following is an example using the DMA to receive data):

Step 1 Configure the DMA data channel, including data transfer source and destination addresses, data receive area address, number of data items to be transferred, and transfer type.

Step 2 Set UART_DMACR to 0x1 to enable the DMA receive function of the UART.

Step 3 Check whether the data is received completely by querying the DMA status. If all data is received, disable the DMA receive function of the UART.

----End

13.2.5 Register Summary

The Hi3521A provides three UART units: UART0, UART1 and UART2. Their base addresses are as follows:

- The base address of UART0 registers is 0x1208_0000.
- The base address of UART1 registers is 0x1209_0000.
- The base address of UART2 registers is 0x120A_0000.

Table 13-2 describes the UART registers.

Table 13-2 Summary of UART registers

Offset Address	Register	Description	Page
0x000	UART_DR	Data register	13-32
0x004	UART_RSR	Receive status register or error clear register	13-33
0x018	UART_FR	Flag register	13-34
0x024	UART_IBRD	Integral baud rate register	13-35
0x028	UART_FBRD	Fractional baud rate register	13-35
0x02C	UART_LCR_H	Line control register	13-36
0x030	UART_CR	Control register	13-37
0x034	UART_IFLS	Interrupt FIFO threshold select register	13-39
0x038	UART_IMSC	Interrupt mask register	13-40
0x03C	UART_RIS	Raw interrupt status register	13-41

Offset Address	Register	Description	Page
0x040	UART_MIS	Masked interrupt status register	13-42
0x044	UART_ICR	Interrupt clear register	13-43
0x048	UART_DMACR	DMA control register	13-44

13.2.6 Register Description

UART_DR

UART_DR is a UART data register that stores the received data and the data to be transmitted. The receive status can be queried by reading this register.

Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe	data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	RO	reserved	Reserved
[11]	RO	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. That is, a data segment is received when the RX FIFO is full.
[10]	RO	be	Break error 0: No break error occurs. 1: A break error occurs. That is, the time of RX data input signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[9]	RO	pe	Parity error 0: No parity error occurs. 1: A parity error occurs.
[8]	RO	fe	Frame error 0: No frame error occurs. 1: A frame error (namely, stop bit error) occurs.
[7:0]	RW	data	Data received and to be transmitted

UART_RSR

UART_RSR is a receive status register or error clear register.

- It acts as the receive status register when being read.
- It acts as the error clear register when being written.

You can query the receive status by reading UART_DR. The status information about the break, frame, and parity read from UART_DR has priority over that read from UART_RSR. That is, the status read from UART_DR changes faster than that read from UART_RSR.

UART_RSR is reset when any value is written to it.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved
[3]	RW	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. When the FIFO is full, the next data segment cannot be written to the FIFO and overflow occurs in the shift register. Therefore, the contents in the FIFO are valid. In this case, the CPU must read the data immediately to spare the FIFO.
[2]	RW	be	Break error 0: No break error occurs. 1: A break error occurs. A break error occurs when the time period during which the RX data signal keeps low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[1]	RW	pe	Parity error 0: No parity error occurs. 1: A parity error occurs when the received data is checked. In FIFO mode, the error is associated with the data at the top of the FIFO.
[0]	RW	fe	Frame error 0: No frame error occurs. 1: The stop bit of the received data is incorrect. The valid stop bit is 1.

UART_FR

UART_FR is a UART flag register.

Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								txfe	rxff	txff	rxfe	busy	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7]	RO	txfe	The definition of the bit is determined by the status of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is set to 1 when the TX holding register is empty. If UART_LCR_H[fen] is 1, this bit is set to 1 when the TX FIFO is empty.
[6]	RO	rxff	The definition of the bit is determined by the status of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is set to 1 when the RX holding register is full. If UART_LCR_H[fen] is 1, this bit is set to 1 when the RX FIFO is full.
[5]	RO	txff	The definition of the bit is determined by the status of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is set to 1 when the TX holding register is full. If UART_LCR_H[fen] is 1, this bit is set to 1 when the TX FIFO is full.
[4]	RO	rxfe	The definition of the bit is determined by the status of UART_LCR_H[fen]. If UART_LCR_H[fen] is 0, this bit is set to 1 when the RX holding register is empty. If UART_LCR_H[fen] is 1, this bit is set to 1 when the RX FIFO is empty.
[3]	RO	busy	UART busy/idle status 0: The UART is idle or data transmission is complete. 1: The UART is busy in transmitting data. If the bit is set to 1, the status is kept until the entire byte (including all stop bits) is transmitted from the shift register. Regardless of whether the UART is enabled, this bit is set to 1 when the TX FIFO is not empty.
[2:0]	RO	reserved	Reserved

UART_IBRD

UART_IBRD is an integral baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	baud divint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	baud divint	Clock frequency divider corresponding to the integral part of the baud rate. All bits are cleared after reset.

UART_FBRD

UART_FBRD is a fractional baud rate register.

CAUTION

- The values of UART_IBRD and UART_FBRD can be updated only after the current data is transmitted and received completely.
- The minimum clock frequency divider is 1 and the maximum divider is 65,535 (216 - 1). That is, UART_IBRD cannot be 0 and UART_FBRD is ignored if UART_IBRD is 0. Similarly, if UART_IBRD is equal to 65,535 (0xFFFF), UART_IBRD must be 0. If UART_FBRD is greater than 0, the data fails to be transmitted or received.

Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		baud divfrac					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	band divfrac	Clock frequency divider corresponding to the fractional part of the baud rate. All bits are cleared after reset.

UART_LCR_H

UART_LCR_H is a line control register. The registers

UART_LCR_H, UART_IBRD, and UART_FBRD are combined to form a 30-bit register. If UART_IBRD and UART_FBRD are updated,

UART_LCR_H must be updated at the same time.

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sps	wlen		fen	stp2	eps	pen	brk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7]	RW	sps	Parity select When bit 1, bit 2, and bit 7 of this register are set to 1, the parity bit is 0 during transmission and detection. When bit 1 and bit 7 of this register are set to 1 and bit 2 is set to 0, the parity bit is 1 during transmission and detection. When bit 1, bit 2, and bit 7 are cleared, the stick parity bit is disabled.
[6:5]	RW	wlen	Count of bits in a transmitted or received frame 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
[4]	RW	fen	TX/RX FIFO enable 0: disabled 1: enabled
[3]	RW	stp2	2-bit stop bit at the end of a transmitted frame 0: There is no 2-bit stop bit at the end of the transmitted frame. 1: There is a 2-bit stop bit at the end of the transmitted frame. The RX logic does not check for the 2-bit stop bit during data reception.
[2]	RW	eps	Parity select during data transmission and reception 0: The odd parity is generated or checked during data transmission and reception. 1: The even parity is generated or checked during data transmission and reception. When UART_LCR_H[fen] is 0, this bit becomes invalid.

[1]	RW	pen	Parity enable 0: The parity is disabled. 1: The parity is generated on the TX side and checked on the RX side.
[0]	RW	brk	Break transmit 0: invalid 1: After the current data transmission is complete, UTXD outputs low level continuously. **NOTE** This bit must retain 1 during the period of at least two full frames to ensure the break command is executed properly. In general, the bit must be set to 0.

UART_CR

UART_CR is a UART control register.

To configure UART_CR, perform the following steps:

Step 1 Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Wait until the current data transmission or reception is complete.

Step 3 Clear

Step 4 UART_LCR_H[fen].

Step 5 Configure UART_CR.

Step 6 Write 1 to UART_CR[uarten] to enable the UART.

----End

Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts	dtr	rxe	txe	lbe	reserved						uarten
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable 0: disabled 1: enabled. Data is transmitted only when the nUARTCTS signal is valid.
[14]	RW	rtsen	RTS hardware flow control enable 0: disabled 1: enabled. The data reception request is raised only when

			the RX FIFO has available space.
[13:12]	RO	reserved	Reserved
[11]	RW	rts	Request transmit This bit is the inversion of the status output signal nUARTRTS of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[10]	RW	dtr	Data transmit ready This bit is the inversion of the status output signal nUARTDTR of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[9]	RW	rxe	UART receive enable 0: disabled 1: enabled If the UART is disabled during data reception, the current data reception is stopped abnormally.
[8]	RW	txe	UART transmit enable 0: disabled 1: enabled If the UART is disabled during data transmission, the current data transmission is stopped abnormally.
[7]	RW	lbe	Loopback enable 0: disabled 1: UARTTXD is looped back to UARTRXD.
[6:1]	RO	reserved	Reserved
[0]	RW	uarten	UART enable 0: disabled 1: enabled If the UART is disabled during data reception and transmission, the data transfer is stopped abnormally.

UART_IFLS

UART_IFLS is an interrupt FIFO threshold select register. It is used to set a threshold for triggering a FIFO interrupt (UART_TXINTR or UART_RXINTR).

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										rxiflsel			txiflsel		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:6]	RO	reserved	Reserved
[5:3]	RW	rxiflsel	RX interrupt FIFO threshold select. An RX interrupt is triggered when any of the following conditions is met: 000: RX FIFO ≥ 1/8 full 001: RX FIFO ≥ 1/4 full 010: RX FIFO ≥ 1/2 full 011: RX FIFO ≥ 3/4 full 100: RX FIFO ≥ 7/8 full 101–111: reserved
[2:0]	RW	txiflsel	TX interrupt FIFO threshold select. A TX interrupt is triggered when any of the following conditions is met: 000: TX FIFO ≤ 1/8 full 001: TX FIFO ≤ 1/4 full 011: TX FIFO ≤ 3/4 full 010: TX FIFO ≤ 1/2 full 100: TX FIFO ≤ 7/8 full 101–111: reserved

UART_IMSC

UART_IMSC is an interrupt mask register. It is used to mask interrupts.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeim	beim	peim	feim	rtim	txim	rxim	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RW	oeim	Mask status of the overflow error interrupt 0: masked 1: not masked
[9]	RW	beim	Mask status of the break error interrupt 0: masked 1: not masked
[8]	RW	peim	Mask status of the parity interrupt 0: masked 1: not masked
[7]	RW	feim	Mask status of the frame error interrupt 0: masked 1: not masked
[6]	RW	rtim	Mask status of the RX timeout interrupt 0: masked 1: not masked
[5]	RW	txim	Mask status of the TX interrupt 0: masked 1: not masked
[4]	RW	rxim	Mask status of the RX interrupt 0: masked 1: not masked
[3:0]	RO	reserved	Reserved

UART_RIS

UART_RIS is a raw interrupt status register. The contents of this register are not affected by the UART_IMSC register.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeris	beris	peris	feris	rtris	txris	rxris	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RO	oeris	Status of the raw overflow error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	beris	Status of the raw break error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	peris	Status of the raw parity interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	feris	Status of the raw error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtris	Status of the raw RX timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	txris	Status of the raw TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxris	Status of the raw RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

UART_MIS

UART_MIS is a masked interrupt status register. The contents of this register are the results obtained after the raw interrupt status is ANDed with the interrupt mask status.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RO	oemis	Status of the masked overflow error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	bemis	Status of the masked break error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	pemis	Status of the masked parity interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	femis	Status of the masked error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtmis	Status of the masked RX timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	txmis	Status of the masked TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxmis	Status of the masked RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

UART_ICR

UART_ICR is an interrupt clear register. When 1 is written to it, the corresponding interrupt is cleared. Writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeic	beic	peic	feic	rtic	txic	rxic	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	WO	oeic	Overflow error interrupt clear 0: invalid 1: cleared
[9]	WO	beic	Break error interrupt clear 0: invalid 1: cleared
[8]	WO	peic	Parity interrupt clear 0: invalid 1: cleared
[7]	WO	feic	Error interrupt clear 0: invalid 1: cleared
[6]	WO	rtic	RX timeout interrupt clear 0: invalid 1: cleared
[5]	WO	txic	TX interrupt clear 0: invalid 1: cleared
[4]	WO	rxic	RX interrupt clear 0: invalid 1: cleared
[3:0]	RO	reserved	Reserved

UART_DMACR

UART_DMACR is a DMA control register. It is used to enable or disable the DMAs of the TX and RX FIFOs.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	RO	reserved	Reserved
[2]	RW	dmaonerr	DMA enable for the RX channel when the UART error interrupt (UARTEINTR) occurs. 0: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is valid. 1: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is invalid.
[1]	RW	txdmae	TX FIFO DMA enable 0: disabled 1: enable
[0]	RW	rxdmae	RX FIFO DMA enable 0: disabled 1: enable

13.3 SPI

13.3.1 Overview

The serial peripheral interface (SPI) controller implements serial-to-parallel conversion and parallel-to-serial conversion, and serves as a master to communicate with peripherals in synchronous and serial modes. The SPI controller supports three types of peripheral interfaces including the SPI, TI synchronous serial interface, and MicroWire interface.

13.3.2 Features

CAUTION

The Hi3521A has one group of SPIs. The SPI group supports two chip selects (CSs) with configurable polarity.

The Hi3520D V300 has one group of SPIs. The SPI group supports one chip select (CSs) with configurable polarity.

The Hi3521A SPIs are master interfaces. The working reference clock is the APB bus clock. The maximum working frequency of the SPI output clock is 31.25 MHz.

The SPI controller has the following features:

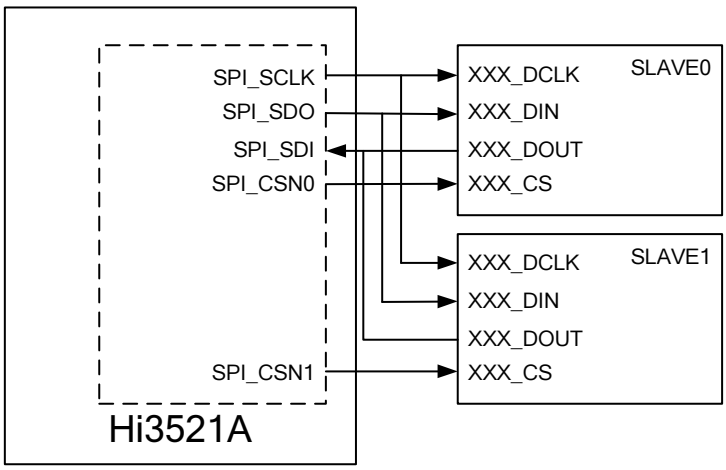
- Supports programmable frequency of the interface clock.
- Supports two separate FIFOs. One acts as an RX FIFO and the other one acts as a TX FIFO. Each of them is 16-bit wide and 256-location deep.
- Supports programmable serial data frame length: 4 bits to 16 bits.
- Provides internal loopback test mode.
- Supports the direct memory access (DMA) operation.
- Supports three types of peripheral interfaces including the SPI, MicroWire interface, and TI synchronous serial interface.
- Supports SPI in full-duplex mode and configurable clock polarity and phase.
- Supports MicroWire in half-duplex mode.
- Supports TI synchronous serial interface in full-duplex mode.

13.3.3 Function Description

Typical Application

Figure 13-5 shows the application block diagram when the SPI is connected to a slave device. The default CS pin SPI_CSN0 is used.

Figure 13-5 Application block diagram when the SPI is connected to a single slave device



13.3.4 Peripheral Bus Timings

The meanings of the abbreviations and acronyms in Figure 13-6 to Figure 13-13 are as follows:

- MSB: most significant bit
- LSB: least significant bit
- Q: Q is an undefined signal

SPI

NOTE

SPO indicates the polarity of SPICLKOUT and SPH indicates the phase of SPICLKOUT. They correspond to SPICR0 bit[7:6].

1. **SPO = 0, SPH = 0**

Figure 13-6 shows the SPI single frame format.

Figure 13-6 SPI single frame format (SPO = 0, SPH = 0)

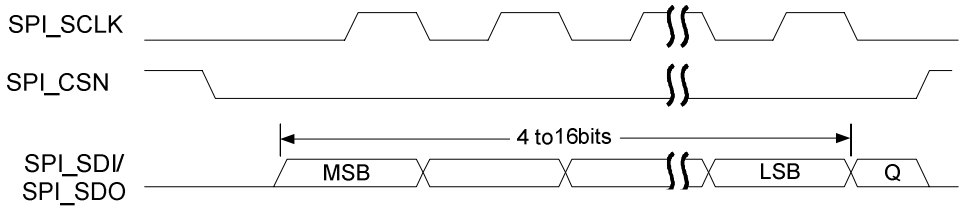
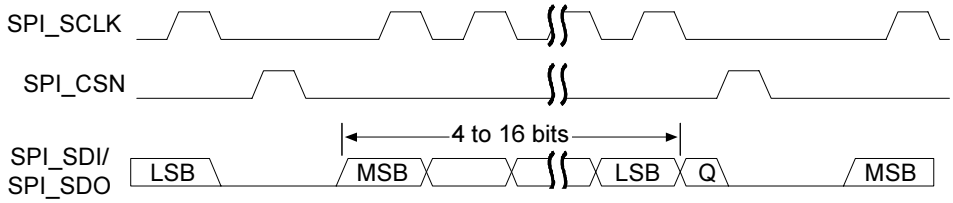


Figure 13-7 shows the SPI continuous frame format.

Figure 13-7 SPI continuous frame format (SPO = 0, SPH = 0)



When the SPI is idle in this mode:

- The SPI_SCLK signal is set to low.
- The SPI_CSN signal is set to high.
- The TX data line SPI_SDO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CSN signal is set to low. The data from the slave device is transferred to the RX data line SIP_DI of the master device immediately. Half SPI_SCLK clock cycle later, the valid master data is transmitted to SPI_SDO. At this time, both the master and slave data become valid. The SPI_SCLK pin changes to high level in the next half SPI_SCLK clock cycle. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_SCLK clock.

If a single word is transferred, SPI_CSN is restored to high level one SPI_SCLK clock later after the last bit is captured.

For continuous transfer, the SPI_CSN signal must pull up the SPI_SCLK clock by one clock cycle between the transfers of two words. When SPH is 0, the slave select pin fixes the data of the internal serial device register. Therefore, the master device must pull up the SPI_CSN signal between the transfers of two words in continuous transfer. When the continuous transfer ends, SPI_CSN is restored to high level one SPI_SCLK clock cycle later after the last bit is captured.

2. **SPO = 0, SPH = 1**

Figure 13-8 shows the SPI single frame format.

Figure 13-8 SPI single frame format (SPO = 0, SPH = 1)

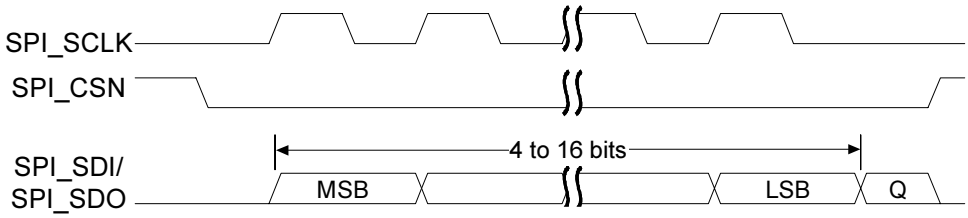
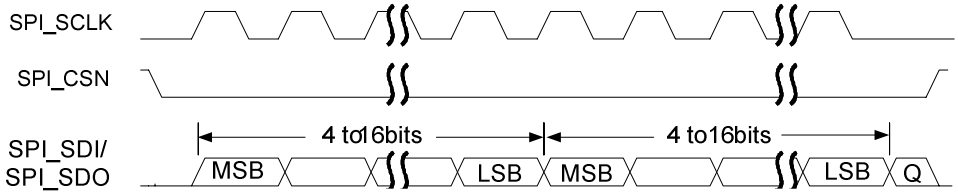


Figure 13-9 shows the SPI continuous frame format.

Figure 13-9 SPI continuous frame format (SPO = 0, SPH = 1)



When the SPI is idle in this mode:

- The SPI_SCLK signal is set to low.
- The SPI_CSN signal is set to high.
- The TX data line SPI_SDO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer start if the SPI_CSN signal is set to low. The master and slave data become valid on their respective transfer line half SPI_SCLK clock cycle later. In addition, SPI_SCLK becomes valid from the first rising edge. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_SCLK clock.

If a single word is transferred, SPI_CSN is restored to high level one SPI_SCLK clock later after the last bit is captured.

For a continuous transfer, SPI_CSN remains low between the transfers of two words. When the continuous transfer ends, SPI_CSN is restored to high level one SPI_SCLK clock cycle later after the last bit is captured.

3. **SPO = 1, SPH = 0**

Figure 13-10 shows the SPI single frame format.

Figure 13-10 SPI single frame format (SPO = 1, SPH = 0)

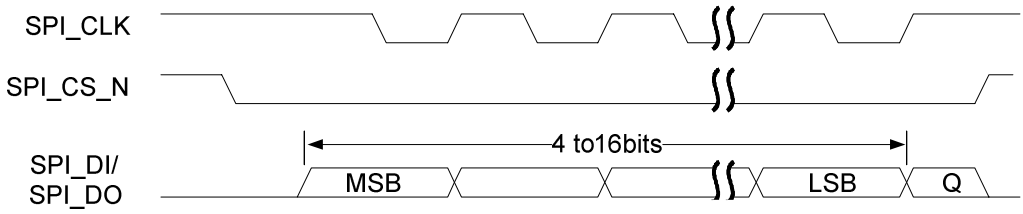
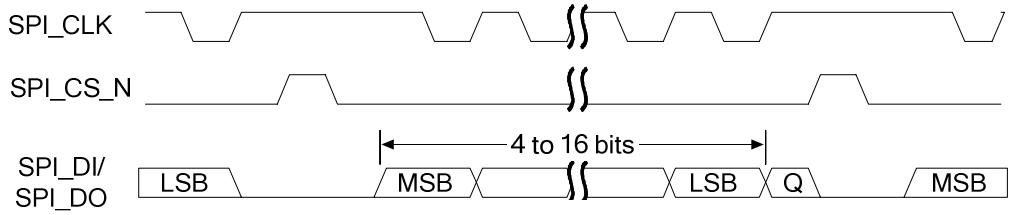


Figure 13-11 shows the SPI continuous frame format.

Figure 13-11 SPI continuous frame format (SPO = 1, SPH = 0)



When the SPI is idle in this mode:

- The SPI_SCLK signal is set to high.
- The SPI_CSN signal is set to high.
- The TX data line SPI_SDO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CSN signal is set to low. The data from the slave device is transferred to the RX data line SPI_SDI of the master device immediately. Half SPI_SCLK clock cycle later, the valid master data is transmitted to SPI_DO. After another half SPI_SCLK clock cycle, the SPI_SCLK master pin is set to low. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_SCLK clock.

If a single word is transferred, SPI_CSN is restored to high level after one SPI_SCLK clock since the data of the last bit is captured.

For a continuous transfer, the SPI_CSN signal must be pulled up between the transfers of two words. This is because that when SPH is 0, the slave select pin fixes the data of the internal serial device register. SPI_CSN is restored to high level one SPI_SCLK clock later after the last bit is captured.

4. **SPO = 1, SPH = 1**

Figure 13-12 shows the SPI single frame format.

Figure 13-12 SPI single frame format (SPO = 1, SPH = 1)

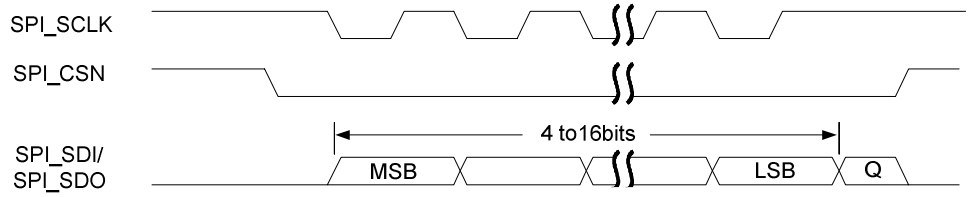
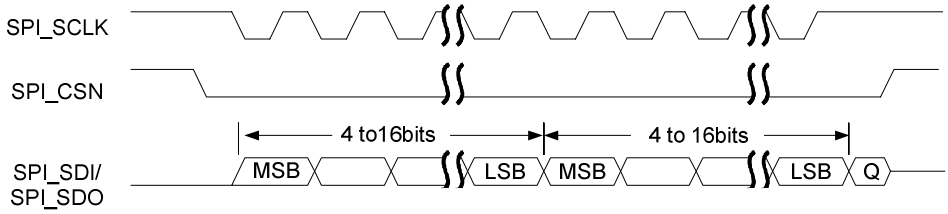


Figure 13-13 shows the SPI continuous frame format.

Figure 13-13 SPI continuous frame format (SPO = 1, SPH = 1)



When the SPI is idle in this mode:

- The SPI_SCLK signal is set to high.
- The SPI_CSN signal is set to high.
- The TX data line SDO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CSN signal is set to low. Half SPI_SCLK clock cycle later, the master data and slave data are valid on respective transfer line. In addition, SPI_SCLK becomes valid from a falling edge of SPI_SCLK. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_SCLK clock. If a single word is being transmitted, SPI_CSN is restored to high level one SPI_SCLK clock cycle later after the last bit is captured.

For a continuous transfer, the SPI_CSN signal remains low. SPI_CSN is restored to high level one SPI_SCLK clock cycle after the last bit is captured. For a continuous transfer, SPI_CSN remains low during transfer. The method of ending data transfer is the same as that in single transfer mode.

5. **Interface timings**

Figure 13-14 SPI timings

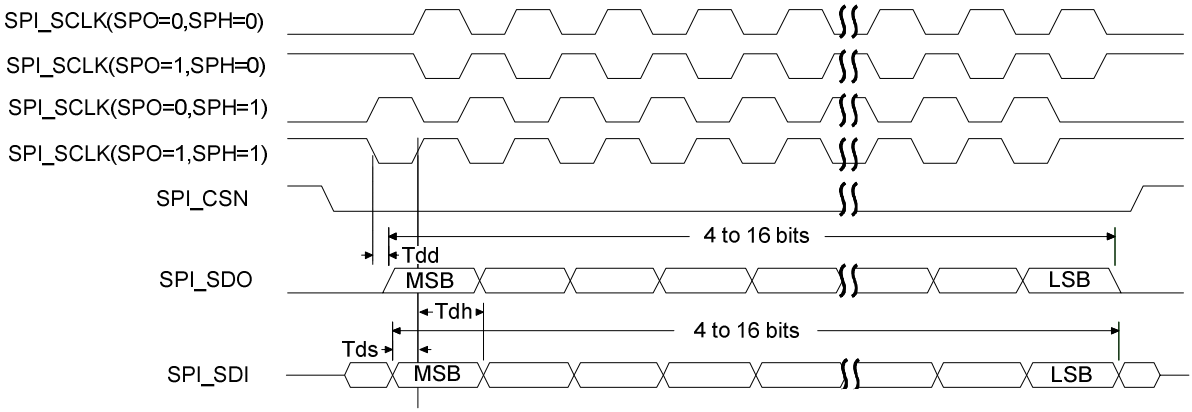


Table 13-3 Timing parameters of the SPI

Parameter	Description	Min	Max	Unit
Tdd	Output data delay	–3.5	5	ns
Tds	Input control signal setup time	23	None	ns
Tdh	Input control signal hold time	0	None	ns

TI Synchronous Serial Interface

Figure 13-15 shows the TI synchronous serial single frame format.

Figure 13-15 TI synchronous serial single frame format

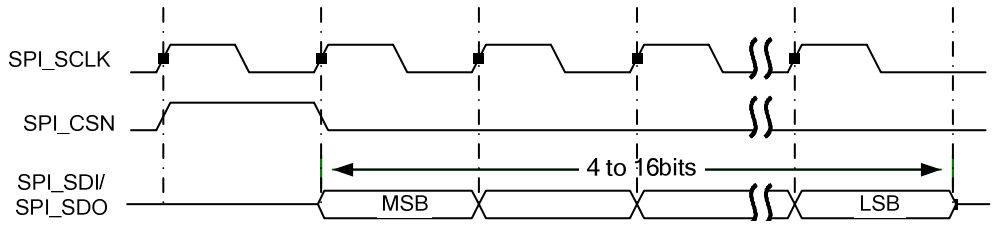
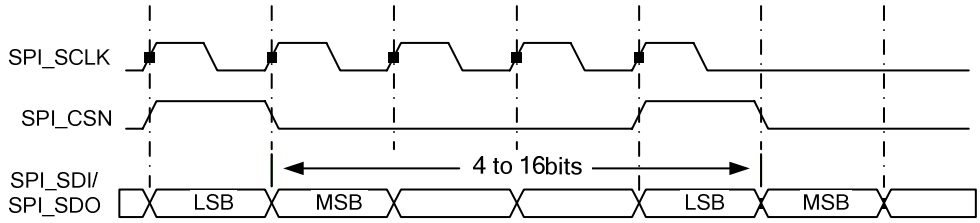


Figure 13-16 shows the TI synchronous serial continuous frame format.

Figure 13-16 TI synchronous serial continuous frame format



When the SPI is idle in this mode:

- The SPI_SCLK signal is set to low.
- The SPI_CSN signal is set to low.
- The transfer data line SPI_SDO retains high impedance.

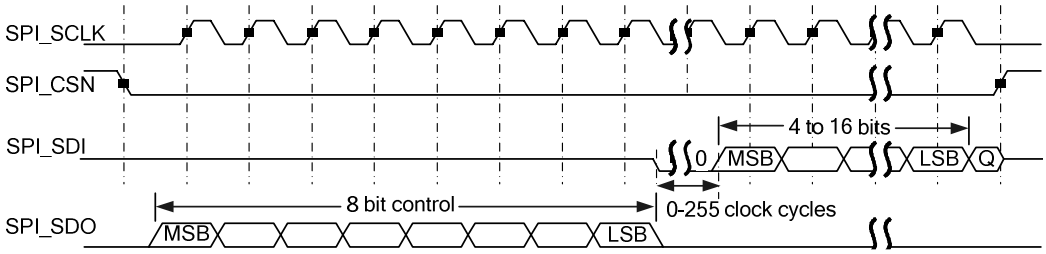
If there is data in the TX FIFO, SPI_CSN generates a high-level pulse in one SPI_SCLK clock cycle. Then, the data to be transmitted is transferred from the TX FIFO to the TX logic serial shift register. In addition, the MSBs of the data frames with the length of 4–16 bits are shifted and output from SPI_SDO on the next rising edge of the SPI_SCLK clock. Similarly, the MSB of the data received from the external serial slave device is shifted and input from the SPI_DI pin.

The SPI and off-chip serial device stores the data in the serial shift register on the falling edge of the SPI_SCLK clock. The RX serial register transmits the data to the RX FIFO on the rising edge of the first SPI_CK clock after receiving the LSB.

National Semiconductor Microwire Interface

Figure 13-17 shows the national semiconductor microwire single frame format.

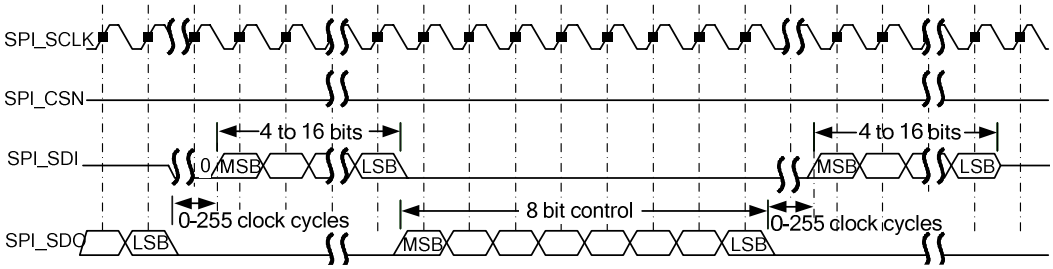
Figure 13-17 National semiconductor microwire single frame format



0 to 255 clock cycles can be delayed between the end of SPI_SDO LSB and the start of SPI_SDI MSB.

Figure 13-18 shows the national semiconductor microwire continuous frame format.

Figure 13-18 National semiconductor microwire continuous frame format



0 to 255 clock cycles can be delayed between the end of SPI_SDO LSB and the start of SPI_SDI MSB.

The microwire format is similar to the SPI format because both of them use the technology of transferring master-slave information. The only difference is that the SPI works in full-duplex mode and the microwire interface works in half-duplex mode. Before the SPI transmits serial data to the external chip, an 8-bit control word needs to be added. In this process, the SPI does not receive any data. After data transfer is complete, the external chip decodes the received data. One clock cycle later after 8-bit control information is transmitted, the slave device starts to respond to the required data. The returned data length is 4 bits to 16 bits, and the length of the entire frame is 13 bits to 25 bits.

When the SPI is idle in this mode:

- The SPI_SCLK signal is set to low.
- The SPI_CSN signal is set to high level.
- The TX data signal SPI_SDO is forced to low level.

Writing one control byte to the TX FIFO starts a data transfer. The data transfer is triggered on a falling edge of SPI_CSN. The data of the TX FIFO is sent to the serial shift register. The MSB of the 8-bit control frame is transmitted to the SPI_SDO pin. During frame transfer, SPI_CSN remains low. Whereas SPI_SDI retains high impedance.

The off-chip serial slave device latches the data to the serial shift register on each rising edge of the SPI_SCLK clock. After the slave device latches the data of the last bit, the slave device starts to decode the received data in the next clock cycle. Then, the slave device provides the data required by the SPI. Each bit is written to SPI_SDI on the falling edge of the SPI_SCLK clock. For a single data transfer, SPI_CSN is pulled up at the end of the frame one clock cycle after the last bit is written to the RX serial register. In this way, the RX data is transmitted to the RX FIFO.

The start and end for a continuous data transfer are the same as those for a signal data transfer. During the continuous data transfer, SPI_CSN retains low and the data transferred is continuous. The control word of the next frame is adjacent to the LSB of the previous frame. When the LSB of the frame is latched to the SPI, each received value is originated from the receive shift register on the falling edge of the SPI_SCLK clock.

13.3.5 Operating Mode

Working Modes

The SPI working modes include the data transmission in the interrupt or query mode and the data transmission in the DMA mode.

Clock and Reset

The frequency of the output SPI clock is calculated as follows:

Fsspclkout = Fsspclk/[CPSDVR x (1 + SCR)]

Fsspclk is the working reference clock of the SPI and its value is 1/4 of the bus clock.

For details about CPSDVR and SCR, query the corresponding registers.

The SPI of the Hi3521A supports separately soft reset, which is controlled by the PERI_CRG33 bit[5] register. To disable the soft reset on the SPI, write 0 to corresponding bits. To enable soft-reset on the SPI, write 1 to corresponding bits. The default value is 0 when the SPI is powered on.

Interrupts

The SPI has five interrupts. Four of them have separate interrupts sources and maskable and active high.

- SPIRXINTR

  RX FIFO interrupt request. When there are four or more valid data segments in the RX FIFO, the interrupt is set to 1.

- SPITXINTR

  TX FIFO interrupt request. When there are four or less valid data segments in the TX FIFO, the interrupt is set to 1.

- SPIRORINTR

  RX overrun interrupt request. When the FIFO is full and new data is written to the FIFO, the FIFO is overrun and the interrupt is set to 1. In this case, the data is written to the RX shift register rather than the FIFO.

- SPIRTINTR

  RX timeout interrupt request. When the RX FIFO is not empty and the SPI is idle for more than a fixed 32-bit cycle, the interrupt is set to 1.

  It indicates that data in the RX FIFO needs to be transmitted. When the RX FIFO is empty or new data is transmitted to SPIRXD, the interrupt is cleared. The interrupt can also be cleared by writing to the SPIICR[RTIC] register.

- SPIINTR

  Combined interrupt. This interrupt is obtained by performing an OR operation on the preceding four interrupts. If any of the preceding four interrupts is set to 1 and enabled, SPIINTR is set to 1.

For details about how to connect the SPIINTR of SPI, see "Interrupts" in this section.

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to SPICR1[sse] to disable the SPI.

Step 2 Write to SPICR0 to set the parameters such as the frame format and transfer data bit width.

Step 3 Configure SPICPSR to set the required clock divider.

Step 4 In the interrupt mode, configure SPIIMSC to enable the corresponding interrupts or disable the generation of corresponding interrupts in query or DMA mode.

Step 5 Configure SPITXFIFOCR and SPIRXFIFOCR in interrupt or DMA mode.

Step 6 Configure SPIDMACR to enable the DMA function of the SPI in DMA mode.

----End

Data Transfer in Query Mode

The full status of the TX or RX FIFO is not considered, because the depth of the TX FIFO or RX FIFO is 512.

Perform the following steps:

Step 1 Write 1 to SPICR1[sse] to enable the SPI.

Step 2 Write the data to be transmitted to SPIDR continuously.

Step 3 Poll SPISR until SPISR[BSY] is 0, SPISR[TFE] is 1, and SPISR[RNE] is 1. If SPISR[BSY] is 0, the bus is busy; if SPISR[TFE] is 1, the TX FIFO is empty; if SPISR[RNE] is 1, the RX FIFO is not empty.enter “Step 5”.

Step 4 Read data until the RX FIFO is empty. You can check whether the RX FIFO is empty by querying SPISR[RNE].

CAUTION

The SPI/Microwire has full-duplex features. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the RX FIFO must be cleared.

Step 5 Write 0 to SPICR1[sse] to disable the SPI.

----End

Data Transfer in Interrupt Mode

Perform the following steps:

Step 1 Write 1 to SPICR1[sse] to disable the SPI.

Step 2 Write the data to be transmitted to SPIDR continuously.

Step 3 Wait for the interrupt SPIRXINTR and read data in cyclic mode until all data is read.

Note that the full-duplex features of the SPI/Microwire. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the RX FIFO must be cleared.

Step 4 Write 0 to SPICR1[sse] to disable the SPI.

----End

Data Transfer in DMA Mode

Perform the following steps:

Step 1 Obtain a DMAC channel.

Step 2 Write 1 to SPICR1[sse] to disable the SPI.

Step 3 Transmit data.

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SPI TX FIFO for the data transfer.
3. Check whether all data is transmitted by viewing the DMA interrupt. If all data is transmitted, disable the DMA transmit function of the SPI.

Step 4 Receive data

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SSP RX FIFO for the data transfer.
3. Check whether all data is received by viewing the DMA interrupt. If all data is received, disable the DMA receive function of the SPI.

Step 5 Write 0 to SPICR1[sse] to disable the SPI.

----End

13.3.6 Register Summary

Table 13-4 describes the registers.

Table 13-4 Summary of SPI registers (base address: 0x120D_0000)

Offset Address	Register	Description	Page
0x000	SPICR0	Control register 0	13-56
0x004	SPICR1	Control register 1	13-57
0x008	SPIDR	Data register	13-58
0x00C	SPISR	Status register	13-58
0x010	SPICPSR	Clock divider register	13-59
0x014	SPIIMSC	Interrupt mask register	13-60

Offset Address	Register	Description	Page
0x018	SPIRIS	Raw interrupt status register	13-61
0x01C	SPIMIS	Masked interrupt status register	13-61
0x020	SPIICR	Interrupt clear register	13-62
0x024	SPIDMACR	DMA control register	13-62
0x028	SPITXFIFOCR	TX FIFO control register	13-63
0x02C	SPIRXFIFOCR	RX FIFO control register	13-64

13.3.7 Register Description

SPICR0

SPICR0 is SPI control register 0.

Offset Address	Register Name	Total Reset Value
0x000	SPICR0	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCR								SPH	SPO	FRF		DSS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	SCR	Serial clock rate, ranging from 0 to 255. The value of the SCR is used to generate the TX and RX bit rates of the SPI. The formula is as follows: FSSPCLK/(CPSDVSR (1 + SCR). CPSDVSR is an even ranging from 2 to 254, and it is configured by SPICPSR.
[7]	RW	SPH	SPICLKOUT phase. For details, see the "SPI frame format of Peripheral Bus Timings" in section 13.3.4 “Peripheral Bus Timings.”
[6]	RW	SPO	SPICLKOUT polarity. For details, see the "SPI Frame Format of Peripheral Bus Timings" in section 13.3.4 “Peripheral Bus Timings.”
[5:4]	RW	FRF	Frame format select 00: Motorola SPI frame format 01: TI synchronous serial frame format 10: National microwire frame format 11: reserved
[3:0]	RW	DSS	Data width 0011: 4 bits

			1000: 9 bits 1101: 14 bits 0100: 5 bits 1001: 10 bits 1110: 15 bits 0101: 6 bits 1010: 11 bits 1111: 16 bits 0110: 7 bits 1011: 12 bits 0111: 8 bits 1100: 13 bits Other values: reserved

SPICR1

SPICR1 is SPI control register 1.

Offset Address	Register Name	Total Reset Value
0x004	SPICR1	0x7F00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WaitEn	WaitVal							reserved			BigEnd	reserved	MS	SSE	LBM
Reset	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	WaitEn	Wait enable. This bit is valid when the SPICR0[FRF] is set to the national microwire frame format. 0: disabled 1: enabled
[14:8]	RW	WaitVal	Number of waiting beats between read and write when in the national microwire frame format. When WaitEn is 1 and the frame format is national microwire, WaitVal is valid.
[7:5]	RW	reserved	Reserved
[4]	RW	BigEnd	Data endian mode 0: little endian 1: big endian
[3]	RW	reserved	Reserved

[2]	RW	MS	Master or slave mode. This bit can be changed only when the SPI is disabled. 0: master mode (default value) 1: reserved
[1]	RW	SSE	SPI enable 0: disabled 1: enabled
[0]	RW	LBM	Loopback mode 0: A normal serial port operation is enabled. 1: The output of the TX serial shift register is connected to the input of the RX serial shift register.

SPIDR

SPIDR is a data register.

Offset Address	Register Name	Total Reset Value
0x008	SPIDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	DATA	TX or RX FIFO Read: RX FIFO Write: TX FIFO If the data is less than 16 bits, the data must be aligned to the right. The TX logic ignores the unused upper bits, and the RX logic automatically aligns the data to the right.

SPISR

SPISR is a status register.

Offset Address	Register Name	Total Reset Value
0x00C	SPISR	0x0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											BSY	RFF	RNE	TNF	TFE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[15:5]	RW	reserved	Reserved
[4]	RW	BSY	SPI busy flag 0: idle 1: busy
[3]	RW	RFF	Whether the RX FIFO is full 0: not full 1: full.
[2]	RW	RNE	Whether the RX FIFO is not empty 0: empty 1: not empty
[1]	RW	TNF	Whether the TX FIFO is not full 0: full 1: not full
[0]	RW	TFE	Whether the TX FIFO is empty 0: not empty 1: empty

SPICPSR

SPICPSR is a clock divider register.

Offset Address	Register Name	Total Reset Value
0x010	SPICPSR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								CPSDVSR							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	reserved	Reserved
[7:0]	RW	CPSDVSR	Clock divider. The value must be an even ranging from 2 to 254. It depends on the frequency of the input clock SPICLK. The LSB is read as 0.

SPIIMSC

SCIIMSC is an interrupt mask register. The value 0 indicates an interrupt is masked and the value1 indicates an interrupt is not masked.

Offset Address	Register Name	Total Reset Value
0x014	SPIIMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXIM	RXIM	RTIM	RORIM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RW	reserved	Reserved
[3]	RW	TXIM	TX FIFO interrupt mask 0: The interrupt is masked when only half of or less data is left in the TX FIFO. 1: The interrupt is not masked when only half of or less data is left in the TX FIFO.
[2]	RW	RXIM	RX FIFO interrupt mask 0: The interrupt is masked when only half of or less data is left in the RX FIFO. 1: The interrupt is not masked when only half of or less data is left in the RX FIFO.
[1]	RW	RTIM	RX timeout interrupt mask 0: masked 1: not masked
[0]	RW	RORIM	RX overflow interrupt mask 0: masked 1: not masked When the value is 1, the hardware stream control function is enabled. That is, when the RX FIFO is full, the SPI stops transmitting data.

SPIRIS

SPIRIS is a raw interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x018	SPIRIS	0x0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXRIS	RXRIS	RTRIS	RORRIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RO	TXRIS	Raw TX FIFO interrupt status
[2]	RO	RXRIS	Raw RX FIFO interrupt status
[1]	RO	RTRIS	Raw RX timeout interrupt status
[0]	RO	RORRIS	Raw RX overflow interrupt status

SPIMIS

SPIMIS is a masked interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x01C	SPIMIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXMIS	RXMIS	RTMIS	RORMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RO	TXMIS	Status of the masked TX FIFO interrupt
[2]	RO	RXMIS	Status of the masked RX FIFO interrupt
[1]	RO	RTMIS	Status of the masked RX timeout interrupt
[0]	RO	RORMIS	Status of the masked RX overflow interrupt

SPIICR

SCIICR is an interrupt clear register. Writing 1 clears an interrupt, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x020	SPIICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														RTIC	RORIC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved
[1]	RO	RTIC	RX timeout interrupt clear
[0]	RO	RORIC	RX overflow interrupt clear

SPIDMACR

SCIDMACR is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x024	SPIDMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														TXDMAE	RXDMAE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	WO	reserved	Reserved
[1]	WO	TXDMAE	DMA TX FIFO enable 0: disabled 1: enabled
[0]	WO	RXDMAE	DMA RX FIFO enable 0: disabled 1: enabled

SPITXFIFOCR

SPITXFIFOCR is a TX FIFO control register.

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										TXINTSize			DMATXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved
[5:3]	RW	TXINTSize	Threshold for generating the TX FIFO request interrupt. That is, when the number of data segments in the TX FIFO is less than or equal to the value of TXINTSize, TXRIS is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMATXBRSize	Threshold for generating the TX FIFO request DMA transfer burst. That is, when the number of data segments in the TX FIFO is less than or equal to the configured value (256 – DMATXBRSize), DMATXBREQ is valid. The width of the TX FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 128

SPIRXFIFOCR

SPIRXFIFOCR is an RX FIFO control register.

Offset Address	Register Name	Total Reset Value
0x02C	SPIRXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										RXINTSize			DMARXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved
[5:3]	RW	RXINTSize	Threshold for generating the RX FIFO request interrupt. That is, when the number of data segments in the TX FIFO is less than or equal to the configured value (256 – RXINTSize), RXRIS is valid. The width of the RX FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMARXBRSize	Burst transfer threshold. When this threshold is reached, the RX FIFO asks the DMA to perform a burst transfer. That is, when number of data segments in the TX FIFO is less than or equal to the value of DMARXBRSize, DMARXBREQ is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 224

13.4 IR Interface

13.4.1 Overview

The infrared (IR) module receives data over the IR interface.

13.4.2 Features

The IR module has the following features:

- Allows you to disable the IR receive module by using software.
- Supports two operating modes:
  - Mode 0: supports decoding in four formats (including NEC with simple repeat code, NEC with full repeat code, SONY, and TC9012), error detection on received data, and IR wakeup.
  - Mode 1: supports the symbol level width detection in any data format.
- In mode 0, supports the RX data overflow interrupt, RX data frame format error interrupt, RX data frame interrupt, key release interrupt, and combined interrupt.
- In mode 1, supports the RX symbol overflow interrupt, RX symbol interrupt, symbol timeout interrupt, and combined interrupt.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Supports interrupt clear and mask (write to clear).
- Supports IR wakeup.
- Supports the reference clock frequency ranging from 1 MHz to 128 MHz and controls the clock frequency divider by software programming, enabling the frequency of the working clock to be prescaled to 1 MHz.

13.4.3 Function Description

The IR module receives infrared signals transmitted by the infrared remote control, decodes the signals, and then transmits the decoded signals to the ARM system. The ARM system performs corresponding operations according to the received codes, which implements expected functions. The IR module connects to the APB of the ARM subsystem. When the chip is in the low-power state (the CPU is at a low frequency), the IR module generates an interrupt after receiving a complete frame, and transmits the interrupt to the CPU. In this way, the IR wake function is implemented.

The analysis of the signals transmitted by various infrared remote controls shows that the lead codes in the infrared commands vary according to remote controls. In addition, the subsequent control commands and the bits of command codes are also different. This is because infrared remote controls are not designed based on a unified infrared remote control standard. The basic encoding principles, however, are the same. That is, the pulses with different periods and duty ratios are used to represent 0 and 1. The duty ratios and pulse cycles may vary according to remote controls. Based on preceding differences, the code formats of the infrared data are classified into NEC with simple repeat code, NEC with full repeat code, TC9012 code, and SONY code.

Note that the parameter values corresponding to the code formats in the following tables are only for reference. The actual measured parameter values prevail.

Table 13-5 to Table 13-7 describe the code formats of the received infrared data.

Table 13-5 Code formats of the received infrared data (NEC with simple repeat code)

Data Format		NEC with Simple Repeat Code			
		uPD6121G	D6121/BU5777/D1913	LC7461M-C13	AEHA
Lead code (10 μs)	LEAD_S	900	900	900	337.6
	LEAD_E	450	450	450	168.8
Bit0 (10 μs)	B0_L	56	56	56	42.2
	B0_H	56	56	56	42.2
Bit1 (10 μs)	B1_L	56	56	56	42.2
	B1_H	169	169	169	126.6
Simple repeat code (10 μs)	SLEAD_S	900	900	900	337.6
	SLEAD_E	225	225	225	337.6
Burst (10 μs)		55	55	55	42.2
Frame length (10 μs)		108,00	10,800	10,800	8,777.6 – 12,828.8
Valid data bit		32	32	42	48

Table 13-6 Code formats of the received infrared data (NEC with full repeat code)

Data Format		NEC with Full Repeat Code						
		uPD6121G	LC7461M-C13	MN6024-C5D6	MN6014-C6D6	MATNEW	MN6030	PANASONIC
Lead code (10 μs)	LEAD_S	900	900	337.6	349.2	348.8	349	352
	LEAD_E	450	450	337.6	349.2	374.4	349	352
Bit 0 (10 μs)	B0_L	56	56	84.4	87.3	43.6	87.3	88
	B0_H	56	56	84.4	87.3	43.6	87.3	88
Bit 1 (10 μs)	B1_L	56	56	84.4	87.3	43.6	87.3	88
	B1_H	169	169	253.2	174.6	130.8	261.9	264
Simple repeat code (10 μs)	SLEAD_S	None	None	None	None	None	None	None
	SLEAD_E							
Burst (10 μs)		55	55	84.4	87.3	43.6	87.3	88
Frame length (10 μs)		10,800	10,800	10,130	10,470	12,413.6 – 16,594.4	10,500	10,400
Valid data bit		32	42	22	24	48	22	22

Table 13-7 Code formats of the received infrared data (TC9012 code and SONY code)

Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
Lead code (10 μs)	LEAD_S	450	240	240	240	240
	LEAD_E	450	60	60	60	60
Bit0 (10 μs)	B0_L	56	60	60	60	60
	B0_H	56	60	60	60	60
Bit1 (10 μs)	B1_L	56	120	120	120	120
	B1_H	169	60	60	60	60
Simple repeat code (10 μs)	SLEAD_S	None	None	None	None	None
	SLEAD_E					
Burst (10 μs)		56	None	None	None	None
Frame length (10 μs)		10,800	4500	4500	4500	4500
Valid data bit		32	12	13	15	20

13.4.3.1 NEC with Simple Repeat Code

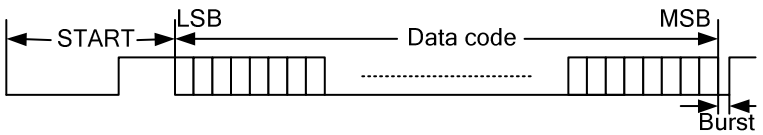
Frame Format

The NEC with simple repeat code consists of the following:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on specific code format. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

Figure 13-19 shows the frame format of transmitting a single NEC with simple repeat code.

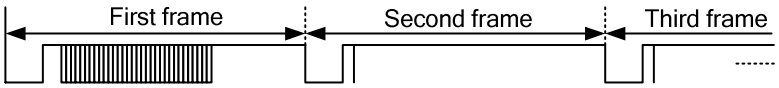
Figure 13-19 Frame format for transmitting a single NEC with simple repeat code



If a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists only of a simple lead code and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). Figure

13-20 shows the frame format for transmitting NEC with simple repeat codes by pressing the key continuously.

Figure 13-20 Frame format for transmitting NEC with simple repeat codes by pressing the key continuously



Code Format

Figure 13-21 shows the definitions of bit0 and bit1 of the NEC with simple repeat code.

Figure 13-21 Definitions of bit0 and bit1 of the NEC with simple repeat code

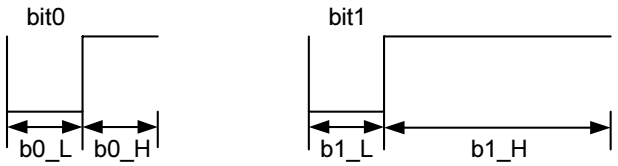


Figure 13-22 shows the format for transmitting a single NEC with simple repeat code. Figure 13-23 shows the format for transmitting consecutive NEC with simple repeat codes.

Figure 13-22 Format for transmitting a single NEC with simple repeat code

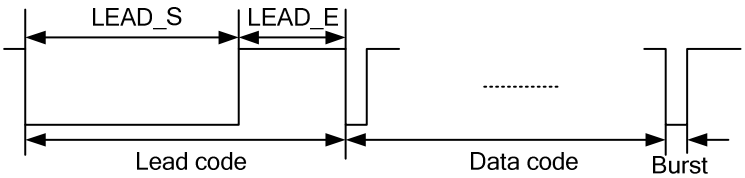
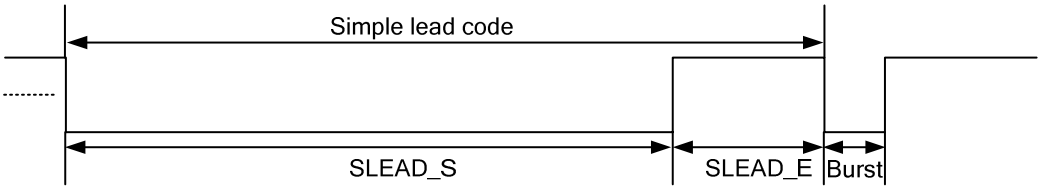


Figure 13-23 Code format for transmitting consecutive NEC with simple repeat codes



NOTE

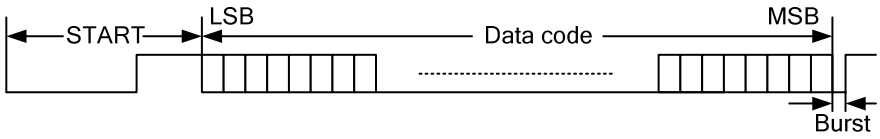
- The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 13-5 to Table 13-7.
- The frame length must be less than or equal to 160 ms. Otherwise, the simple lead code cannot be identified.

13.4.3.2 NEC with Full Repeat Code

Frame Format

The data format of the NEC with full repeat code consists of the following parts: START (lead code), data code, and burst. START (lead code): Consists of a start code (low level) and an end code (high level). Data code: The valid bits and the definition of each bit are determined by the specific code format. During data code reception, its LSB is received first. Burst signal: It is used to receive the last data bit. Figure 13-24 shows the frame format for transmitting a single NEC with full repeat code.

Figure 13-24 Frame format for transmitting a single NEC with full repeat code



If a complete data frame (first frame) is received after the key is held down for more than one frame length, the subsequently received data frame is still a complete data frame. That is, the first frame is transmitted repeatedly based on the frame length. Figure 13-25 shows the frame format for transmitting NEC with full repeat codes by pressing the key continuously.

Figure 13-25 Frame format for transmitting NEC with full repeat codes by pressing the key continuously

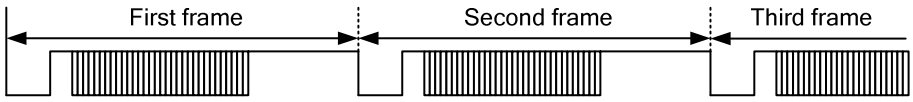


Figure 13-24 and Figure 13-25 show that the only difference between the NEC with simple repeat code and the NEC with full repeat code is the format of the repeat frame. For the NEC with simple repeat code, the simple lead code is transmitted; for the NEC with full repeat code, the complete frame is transmitted. That is, the first frame and the repeat frame are the same.

Code Format

Figure 13-26 shows the definitions of bit0 and bit1 of the NEC with full repeat code.

Figure 13-26 Definitions of bit0 and bit1 of the NEC with full repeat code

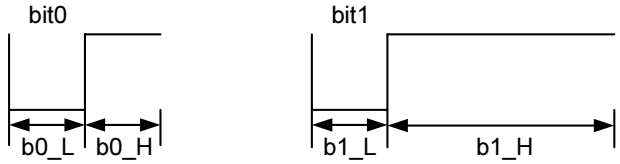
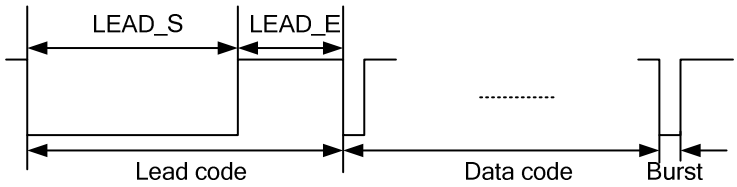


Figure 13-27 shows the format for transmitting a single NEC with full repeat code.

Figure 13-27 Format for transmitting a single NEC with full repeat code



NOTE

The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 13-5 to Table 13-7.

13.4.3.3 TC9012 Code

Frame Format

CAUTION

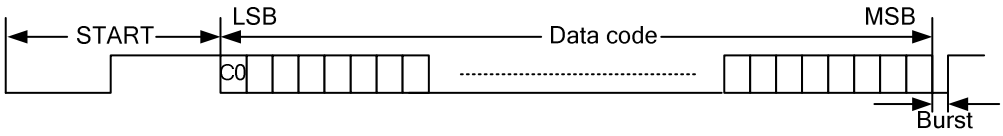
According to the features of the TC9012 code, the first bit of all key codes must be all 1s or all 0s. Otherwise, unnecessary frames are generated when the key are pressed continuously.

The TC9012 code consists of the following parts:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on the specific code pattern. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

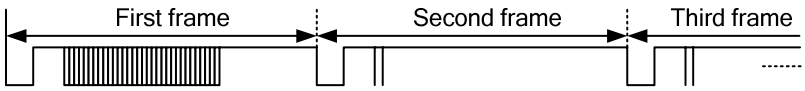
Figure 13-28 shows the frame format for transmitting a single TC9012 code.

Figure 13-28 Frame format for transmitting a single TC9012 code



When a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists of a lead code, a data bit, and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). The data bit is the complement of the first data bit (C0) received in the previous frame. Figure 13-29 shows the frame format for transmitting TC9012 codes by pressing the key continuously.

Figure 13-29 Frame format for transmitting TC9012 codes by pressing the key continuously



Code Format

Figure 13-30 shows the definitions of bit0 and bit1 of the TC9012 code.

Figure 13-30 Definitions of bit0 and bit1 of the TC9012 code

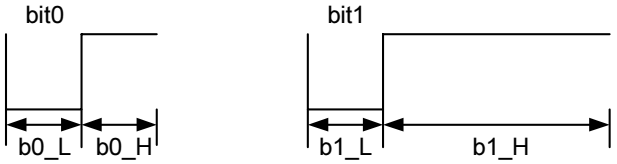


Figure 13-31 shows the format for transmitting a single TC9012 code.

Figure 13-31 Format for transmitting a single TC9012 code

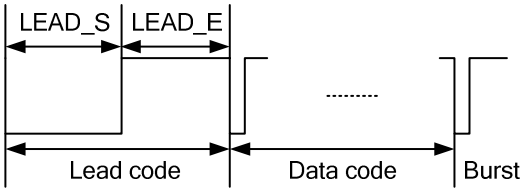


Figure 13-32 shows the format for transmitting consecutive TC9012 codes when C0 is 1.

Figure 13-32 Format for transmitting consecutive TC9012 codes (C0 = 1)

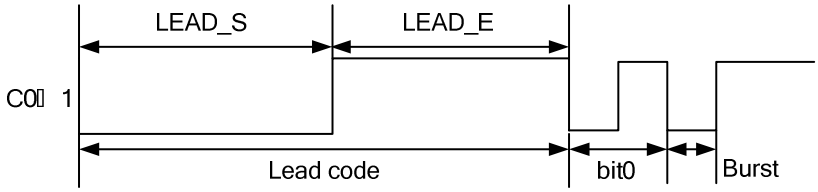
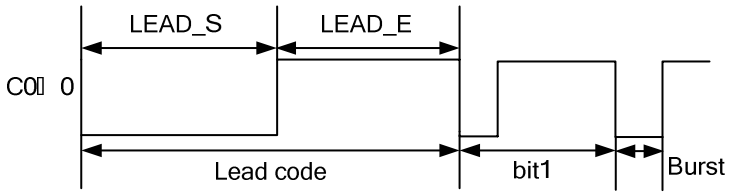


Figure 13-33 shows the format for transmitting consecutive TC9012 codes when C0 is 0.

Figure 13-33 Format for transmitting consecutiveTC9012 codes (C0 = 0)



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 13-5 to Table 13-7. In addition, the frame length must be less than or equal to 160 ms. Otherwise, the repeat frame cannot be identified.

13.4.3.4 SONY Code

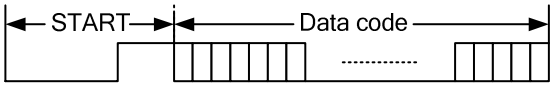
Frame Format

A SONY code consists of the following parts:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit are determined by the specific code pattern.

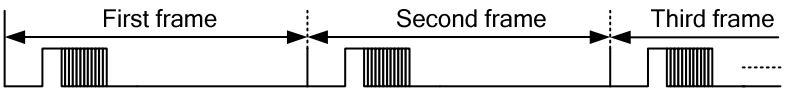
During reception, the LSB is received first. Figure 13-34 shows the frame format for transmitting a single SONY code.

Figure 13-34 Frame format for transmitting a single SONY code



When a complete data frame is received after the key is pressed for more than one frame length, the subsequently received data frame is also a complete data frame. Figure 13-35 shows the frame format for continuously transmitting SONY codes by pressing the key.

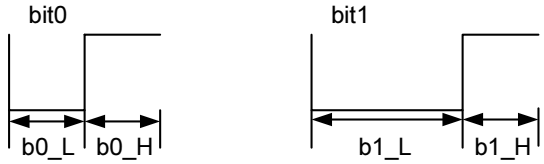
Figure 13-35 Frame format for continuously transmitting SONY codes by pressing the key



Code Format

Figure 13-36 shows the definitions of bit0 and bit1 of a SONY code.

Figure 13-36 Definitions of bit0 and bit1 of a SONY code



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 13-5 to Table 13-7.

13.4.4 Operating Mode

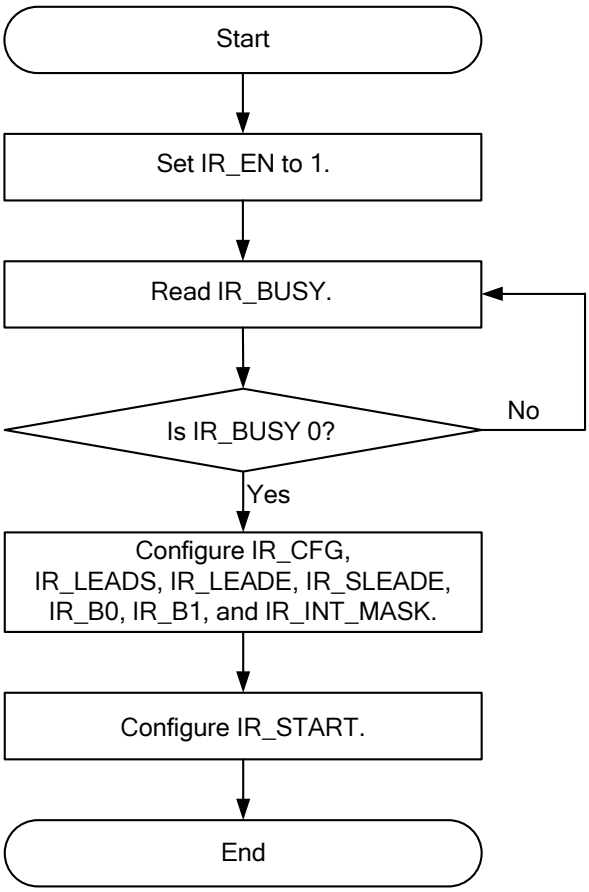
Soft Reset

When PERI_CRG33[4] is set to 1, the IR module is soft-reset separately. After reset, each configuration register is restored its default value. Therefore, these registers must be reinitialized.

Instances of Configuring Registers

Figure 13-37 shows the process of initializing the IR module.

Figure 13-37 Process of initializing the IR module



To initialize the IR module, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Set IR_EN[0] to 1 to enable the IR receive module.

Step 3 Read IR_BUSY to check the current status of the IR module.

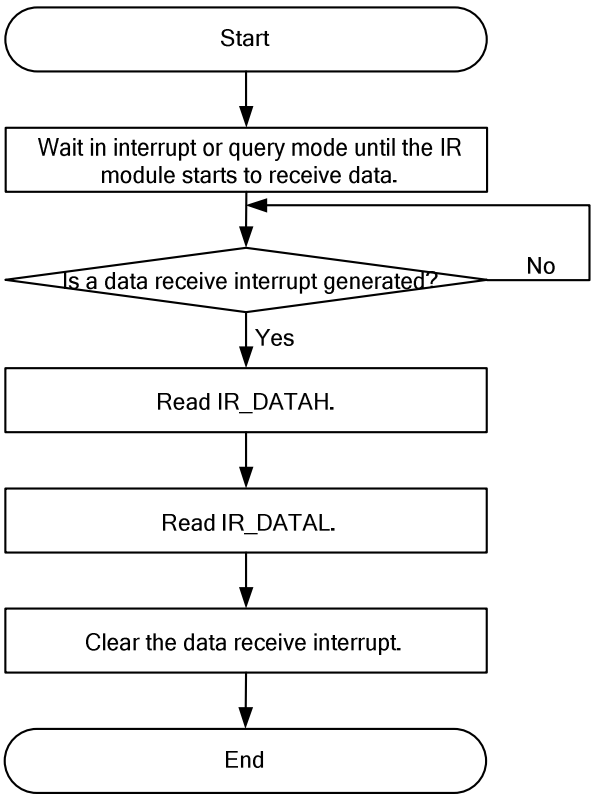
- If the value of IR_BUSY is 1, the IR module is busy. Then continue to read IR_BUSY. Note that configuring other control registers of the IR module by using software has no effect in this case.
- If the value of is 0, the IR module is idle. Then go to Step 4.

Step 4 Configure IR_CFG, IR_LEADS, IR_LEADE, IR_SLEADE, IR_B0, IR_B1, and IR_INT_MASK. Note: You can update corresponding registers as required. If the registers are not updated, the original values are retained.

Step 5 Configure IR_STARTafter all IR control registers are configured. This is because IR_START is used to generate the start signal. If IR_START is configured, the IR module starts to receive infrared data based on the values of IR control registers.

----End

Figure 13-38 Process of reading the decoded data



To read the decoded data, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Wait in interrupt or query mode until data frames are received.

- In interrupt mode, when the CPU receives an interrupt request signal from the IR module, read the value of IR_INT_STATUS[intms_rcv]. If the value is 1, the IR module receives a data frame. Then, go to Step 3. If the value is 0, repeat Step 2 to wait for an interrupt.
- In query mode, continuously read the value of IR_INT_STATUS[intrs_rcv] by using software or read the value at intervals. If the value is 1, the IR module receives a data frame. Then, go to Step 3. If the value is 0, the IR module does not receive any data frame. Then, repeat Step 2 to continue the query.

Step 3 Read IR_DATAH. If the number of data bits in one frame is less than or equal to 32, skip this step.

Step 4 Read IR_DATAL.

Step 5 Clear the data receive interrupt.

----End

13.4.5 Register Summary

Table 13-8 describes IR registers.

Table 13-8 Summary of IR registers (base address: 0x1214_0000)

Offset Address	Register	Description	Page
0x000	IR_EN	IR receive enable control register	13-77
0x004	IR_CFG	IR configuration register	13-77
0x008	IR_LEADS	Lead code start bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-79
0x00C	IR_LEADE	Lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-80
0x010	IR_SLEADE	Simple lead code end bit margin configuration register (valid when IR_CFG[ir_mode] is 0 only)	13-81
0x014	IR_B0	Data 0 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	13-82
0x018	IR_B1	Data 1 level judge margin configuration register (used only when IR_CFG[ir_mode] is 0)	13-83
0x01C	IR_BUSY	Configuration busy flag register	13-84
0x020	IR_DATAH	Upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)	13-85
0x024	IR_DATAL	Lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR received symbol width register (IR_CFG[ir_mode] = 1)	13-86
0x028	IR_INT_MASK	IR interrupt mask register	13-86
0x02C	IR_INT_STATUS	IR interrupt status register	13-88
0x030	IR_INT_CLR	IR interrupt clear register	13-90
0x034	IR_START	IR start configuration register	13-92

13.4.6 Register Description

IR_EN

IR_EN is an IR receive enable control register.

CAUTION

Before configuring other registers, you must set IR_EN[ir_en] to 1 by using software. When IR_EN[ir_en] is 0, other registers are read-only and the read values are their reset values.

Offset Address	Register Name	Total Reset Value
0x000	IR_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ir_en	IR receive module enable 0: disabled 1: enabled

IR_CFG

IR_CFG is an IR configuration register.

CAUTION

Before configuring this register, you must set
IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value is retained after configuration.

The reference clock frequency supported by the IR module ranges from 1 MHz to 128 MHz. The relationship between the frequency and the clock frequency divider ir_freq is as follows:

- When the reference clock frequency is 1 MHz, ir_freq must be set to 0x00.
- If the reference clock frequency is 128 MHz, ir_freq must be set to 0x7F.

When the frequency of the IR reference clock is not an integer ranging from 1 MHz to 128 MHz, the clock frequency divider is rounded off. For example, if the reference clock frequency is 12.1 MHz, the clock frequency divider is 0x0B; if the reference clock frequency is 12.8 MHz, the clock frequency divider is 0x0C.

The relationship between the frequency offset and the count deviation is as follows: If the base frequency is f and the frequency variation is D_f, the frequency offset ratio is D_f/f. If the count deviation of the counter is Dcnt, and the judge level width is s (in μs), the count deviation Dcnt is calculated as follows: Dcnt = |0.1 x s x ratio|Therefore, when the clock has frequency offset, the valid range of the parameter value needs to be changed. If the frequency increases, the corresponding margin range is changed to [min + Dcnt, max + Dcnt]. Where, min and max indicate the margins without frequency offset. If the frequency decreases, the offset range is changed to [min – Dcnt, max – Dcnt]. Take the margin of the start bit in the lead code as an example. If the base frequency is 100 MHz, and the frequency increases by 0.1 MHz, then the ratio is 0.001 (0.1/100). Assume that s is 9000 μs. Dcnt is calculated as follows: Dcnt = |0.1 x 9,000 x 0.001| = 1. In this case, the margin range of ir_leads must be changed to [0x033D, 0x3CD].

Offset Address	Register Name	Total Reset Value
0x004	IR_CFG	0x3E80_1F0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_max_level_width																ir_format				ir_bits				ir_mode				ir_freq			
Reset	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:16]	RW	ir_max_level_width	Invalid when IR_CFG[ir_mode] is 0 Indicates the maximum level width (in 10 μs) of a symbol whenIR_CFG[ir_mode] is 1. This width indicates the end of a symbol stream.
[15:14]	RW	ir_format	Data code format when IR_CFG[ir_mode] is 0 00: NEC with simple repeat code 01: TC9012 code 10: NEC with full repeat code 11: SONY code For details about the relationship between code types and code formats, see Table 13-5 to Table 13-7. Symbol format when IR_CFG[ir_mode] is 1 bit[15]: reserved The definitions of bit[14] are as follows: 0: The symbol is from low to high, and the symbol stream ends at the high level. 1: The symbol is from high to low, and the symbol stream ends at the low level.
[13:8]	RW	ir_bits	Number of data bits in a frame when IR_CFG[ir_mode] is 0 0x00–0x2F: 1–48 data bits in a frame 0x30–0x3F: reserved If ir_bits is set to a value ranging from 0x30 to 0x3F by using

			software, the setting has no effect and the original value is retained. Symbol receive interrupt threshold when IR_CFG[ir_mode] is 1 bit[13]: reserved bit[12:8]: 0x0–0x1F. 0x0 indicates that an interrupt is reported when there is at least one symbol in the FIFO; 0x1F indicates that an interrupt is reported when there are at least 32 symbols in the FIFO, and so on.
[7]	RW	ir_mode	IR operating mode 0: The decoded complete data frames are output. 1: Only the symbol width is output.
[6:0]	RW	ir_freq	Frequency divider of the working clock 0x00–0x7F: correspond to the working clock divider 1–128 respectively.

IR_LEADS

IR_LEADS is a lead code start bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set Register Description[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.

The margin must be considered based on the typical value of the specific code type for accurately judging the start bit of the lead code. For details about the typical values of specified code types, see the values of LEAD_S in Table 13-5 to Table 13-7.

- For a pulse width whose typical value is greater than or equal to 400 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_S is 900, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 900 x 92% = 828 = 0x33C cnt_leads_max = 900 x 108% = 972 = 0x3CC
- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 as an example. If the typical value of LEAD_S is 240, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 240 x 80% = 192 = 0xC0 cnt_leads_max = 240 x 120% = 288 = 0x120

The basic configuration principle is as follows: cnt_leads_max is greater than or equal to cnt_leads_min, and cnt_leads_min is greater than cnt0_b_max and cnt1_b_max.

Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								cnt_leads_min								reserved								cnt_leads_max							
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	cnt_leads_min	Minimum pulse width of the start bit of the lead code 0x000–0x007: reserved
[15:10]	RO	reserved	Reserved
[9:0]	RW	cnt_leads_max	Maximum pulse width of the start bit of the lead code 0x000–0x007: reserved

IR_LEADE

IR_LEADE is a lead code end bit margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the lead code. The margin is about 8% of the type value. For details about the typical values of specific code types, see the values of LEAD_E in Table 13-5 to Table 13-7.

- For the pulse width whose typical values is greater than or equal to 400 (10 µs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_E is 450, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

  cnt_leade_min = 450 x 92% = 414 = 0x19E cnt_leade_max = 450 x 108% = 486 = 0x1E6
- For a pulse width whose typical value is less than 400 (10 µs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 code as an example. If the typical value of LEAD_E is 60, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

cnt_leade_min = 60 x 80% = 48 = 0x030 cnt_leade_max = 60 x 120% = 72 = 0x048

The basic configuration principle is as follows: cnt_leade_max is greater than or equal to cnt_leade_min.

Offset Address	Register Name	Total Reset Value
0x00C	IR_LEADE	0x019E_01E6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_leade_min								reserved								cnt_leade_max							
Reset	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt_leade_min	Minimum pulse width of the end bit of the lead code 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt_leade_max	Maximum pulse width of the end bit of the lead code 0x000–0x007: reserved

IR_SLEADE

IR_SLEADE is a simple lead code end bit margin configuration register (IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.
- This register must be configured only for the NEC with simple repeat code.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the simple lead code. For details about the typical values of specific code types, see the values of SLEAD_E in Table 13-5 to Table 13-7.

- For a pulse width whose typical value is greater than or equal to 225 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of SLEAD_E is 225, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:

  cnt_sleade_min = 225 x 92% = 207 = 0xCF cnt_sleade_max = 225 x 108% = 243 = 0xF3

- For a pulse width whose typical value is less than 225 (10 µs precision), the recommended margin is 20% of the typical value. For example, if the typical value of SLEAD_E of a code type is 60, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:

  cnt_sleade_min = 60 x 80% = 48 = 0x30 cnt_sleade_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt_sleade_max is greater than or equal to cnt_sleade_min.

Offset Address	Register Name	Total Reset Value
0x010	IR_SLEADE	0x00CF_00F3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_sleade_min								reserved								cnt_sleade_max							
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt_sleade_min	Minimum pulse width of the end bit of the simple lead code 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt_sleade_max	Maximum pulse width of the start bit of the simple lead code 0x000–0x007: reserved

IR_B0

IR_B0 is data 0 level judge margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[ir_busy] to 0 and set IR_EN[ir_en] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type to accurately judging bit0. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with full repeat code, NEC with simple repeat code, and TC9012 code, see the values of B0_H in Table 13-5 to Table 13-7. Take the D6121 code as an example. If the typical value of B0_H is 56 (10 µs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

cnt0_b_min = 56 x 80% = 45 = 0x2D cnt0_b_max = 56 x 120% = 67 = 0x43

- For details about the typical value of the SONY code, see the values of B0_L in Table 13-5 to Table 13-7. Take the SONY-D7C5 code as an example. If the typical value of B0_L is 60 (10 μs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 60 x 80% = 48 = 0x30 cnt0_b_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt0_b_max is greater than or equal to cnt0_b_min.

Offset Address	Register Name	Total Reset Value
0x014	IR_B0	0x002D_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt0_b_min								reserved								cnt0_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt0_b_min	Minimum pulse width of the level for judging bit0 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt0_b_max	Maximum pulse width of the level for judging bit0 0x000–0x007: reserved

IR_B1

IR_B1 is data 1 judge level margin configuration register (valid only when IR_CFG[ir_mode] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[0] to 0 and set IR_EN[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type for accurately judging bit1. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with simple repeat code, NEC with simple repeat code, and TC9012 code, see the values of B1_H in Table 13-5 to Table

13-7. Take the D6121 code as an example. If the typical value of B1_H is 169 (10 μs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

cnt1_b_min = 169 x 80% = 135 = 0x87 cnt1_b_max = 169 x 120% = 203 = 0xCB

- For details about the typical value of the SONY code, see the values of B1_L in Table 13-5 to Table 13-7. Take the SONY-D7C5 code as an example. If the typical value of B1_L is 120 (10 μs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 120 x 80% = 96 = 0x60 cnt1_b_max = 120 x 120% = 144 = 0x90

The basic configuration principle is as follows: cnt1_b_max is greater than or equal to cnt1_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt1_b_min								reserved								cnt1_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt1_b_min	Minimum pulse width of the level for judging bit1 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt1_b_max	Maximum pulse width of the level for judging bit1 0x000–0x007: reserved

IR_BUSY

IR_BUSY is a configuration busy flag register.

Offset Address	Register Name	Total Reset Value
0x01C	IR_BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RO	ir_busy	Busy status flag 0: idle. In this case, software can configure data. 1: Indicates the busy state. In this state, software cannot configure data.

IR_DATAH

IR_DATAH is an upper 16-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or symbol count register in the symbol FIFO (IR_CFG[ir_mode] = 1)

The IR_DATAH register stores the upper 16 bits of the decoded data received by the IR, whereas IR_DATAL stores the lower 32 bits of the decoded data received by the IR. The data bits depend on the valid data bits in a frame and the specific code. For details, see the valid data bits in Table 13-5 to Table 13-7.

Data is stored as follows: The data is stored in IR_DATAH and IR_DATAL in sequence from MSB to LSB. That is, after IR_DATAL is full, the remaining data is stored in IR_DATAH. The unused upper bits are reserved. Data is read as follows: IR_DATAH and IR_DATAL are read in sequence.

The hardware receives all data bits without checking the definition of each data bit. The software is responsible for processing data bits.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ir_datah															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	ir_datah	Upper 16 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0 Symbol count in the symbol FIFO when IR_CFG[ir_mode] is 1 bit[15:6]: reserved bit[5:0]: number of symbols in the symbol FIFO

IR_DATAL

IR_DATAL is a lower 32-bit IR receive decoded data register (IR_CFG[ir_mode] = 0) or IR receive symbol width register (IR_CFG[ir_mode] = 1).

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_datal																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ir_datal	Lower 32 bits of the decoded data received by the IR module when IR_CFG[ir_mode] is 0 Width of the symbol received by the IR module when IR_CFG[ir_mode] is 1 The definitions of bit[31:16] are as follows: Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR when the symbol level is from low to high. Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low. The definitions of bit[15:0] are as follows: Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from low to high. Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low.

IR_INT_MASK

IR_INT_MASK is an IR interrupt mask register.

CAUTION

- Before setting this register, you must set IR_EN[ir_en] to 1. Otherwise, the original value of the register is retained after setting.
- If all interrupts are masked, the IR wake-up function is unavailable.
- When IR_CFG[ir_mode] is 0, IR_INT_MASK[3:0] are valid; when IR_CFG[ir_mode] is 1, IR_INT_MASK[18:16] are valid.

The definitions of the interrupts related to the register are as follows:

- RX data overflow interrupt

If the CPU does not fetch the current frame and the next frame is already received, the next frame overwrites the current frame and a raw RX data overflow error interrupt is reported.

- RX data frame format error interrupt

  If the received data frame is not complete or the data pulse width does not meet the margin requirements, a raw RX frame format error interrupt is reported.

- RX data frame interrupt

  After a complete frame data is received, a raw RX data frame interrupt is reported.

- Key release detection interrupt

  For the NEC with simple repeat code and TC9012 code, if the start synchronous code is not detected again within 160 ms after the previously detected start synchronous code, or a valid data frame rather than a simple lead code is detected, a raw key release detection interrupt is reported. Both the NEC with full repeat code and the SONY code do not support the key release detection interrupt.

- RX symbol overflow interrupt

  If the symbol FIFO is full because the CPU does not fetch the data in time and the subsequent symbol is already received, a raw RX symbol overflow error interrupt is reported.

- RX symbol interrupt

  If a complete symbol is received and the symbol count of the symbol FIFO is above the threshold configured by IR_CFG[ir_bits], a raw RX symbol interrupt is reported.

- Symbol timeout interrupt

  If no new symbol interrupt is received during the period configured by IR_CFG[ir_max_level_width] after a valid symbol is received, a raw symbol timeout interrupt is reported.

The hardware does not identify the interrupt priority. An interrupt is generated if one or more masked interrupt sources are valid.

Offset Address	Register Name	Total Reset Value
0x028	IR_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intm_overrun	intm_time_out	intm_symb_rcv	reserved												intm_release	intm_overflow	intm_frame_error	intm_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	intm_overrun	Symbol overflow interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked

[17]	RW	intm_time_out	Symbol timeout interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked
[16]	RW	intm_symb_rcv	RX N symbol interrupt mask when IR_CFG[ir_mode] is 1 0: not masked 1: masked
[15:4]	-	reserved	Reserved
[3]	RW	intm_release	Key release interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[2]	RW	intm_overflow	RX data overflow interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[1]	RW	intm_frame_error	RX data frame format error interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked
[0]	RW	intm_rcv	RX data frame interrupt mask when IR_CFG[ir_mode] is 0 0: not masked 1: masked

IR_INT_STATUS

IR_INT_STATUS is an IR interrupt status register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_STATUS[3:0] and IR_INT_STATUS[19:16] are valid.
- When IR_CFG[ir_mode] is 1, IR_INT_STATUS[10:8] and IR_INT_STATUS[26:24] are valid.

Offset Address	Register Name	Total Reset Value
0x02C	IR_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved					intms_overrun	intms_time_out	intms_symb_rcv	reserved				intms_release	intms_overflow	intms_frame_error	intms_rcv	reserved				intrs_overrun	intrs_time_out	intrs_symb_rcv		reserved				intrs_release	intrs_overflow	intrs_frame_error	intrs_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RO	intms_overrun	Masked symbol overflow interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RO	intms_time_out	Masked symbol timeout interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RO	intms_symb_rcv	Masked RX symbol interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[23:20]	RO	reserved	Reserved
[19]	RO	intms_release	Masked key release interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	intms_overflow	Masked RX data overflow error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	intms_frame_error	Masked RX data frame format error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	intms_rcv	Masked RX data frame interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[15:11]	RO	reserved	Reserved

[10]	RO	intrs_overrun	Raw symbol overflow interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	intrs_time_out	Raw symbol timeout interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	intrs_symb_rcv	Raw RX symbol interrupt status when IR_CFG[ir_mode] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[7:4]	RO	reserved	Reserved
[3]	RO	intrs_release	Raw key release interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	intrs_overflow	Raw RX data overflow error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	intrs_frame_error	Raw RX data frame format error interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	intrs_rcv	Raw RX data frame interrupt status when IR_CFG[ir_mode] is 0 0: No interrupt is generated. 1: An interrupt is generated.

IR_INT_CLR

IR_INT_CLR is an IR interrupt clear register.

CAUTION

- When IR_CFG[ir_mode] is 0, IR_INT_CLR[3:0] are valid.
- When IR_CFG[ir_mode] is 1, IR_INT_CLR[18:16] are valid.

Offset Address	Register Name	Total Reset Value
0x030	IR_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intc_overrun	intc_time_out	intc_symb_rcv	reserved												intc_release	intc_overflow	intc_frame_error	intc_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	WC	intc_overrun	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol overflow interrupt request is cleared. 0: no effect 1: cleared
[17]	WC	intc_time_out	When IR_CFG[ir_mode] is 1, this bit indicates whether the symbol timeout interrupt request is cleared. 0: no effect 1: cleared
[16]	WC	intc_symb_rcv	When IR_CFG[ir_mode] is 1, this bit indicates whether the RX symbol interrupt request is cleared. 0: no effect 1: cleared
[15:4]	RO	reserved	Reserved
[3]	WC	intc_release	When IR_CFG[ir_mode] is 0, this bit indicates whether the key release interrupt request is cleared. 0: no effect 1: cleared
[2]	WC	intc_overflow	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data overflow error interrupt request is cleared. 0: no effect 1: cleared
[1]	WC	intc_frame_error	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data frame format error interrupt request is cleared. 0: no effect 1: cleared

[0]	WC	intc_rcv	When IR_CFG[ir_mode] is 0, this bit indicates whether the RX data frame interrupt request is cleared. 0: no effect 1: cleared If an RX data frame interrupt is generated and the software writes 1 to the bit without reading the data in IR_DATAL, the interrupt cannot be cleared.

IR_START

IR_START is an IR start configuration register.

After other registers are configured, IR_START can be started when any value is written to the corresponding address during the startup of the IR module.

Offset Address	Register Name	Total Reset Value
0x034	IR_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	ir_start	IR start configuration register

13.5 GPIO

13.5.1 Overview

The Hi3521A supports 14 groups of general purpose input/output (GPIO) pins, that is, GPIO0 to GPIO13. Each group of GPIO pins provides eight programmable input/output pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes. As input, each GPIO pin can act as an interrupt source; as output, each GPIO pin can be set to 0 or 1 separately.

The GPIO can generate maskable interrupts based on the level or transition value. The general purpose input output interrupt (GPIOINTR) signal provides an indicator to the interrupt controller, indicating that an interrupt occurs.

CAUTION

- For details about the number of GPIO pins and multiplexing relationship between GPIO pins and other pins, see chapter 2 "Hardware." For details about control modes, see section 2.3 "Pin Multiplexing Registers."
- For the multiplexed GPIO pins that are output by default, note that the pins that connect to the chip and the components must be input.
- The Hi3520D V300 does not supports partial pins, for details about the GPIO pins and multiplexing relationship between GPIO pins and other pins, see chapter 2 "Hardware."

13.5.2 Features

Each GPIO pin can be configured as input or output.

- As input, each GPIO pin can act as an interrupt source.
- As output, each GPIO can be set to 0 or 1 separately.

13.5.3 Operating Mode

Interface Reset

The GPIO is reset during chip power-on reset or system reset, and GPIO pins are in input state after being reset.

GPIO

Each pin can be configured as input or output. To configure a GPIO pin, perform the following steps:

Step 1 Enable the required GPIO pins by configuring corresponding pins according to the description of multiplexing registers.

Step 2 Configure the GPIO as input or output by using the GPIO_DIR register.

Step 3 When the GPIO pins are in input mode, read the GPIO_DATA register to check the input signal value. When the GPIO pins are in output mode, write the output value to the GPIO_DATA register to control the output level of the GPIO pins.

----End

CAUTION

When the GPIO pins are in output mode, do not enable the GPIO interrupt. Otherwise, the GPIO interrupt will be generated when output signals meet interrupt generation conditions.

Interrupt Operation

The GPIO interrupt is controlled through seven registers (such as GPIO_IS). These registers enable you to select the interrupt source, interrupt edge (falling edge or rising edge), and interrupt trigger modes (level-sensitive mode or edge-sensitive mode). For details about the corresponding interrupt registers of the GPIO, see section 3.4 "Interrupt Systems."

When multiple interrupts are generated at the same time, these interrupts are combined into an interrupt and then reported. For details about the GPIO interrupt mapping, see section 3.3 "Interrupt Systems."

The

GPIO_IS, GPIO_IBE, and GPIO_IEV registers determine the features of the interrupt source and interrupt trigger type.

GPIO_RIS and GPIO_MIS are used to read the raw interrupt status and masked interrupt status, respectively. GPIO_IEV controls the final report status of each interrupt. In addition, GPIO_IC is provided to clear the interrupt status.

Perform the following operations to configure GPIO pins to the interrupt mode:

Step 1 Select the edge-sensitive mode or level-sensitive mode by configuring the

Step 2 GPIO_IS register.

Step 3 Select the falling-/rising-edge-sensitive mode or high-/low-level-sensitive mode by configuring the GPIO_IEV register.

Step 4 If the edge-sensitive mode is selected, select single-edge-sensitive mode or dual-edge-sensitive mode by configuring the GPIO_IBE register.

Step 5 Write 0xFF to the GPIO_IC register to clear the interrupt.

Step 6 Set the GPIO_IE to 1 to enable the interrupt.

----End

CAUTION

Ensure that data in GPIO pins is stable during initialization to prevent pseudo interrupts.

The GPIO interrupts are controlled by seven registers. When one or more GPIO pins generate interrupts, a combined interrupt is output to the interrupt controller. The differences between the edge-sensitive mode and level-sensitive mode are as follows:

- Edge-sensitive mode: Software must clear this interrupt to enable superior interrupts.
- Level-sensitive mode: The external interrupt source must keep this level until the processor identifies this interrupt.

13.5.4 Register Summary

Table 13-9 lists the base addresses for 14 groups of GPIO registers.

Table 13-9 Base addresses for 14 groups of GPIO registers

Register	Base Address
GPIO13	0x1222_0000
GPIO12	0x1221_0000
GPIO11	0x1220_0000
GPIO10	0x121F_0000
GPIO9	0x121E_0000
GPIO8	0x121D_0000
GPIO7	0x121C_0000
GPIO6	0x121B_0000
GPIO5	0x121A_0000
GPIO4	0x1219_0000
GPIO3	0x1218_0000
GPIO2	0x1217_0000
GPIO1	0x1216_0000
GPIO0	0x1215_0000

Table 13-10 describes the offset addresses and definitions of a group of internal GPIO registers. GPIO0 to GPIO13 also have the same internal GPIO registers.

NOTE

- Register address of GPIOn = GPIOn base address + Offset address of the register
- The value of n ranges from 0 to 13.

Table 13-10 Summary of GPIO registers

Offset Address	Register	Description	Page
0x000–0x3FC	GPIO_DATA	GPIO data register	13-96
0x400	GPIO_DIR	GPIO direction control register	13-97
0x404	GPIO_IS	GPIO interrupt trigger register	13-97
0x408	GPIO_IBE	GPIO interrupt dual-edge trigger register	13-97
0x40C	GPIO_IEV	GPIO interrupt trigger event register	13-98
0x410	GPIO_IE	GPIO interrupt mask register	13-98
0x414	GPIO_RIS	GPIO raw interrupt status register	13-99
0x418	GPIO_MIS	GPIO masked interrupt status register	13-99

Offset Address	Register	Description	Page
0x41C	GPIO_IC	GPIO interrupt clear register	13-100

13.5.5 Register Description

GPIO_DATA

GPIO_DATA is a GPIO data register. It is used to buffer the input or output data.

When the corresponding bit of the GPIO_DIR is configured as output, the values written to the GPIO_DATA register are sent to the corresponding pin (note that the pin multiplexing configuration must be correct). If the bit is configured as input, the value of the corresponding input pin is read.

CAUTION

If the corresponding bit of GPIO_DIR is configured as input, the pin value is returned after a valid read; if the corresponding bit is configured as output, the written value is returned after a valid read.

Through PADDR[9:2], the GPIO_DATA register masks the read and write operations on the register. The register corresponds to 256 address spaces. PADDR[9:2] corresponds to GPIO_DATA[7:0]. When the corresponding bit is high, it can be read or written. When the corresponding bit is low, no operations are supported. For example:

- If the address is 0x3FC (0b11_1111_1100), the operations on all the eight bits of GPIO_DATA[7:0] are valid.
- If the address is 0x200 (0b10_0000_0000), only the operation on GPIO_DATA[7] is valid.

Offset Address	Register Name	Total Reset Value
0x000–0x3FC	GPIO_DATA	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_data							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_data	Indicates the GPIO input data when the GPIO is configured as input; indicates the GPIO output data when the GPIO is configured as output. Each bit can be controlled separately. The register is used together with GPIO_DIR.

GPIO_DIR

GPIO_DIR is a GPIO direction control register. It is used to configure the direction of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x400	GPIO_DIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_dir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_dir	GPIO direction control register. Bit[7:0] correspond to GPIO_DATA[7:0] respectively. Each bit can be controlled separately. 0: input 1: output

GPIO_IS

GPIO_IS is a GPIO interrupt trigger register. It is used to configure the interrupt trigger mode.

Offset Address	Register Name	Total Reset Value
0x404	GPIO_IS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_is							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_is	GPIO interrupt trigger control register. Bit[7:0] correspond to GPIO_DATA[7:0]. Each bit is controlled separately. 0: edge-sensitive mode 1: level-sensitive mode

GPIO_IBE

GPIO_IBE is a GPIO interrupt dual-edge trigger register. It is used to configure the edge trigger mode of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x408	GPIO_IBE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ibe							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ibe	GPIO interrupt edge control register. Bit[7:0] correspond to GPIO_DATA[7:0] respectively. Each bit is controlled independently. 0: single-edge-sensitive mode. The GPIO_IEV register controls whether the interrupt is rising-edge-sensitive or falling-edge-sensitive. 1: dual-edge-sensitive mode

GPIO_IEV

GPIO_IEV is a GPIO interrupt event register. It is used to configure the interrupt trigger event of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x40C	GPIO_IEV	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_iev							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_iev	GPIO interrupt trigger event register. Bit[7:0] correspond to GPIO_DATA[7:0]. Each bit is controlled separately. 0: falling-edge-sensitive mode or low-level-sensitive mode 1: rising-edge-sensitive mode or high-level-sensitive mode.

GPIO_IE

GPIO_IE is a GPIO interrupt mask register. It is used to mask GPIO interrupts.

Offset Address	Register Name	Total Reset Value
0x410	GPIO_IE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ie							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ie	GPIO interrupt mask register. Bit[7:0] correspond to GPIO_DATA[7:0]. Each bit is controlled separately. 0: masked 1: not masked

GPIO_RIS

GPIO_RIS is a GPIO raw interrupt status register. It is used to query the raw interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x414	GPIO_RIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ris							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_ris	GPIO raw interrupt status register. Bit[7:0] correspond to GPIO_DATA[7:0], indicating the unmasked interrupt status. The status cannot be masked and controlled by the GPIO_IE register. 0: No interrupt occurs. 1: An interrupt is generated.

GPIO_MIS

GPIO_MIS is a GPIO masked interrupt status register. It is used to query the masked interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x418	GPIO_MIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_mis							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_mis	GPIO masked interrupt status register. Bit[7:0] correspond to GPIO_DATA[7:0], indicating the masked interrupt status. The status is controlled by the GPIO_IE register. 0: The interrupt is invalid.

			1: The interrupt is valid.

GPIO_IC

GPIO_IC is a GPIO interrupt clear register. It is used to clear the interrupts generated by GPIO pins and clear the GPIO_RIS and GPIO_MIS registers.

Offset Address	Register Name	Total Reset Value
0x41C	GPIO_IC	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ic							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	WC	gpio_ic	GPIO interrupt clear register. Bit[7:0] correspond to GPIO_DATA[7:0]. Each bit is controlled separately. 0: no effect 1: cleared

13.6 SATA

13.6.1 Overview

The serial advanced technology attachment (SATA) module provides advanced microcontroller bus architecture (AMBA) 3.0 advanced eXtensible interfaces (AXIs). The interfaces are used to implement rapid integration on the system-on-chip (SoC) system. With the drivers developed on Linux, the SATA ports help software engineers rapidly customize and develop the drivers of the SoC subsystem. The Hi3521A provides two SATA ports (32 interfaces supported according to the SATA protocol) and supports new SATA features such as the native command queuing (NCQ), hot-plugging, port multiplier (PM), frame information structure-based switching (FBS), eSATA, and power supply management.

13.6.2 Features

The SATA module has the following features:

- Provides the ARM AHB system bus interface that supports slave operations, complies with AMBA Spec 2.0, and supports only the 32-bit access mode.
- Provides the ARM AXI system bus interface that supports master operations, complies with AMBA Spec 3.0, and supports only the 128-bit access mode.
- Provides a standard interface signal for connecting to the PHY.
- Supports SATA 3.0 and AHCI 1.3 protocols as well as SATA 2.6 and AHCI 1.2 protocols .
- Supports programmable input/output (PIO), legacy DMA, and NCQ operations.

- Supports power supply management.
- Supports PMs and FBS.
- Provides two SATA ports.
- Supports automatic rate negotiation among 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s .
- Supports the error interrupt report mechanism.

CAUTION

Hi3520D V300 Supports SATA 2.6 and AHCI 1.2 protocols

Hi3520D V300 Supports automatic rate negotiation among 1.5 Gbit/s and 3 Gbit/s

13.6.3 Signal Description

Table 13-11 describes the SATA port signals.

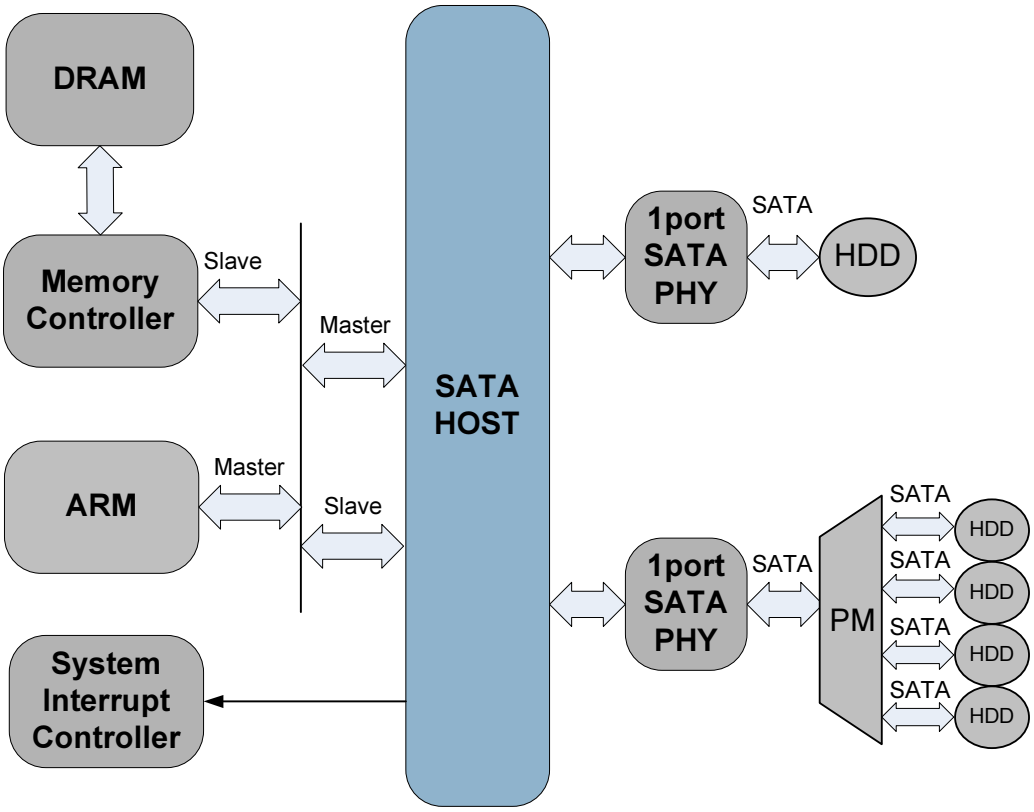
Table 13-11 SATA port signals

Signal	Direction	Description	Corresponding Pin
Rx0_m	I	Negative terminal of the RX differential signal of SATA port 0	SATA_RXM0
Rx0_p	I	Positive terminal of the RX differential signal of SATA port 0	SATA_RXP0
Tx0_m	O	Negative terminal of the TX differential signal of SATA port 0	SATA_TXM0
Tx0_p	O	Positive terminal of the TX differential signal of SATA port 0	SATA_TXP0
Rx1_m	I	Negative terminal of the RX differential signal of SATA port 1	SATA_RXM1
Rx1_p	I	Positive terminal of the RX differential signal of SATA port 1	SATA_RXP1
Tx1_m	O	Negative terminal of the TX differential signal of SATA port 1	SATA_TXM1
Tx1_p	O	Positive terminal of the TX differential signal of SATA port 1	SATA_TXP1
Resref	I/O	SATA extended resistor pin, connected to external extended resistors	SATA_REXT

13.6.4 Function Description

Figure 13-39 shows the application scenario of the SATA host.

Figure 13-39 Application block diagram of the SATA host



The AXI master interface is mounted on the ARM AMBA 3.0-based system bus AXI, and the AHB slave interface is mounted on the ARM AMBA 2.0-based AHB. Software configures the SATA host over the AHB slave interface. The AXI master interface can proactively access the DRAM controlled by the system memory controller to read commands or read and write data.

The interrupt signal connects to the system interrupt controller.

In the Hi3521A, the SATA PHY port connects to SATA host. Outside the Hi3535, the SATA PHY can connect to the SATA hard disk, flash drive, or SATA PM for extending ports.

The LED activity display signal can be directly transferred from the chip, which can be selected based on the actual scenario.

This design supports AHCI-complied drivers on various operating systems.

13.6.5 Operating Mode

13.6.5.1 Pin Multiplexing Configuration

The LED logic control sata_led_n_X (X = 0−1) is multiplexed with a GPIO pin. Each port has a control signal. For details, see section 13.5 "GPIO."

13.6.5.2 Clock Gating

Clock gating is implemented in the CRG module. For details, see the descriptions of CRG in section 3.2 "Clock."

13.6.5.3 Clock Configuration

The reference clocks with different frequencies can be provided for the SATA PHY 1, and SATA PHY 0 by configuring PERI_CRG26[3] and PERI_CRG26[1] respectively. When the provided reference clocks change, you need to configure the internal control registers of the SATA host (SATA_PHY1_CTLL[8:1] and SATA_PHY0_CTLL[8:1]) to meet the clock requirements of the MPLL in the PHY. For details, see section 13.6.7 "Register Description."

13.6.5.4 Soft Reset

The SATA host controller provides two sync rest policies that can be used to reset the controller and a port respectively.

- When SATA_GHC_GHC bit[0] of the SATA host controller is set to 1, the controller enters the rest state, and the logic of all internal modules is restored to initial value. After reset, SATA_GHC_GHC bit[0] is automatically cleared.
- When SATA_PORT_CMD bit[0] of port 0 or port 1 is changed from 1 to 0, port 0 or port 1 enters the reset state.

13.6.5.5 Operating Mode Configuration

Before starting the SATA host, you must initialize the SATA PHY and perform initial negotiation between the SATA host and the SATA device.

Initializing the PHY

The following describes how to initialize the SATA PHY by using the 100 MHz internal PHY reference clock and 3 Gbit/s port 0 as an example:

Step 1 Set PERI_CRG26 bit[1:0] to 01 to select and enable the 100 MHz reference clock from the CRG module.

Step 2 Set muxctrl_reg97 bit[0] to 1 to enable SATA_LED_N0.

Step 3 Set SATA_PORT_PHYCTL to 0x0E39_0000 to select the 3 Gbit/s port rate.

Step 4 Set SATA_PHY0_CTLL to 0x4900_003D to reset the SATA PHY.

Step 5 Set SATA_PORT_PHYCTL2 to x0006_0555 to reset lane 0 of the SATA PHY.

Step 6 Set SATA_PHY0_CTLL to 0x4900_023D to configure the SATA PHY clock.

Step 7 Set SATA_PORT_PHYCTL2 to 0x0002_0555 to deassert soft reset on the clock domain of lane 0 of the SATA PHY.

Step 8 Set SATA_PHY0_CTLL to 0x4980_023C to deassert reset on the SATA PHY.

Step 9 Set SATA_PHY0_CTLH bit[3] to 1, ensuring that the endian modes of the PHY and parallel data interface connected to the SATA controller are opposite.

----End

Initialization Negotiation

After the PLL of the SATA PHY works properly, initialization negotiation is performed between the SATA host and SATA device as follows:

Step 1 Set SATA_PORT_CMD[cmd_sud] to 1.

Step 2 Wait until the indicator signal phyrdy from the SATA PHY is valid and check whether SATA_PORT_SSTS[pxssts_det] is 3. If SATA_PORT_SSTS[pxssts_det] is 3, the corresponding port works properly and initialization is successful.

---End

Running Services

After initialization negotiation, start services as follows by using the DMA mode as an example:

Step 1 Clear interrupts (skip this step after reset or if services are started initially). To be specific, set the values of SATA_PORT_SERR, SATA_PORT_IS, and SATA_GHC_IS to 0xFFFFFFFF.

Step 2 Configure the interrupt mask register SATA_PORT_IE to mask the interrupts that do not need to be reported.

Step 3 Enable the global interrupt by setting SATA_GHC_GHC to 0x80000002.

Step 4 Set up a linked list based on SATA command linked list format of the appendix A.

Step 5 Set the base address for the port command lists in the memory by configuring SATA_PORT_CLB[port_clb] and notify the TX DMAC of the position for storing the commands and data to be read. The configured base address is the memory base address allocated for the port command lists.

Step 6 Set the base address in the memory for storing the frames received through the port by configuring SATA_PORT_FB[port_fb] and notify the RX DMAC of the position for storing the received frame information structures (FISs). The configured base address is the memory base address allocated for the port receive frames.

Step 7 Set SATA_PORT_CMD to 0x0020_0015 to enable the TX and RX DMACs to transmit commands and data and receive FISs and write them to the memory.

Step 8 Configure the port command TX control register SATA_PORT_CI to specify the command to be transmitted.

Step 9 Transmit the commands and data.

Step 10 Check whether the current command is complete through the interrupt bit and command execution status. When interrupts are received, check whether all the CI bits are cleared for the PIO or DMA operation and check the CI and SACT bits are cleared for the NCQ operation.

Step 11 Repeat Step 1 to Step 10 for the next transfer if necessary.

---End

NOTE

- Perform the operations of legacy DMA, PIO, and ATAPI according to the preceding steps. The linked lists (such as the command codes and flag bits), however, are different for theses operations.

- For the NCQ operation, besides a different linked list, SATA_PORT_SACT also needs to be configured to indicate the number of executed commands during the NCQ operation. To be specific, configure SATA_PORT_SACT after step 7, and ensure that the position of the commands configured by SATA_PORT_SACT map to those of the commands in SATA_PORT_CI.

13.6.6 Register Summary

SATA Registers

Table 13-12 describes SATA registers.

Table 13-12 Summary of SATA registers (base address: 0x1101_0000)

Offset Address	Register	Description	Page
0x0000	SATA_GHC_CAP1	Feature support register 1	13-108
0x0004	SATA_GHC_GHC	Global Control Registers	13-109
0x0008	SATA_GHC_IS	Interrupt status register	13-109
0x000C	SATA_GHC_PI	Port implementation register	13-110
0x0010	SATA_GHC_VS	AHCI version identifier register	13-111
0x0014	SATA_GHC_CCC_CTL	Command completion coalescing (CCC) control register	13-111
0x0018	SATA_GHC_CCC_PORTS	CCC port enable register	13-112
0x0024	SATA_GHC_CAP2	Feature support register 2	13-112
0x0028	SATA_GHC_BOHC	Basic input/output system (BIOS)/operating system (OS) handoff control register	13-113
0x00A0	SATA_PHY0_CTLL	Lower-bit PHY 0 global control register	13-114
0x00A4	SATA_PHY0_CTLH	Upper-bit PHY 0 global control register	13-115
0x00A8	SATA_PHY0_STS	PHY 0 global status register	13-116
0x00AC	SATA_PHY1_CTLL	Lower-bit PHY 1 global control register	13-116
0x00B0	SATA_PHY1_CTLH	Upper-bit PHY 1 global control register	13-117
0x00B4	SATA_PHY1_STS	PHY 1 global status register	13-118
0x00B8	SATA_OOB_CTL	PHY out of band (OOB) control register	13-118
0x00BC	SATA_AXI_DFX0	SATA AXI bus control register	13-119
0x00C0	SATA_AXI_DFX1	SATA AXI bus status register 1	13-121
0x00C4	SATA_AXI_DFX2	SATA AXI bus status register 2	13-121
0x00C8	SATA_AXI_DFX3	SATA AXI bus status register 3	13-122

Offset Address	Register	Description	Page
0x00CC	SATA_AXI_DFX4	SATA AXI bus status register 4	13-122
0x00D0	SATA_AXI_DFX5	SATA AXI bus status register 5	13-122
0x00D8	SATA_AXI_DFX7	SATA AXI bus status register 7	13-123
0x00E0	SATA_AXI_DFX9	SATA AXI bus status register 9	13-124
0x00E8	SATA_AXI_DFX11	SATA AXI bus status register 11	13-124

SATA Port Configuration Registers

NOTE

The variable *n* in the offset addresses indicate the port ID and range from 0 to 1.

Table 13-13 describes the SATA port configuration registers.

Table 13-13 Summary of the SATA port configuration registers (base address: 0x1101_0100)

Offset Address	Register	Description	Page
0x000 + *n* x 0x80	SATA_PORT_CLB	Command list base address register	13-125
0x008 + *n* x 0x80	SATA_PORT_FB	RX FIS base address register	13-125
0x010 + *n* x 0x80	SATA_PORT_IS	Port interrupt status register	13-126
0x014 + *n* x 0x80	SATA_PORT_IE	Port interrupt mask register	13-128
0x018 + *n* x 0x80	SATA_PORT_CMD	Port command and status register	13-129
0x20 + *n* x 0x80	SATA_PORT_TFD	Port task file register	13-132
0x24 + *n* x 0x80	SATA_PORT_SIG	Port signature register	13-132
0x028 + *n* x 0x80	SATA_PORT_SSTS	Port status register	13-133
0x02C + *n* x 0x80	SATA_PORT_SCTL	Port control register	13-134
0x30 + *n* x 0x80	SATA_PORT_SERR	Error diagnosis status register	13-135
0x034 + *n* x 0x80	SATA_PORT_SACT	NCQ command identifier control register	13-136

Offset Address	Register	Description	Page
0x38 + *n* x 0x80	SATA_PORT_CI	Command transmit control register	13-137
0x3C + *n* x 0x80	SATA_PORT_SNTF	Async notification event indicator register	13-138
0x40 + *n* x 0x80	SATA_PORT_FBS	FIS-based switching control register	13-138
0x044 + *n* x 0x80	SATA_PORT_FIFOTH	RX FIFO threshold register	13-139
0x048 + *n* x 0x80	SATA_PORT_PHYCTL1	PHY control register 1	13-140
0x04C + *n* x 0x80	SATA_PORT_PHYCTL2	PHY control register 2	13-141
0x050 + *n* x 0x80	SATA_PORT_HBA	Host bus adapter (HBA) test status register	13-141
0x054 + *n* x 0x80	SATA_PORT_LINK	Link test status register	13-142
0x058 + *n* x 0x80	SATA_PORT_DMA1	DMAC test status register 1	13-143
0x05C + *n* x 0x80	SATA_PORT_DMA2	DMAC test status register 2	13-144
0x060 + *n* x 0x80	SATA_PORT_DMA3	DMAC test status register 3	13-145
0x064 + *n* x 0x80	SATA_PORT_DMA4	DMAC test status register 4	13-145
0x068 + *n* x 0x80	SATA_PORT_DMA5	DMAC test status register 5	13-145
0x6C + *n* x 0x80	SATA_PORT_DMA6	DMAC test status register 6	13-146
0x070 + *n* x 0x80	SATA_PORT_DMA7	DMAC test status register 7	13-146
0x074 + *n* x 0x80	SATA_PORT_PHYCTL	PHY control register	13-148
0x078 + *n* x 0x80	SATA_PORT_PHYSTS	PHY test status register	13-149
0x07C + *n* x 0x80	SATA_PORT_OUTSTANDING	AXI outstanding control register	13-150

13.6.7 Register Description

13.6.7.1 SATA Registers

SATA_GHC_CAP1

SATA_GHC_CAP1 is feature support register 1.

Offset Address	Register Name	Total Reset Value
0x0000	SATA_GHC_CAP1	0x6F37_7FA1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	s64a		sncq		ssntf		smps		sss		salp		sal		sclo		iss				reserved		sam		spm		fbss		pmd		ssc		psc		ncs				cccs		ems		sxs		np				
Reset	0		1		1		0		1		1		1		1		0		0		1		1		1		1		0		1		1		1		1		1		1		0		1		0		0		0		0		0		1	

Bits	Access	Name	Description
[31]	RO	s64a	Fixed at 0, indicating that the 64-bit data structure cannot be accessed.
[30]	RO	sncq	Fixed at 1, indicating that NCQ is supported.
[29]	RO	ssntf	Fixed at 1, indicating that the port SNTF register is supported.
[28]	RO	smps	Fixed at 0, indicating that mechanical hot-plugging is not supported.
[27]	RO	sss	Fixed at 1, indicating that staggered spin-up is supported.
[26]	RO	salp	Fixed at 1, indicating that power supply management is supported.
[25]	RO	sal	Fixed at 1, indicating that the LED pin is supported.
[24]	RO	sclo	Fixed at 1, indicating that command linked list override is supported.
[23:20]	RO	iss	Fixed at 0x3, indicating that the maximum rate is 6 Gbit/s.
[19]	RO	reserved	Reserved
[18]	RO	sam	Fixed at 1, indicating that only the AHCI mode is supported.
[17]	RO	spm	Fixed at 1, indicating that the port multiplier is supported.
[16]	RO	fbss	Fixed at 1, indicating that FIS-based switching is supported.
[15]	RO	pmd	Fixed at 0, indicating that multiple DRQ blocks cannot be transferred in PIO mode.
[14]	RO	ssc	Fixed at 1, indicating that the transition to the slumber status is supported.
[13]	RO	psc	Fixed at 1, indicating that the transition to the partial status is supported.
[12:8]	RO	ncs	Fixed at 0x1F, indicating that 32 command slots are supported.

[7]	RO	cccs	Fixed at 1, indicating that the CCC function is supported.
[6]	RO	ems	Fixed at 0, indicating that enclose management is not supported.
[5]	RO	sxs	Fixed at 1, indicating that the external SATA port is supported.
[4:0]	RO	np	Fixed at 0x01, indicating that two SATA ports are supported.

SATA_GHC_GHC

SATA_GHC_GHC is a global control register.

Offset Address	Register Name	Total Reset Value
0x0004	SATA_GHC_GHC	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahci_en	Reserved																													int_enable	hba_rst
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	ahci_en	Fixed at 1, indicating that the software can interact with the controller only through the AHCI mechanism.
[30:2]	RO	reserved	Reserved
[1]	RW	int_enable	Controller interrupt enable 0: disabled 1: enabled
[0]	RW	hba_rst	Soft reset control for the controller 0: not reset 1: reset Writing 1 resets the controller and this bit is automatically cleared after reset; writing 0 has no effect. In addition, reset has no effect on the registers SATA_GHC_BOHC, SATA_PORT_FB, and SATA_PORT_CLB.

SATA_GHC_IS

SATA_GHC_IS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0008	SATA_GHC_IS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ips_ccc	Reserved																													ips_port1	ips_port0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	WC	ips_ccc	CCC interrupt status 0: No CCC interrupt is generated. 1: A CCC interrupt is generated.
[30:2]	RO	reserved	Reserved
[1]	WC	ips_port1	Interrupt status of port 1 0: No interrupt is reported. 1: An interrupt is reported.
[0]	WC	ips_port0	Interrupt status of port 0 0: No interrupt is reported. 1: An interrupt is reported.

SATA_GHC_PI

SATA_GHC_PI is a port implementation register.

Offset Address	Register Name	Total Reset Value
0x000C	SATA_GHC_PI	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																														port_imp	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RO	port_imp	Port validity indicator. If the value is 0x3, three ports (ports 0−1) are valid. Bit[1] to bit[0] correspond to port 1 to port 0 respectively. 0: invalid 1: valid

SATA_GHC_VS

SATA_GHC_VS is an AHCI version identifier register.

Offset Address	Register Name	Total Reset Value
0x0010	SATA_GHC_VS	0x0001_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	achi_vs																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	achi_vs	The supported AHCI version is V1.3.

SATA_GHC_CCC_CTL

SATA_GHC_CCC_CTL is a CCC control register.

Offset Address	Register Name	Total Reset Value
0x0014	SATA_GHC_CCC_CTL	0x0001_01F8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ccc_tv																ccc_cc								ccc_int					reserved		ccc_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	ccc_tv	CCC timeout parameter, in the unit of ms When the CCC function is enabled, the timeout counter loads this parameter value. If a command is executed on a port involved in CCC counting, the counter decreases by 1 every 1 ms until a CCC interrupt is generated when the counter reaches 0. Then the counter reloads the parameter value for the next counting. Note that these bits cannot be set to 0s.

[15:8]	RW	ccc_cc	CCC command completion upper limit When the CCC function is enabled, the counter is cleared after commands are executed. Then the counter starts to count the number of completed commands on the ports involved in CCC counting. If the count value is greater than or equal to the parameter value, a CCC interrupt is generated. In this case, the counter is cleared again for the next counting. If the value 0 is written, the command completion interrupt is disabled and the CCC interrupt is generated only after timeout.
[7:3]	RO	ccc_int	CCC interrupt vector ID. If the value is 0x1F (31), SATA_GHC_IS bit[31] indicates the CCC interrupt status.
[2:1]	RO	reserved	Reserved
[0]	RW	ccc_en	CCC function enable 0: disabled 1: enabled When the CCC function is enabled, the values of ccc_tv and ccc_cc cannot be changed.

SATA_GHC_CCC_PORTS

SATA_GHC_CCC_PORTS is a CCC port enable register.

Offset Address	Register Name	Total Reset Value
0x0018	SATA_GHC_CCC_PORTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																														ccc_prt	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	ccc_prt	Specifies the port that is involved in CCC counting. Bit[1] to bit[0] correspond to port 1 to port 0 respectively. If the related bit is 1, the port is involved in CCC counting. If the related bit is 0. The port is not involved in CCC counting. The value of this register can be changed at any time and the changed value takes effect immediately.

SATA_GHC_CAP2

SATA_GHC_CAP2 is feature support register 2.

Offset Address	Register Name	Total Reset Value
0x0024	SATA_GHC_CAP2	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																															cap_boh
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	cap_boh	Fixed at 1, indicating that BIOS/OS handoff control is supported.

SATA_GHC_BOHC

SATA_GHC_BOHC is a BIOS/OS handoff control register.

Offset Address	Register Name	Total Reset Value
0x0028	SATA_GHC_BOHC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																											bohc_bb	bohc_ooc	bohc_sooe	bohc_oos	bohc_bos
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	bohc_bb	BIOS status indicator 0: The BIOS is not busy. 1: The BIOS is busy in performing certain operations and is ready to hand the control permission off to the OS.
[3]	WC	bohc_ooc	When the value of bohc_oos is changed from 0 to 1, this bit is fixed at 1. Writing 1 clears this bit and writing 0 has no effect.
[2]	RW	bohc_sooe	Message interrupt enable 0: No message interrupt is generated. 1: When bohc_ooc is set to 1, a message interrupt is generated.

[1]	RW	bohc_oos	Request applied by the OS for controlling the controller 0: The OS does not apply for the control permission on the controller. 1: The OS applies for the control permission on the controller. If bohc_oos is 1 and bios_bos is 0, it indicates that the OS has obtained the control permission on the SATA controller. Resetting the SATA controller through SATA_GHC_GHC[hab_rst] has no effect on this bit.
[0]	RW	bohc_bos	Flag indicating that the BIOS has the control permission on the controller 0: The BIOS does not have the control permission on the controller. 1: The BIOS has the control permission on the controller. If the OS applies for the control permission on the controller, the BIOS clears this bit. Resetting the SATA controller through SATA_GHC_GHC[hab_rst] has no effect on this bit.

SATA_PHY0_CTLL

SATA_PHY0_CTLL is a lower-bit PHY 0 global control register.

Offset Address	Register Name	Total Reset Value
0x00A0	SATA_PHY0_CTLL	0x4980_003C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	los_bias				los_level				reserved	ssc_ref_clk_sel											ssc_range		ssc_en	ref_ssp_en	ref_clkdiv2	mpll_multiplier							reset
Reset	0	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits	Access	Name	Description
[31:29]	RW	los_bias	Loss-of-signal detection voltage threshold. This field must be set to 0x2.
[28:24]	RW	los_level	Loss-of-signal detection voltage threshold. This field must be set to 0x9.
[23]	RO	reserved	Reserved
[22:14]	RW	ssc_ref_clk_sel	Spread spectrum clocking shifting

[13:11]	RW	ssc_range	Clock frequency offset when ssc_en is valid 000: −4980 001: −4492 010: −4003 011: −2000 100: +4980 101: +4492 110: +4003 111: +2000
[10]	RW	ssc_en	Clock spread spectrum enable 0: disabled 1: enabled
[9]	RW	ref_ssp_en	Reference clock enable 0: disabled 1: enabled
[8]	RW	ref_clkdiv2	Whether frequency division is performed on the input reference clock. If the input reference clock is higher than 100 MHz, this bit must be set to 1.
[7:1]	RW	mpll_multiplier	SerDes MPLL frequency output. The reference clock frequency is multiplied based on the MPLL frequency output to generate required high-frequency clocks. If the reference clock is 100 MHz, the value is set to 7'b0011110.
[0]	RW	reset	Reset signal, active high. This signal must be retained for 5 ns at least.

SATA_PHY0_CTLH

SATA_PHY0_CTLH is an upper-bit PHY 0 global control register.

Offset Address	Register Name	Total Reset Value
0x00A4	SATA_PHY0_CTLH	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												data_invert	test_powerdown	test_bypass	test_burnin
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved

[3]	RW	data_invert	0: The endian modes of the PHY and parallel data interface connected to the SATA controller are the same. 1: The endian modes of the PHY and parallel data interface connected to the SATA controller are opposite.
[2]	RW	test_powerdown	Test control signal for controlling the power-down mode of all circuits. This field is used during the IDDQ test. 0: not powered down 1: powered down
[1]	RW	test_bypass	Test control signal, connected to ground
[0]	RW	test_burnin	Test control signal, connected to ground

SATA_PHY0_STS

SATA_PHY0_STS is a PHY 0 global status register.

Offset Address	Register Name	Total Reset Value
0x00A8	SATA_PHY0_STS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy0_sts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	phy0_sts	Status of the common part of SATA PHY 0

SATA_PHY1_CTLL

SATA_PHY1_CTLL is a lower-bit PHY 1 global control register.

Offset Address	Register Name	Total Reset Value
0x00AC	SATA_PHY1_CTLL	0x4980_003C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	los_bias				los_level				reserved	ssc_ref_clk_sel											ssc_range			ssc_en	ref_ssp_en	ref_clkdiv2	mpll_multiplier						reset	
Reset	0	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits	Access	Name	Description
[31:29]	RW	los_bias	Loss-of-signal detection voltage threshold. This field must be set to 0x2.

[28:24]	RW	los_level	Loss-of-signal detection voltage threshold. This field must be set to 0x9.
[23]	RO	reserved	Reserved
[22:14]	RW	ssc_ref_clk_sel	Spread spectrum clocking shifting
[13:11]	RW	ssc_range	Clock frequency offset when ssc_en is valid 000: −4980 001: −4492 010: −4003 011: −2000 100: +4980 101: +4492 110: +4003 111: +2000
[10]	RW	ssc_en	Clock spread spectrum enable 0: disabled 1: enabled
[9]	RW	ref_ssp_en	Reference clock enable 0: disabled 1: enabled
[8]	RW	ref_clkdiv2	Whether frequency division is performed on the input reference clock. If the input reference clock is higher than 100 MHz, this bit must be set to 1.
[7:1]	RW	mpll_multiplier	SerDes MPLL frequency output. The reference clock frequency is multiplied based on the MPLL frequency output to generate required high-frequency clocks. If the reference clock is 100 MHz, the value is set to 7'b0011110.
[0]	RW	reset	Reset signal, active high. This signal must be retained for 5 ns at least.

SATA_PHY1_CTLH

SATA_PHY1_CTLH is an upper-bit PHY 1 global control register.

Offset Address	Register Name	Total Reset Value
0x00B0	SATA_PHY1_CTLH	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												data_invert		test_powerdown		test_bypass		test_burnin	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	data_invert	0: The endian modes of the PHY and parallel data interface connected to the SATA controller are the same. 1: The endian modes of the PHY and parallel data interface connected to the SATA controller are opposite.
[2]	RW	test_powerdown	Test control signal for controlling the power-down mode of all circuits. This field is used during the IDDQ test. 0: not powered down 1: powered down
[1]	RW	test_bypass	Test control signal, connected to ground
[0]	RW	test_burnin	Test control signal, connected to ground

SATA_PHY1_STS

SATA_PHY1_STS is a PHY 1 global status register.

Offset Address	Register Name	Total Reset Value
0x00B4	SATA_PHY1_STS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy1_sts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	phy1_sts	Status of the common part of SATA PHY 1

SATA_OOB_CTL

SATA_OOB_CTL is a PHY OOB control register.

Offset Address	Register Name	Total Reset Value
0x00B8	SATA_OOB_CTL	0x8406_0C15

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	oob_ctrl_valid				min_comiwake				max_comwake								min_cominit								max_cominit							
Reset	1	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	0	1

Bits	Access	Name	Description
[31]	RW	oob_ctrl_valid	Configuration bit of the OOB detection parameter. For high level, this bit is used to select the parameter configurations of this register.
[30:24]	RW	min_comiwake	Minimum space required for the COMWAKE space detection
[23:16]	RW	max_comwake	Maximum space required for the COMWAKE space detection
[15:8]	RW	min_cominit	Minimum space required for the COMINIT space detection
[7:0]	RW	max_cominit	Maximum space required for the COMINIT space detection

SATA_AXI_DFX0

SATA_AXI_DFX0 is a SATA AXI bus control register.

Offset Address	Register Name	Total Reset Value
0x00BC	SATA_AXI_DFX0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cnt_wr3	cnt_wr2	cnt_wr1	cnt_wr0	reserved				cnt_rd3	cnt_rd2	cnt_rd1	cnt_rd0	cnt_wr_latency_clr	cnt_wr_acc_clr	cnt_rd_latency_clr	cnt_rd_acc_clr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	cnt_wr3	Whether to enable the DFX function on internal AXI channel 3 (SATA port 1 RX DMAC) in the write direction. This bit is active high. 0: disabled 1: enabled

[14]	RW	cnt_wr2	Whether to enable the DFX function on internal AXI channel 2 (SATA port 1 RX DMAC) in the write direction. This bit is active high. 0: disabled 1: enabled
[13]	RW	cnt_wr1	Whether to enable the DFX function on internal AXI channel 1 (SATA port 0 RX DMAC) in the write direction. This bit is active high. 0: disabled 1: enabled
[12]	RW	cnt_wr0	Whether to enable the DFX function on internal AXI channel 0 (SATA port 0 TX DMAC) in the write direction. This bit is active high. 0: disabled 1: enabled
[11:8]	RO	reserved	Reserved
[7]	RW	cnt_rd3	Whether to enable the DFX function on internal AXI channel 3 (SATA port 1 RX DMAC) in the read direction. This bit is active high. 0: disabled 1: enabled
[6]	RW	cnt_rd2	Whether to enable the DFX function on internal AXI channel 2 (SATA port 1 TX DMAC) in the read direction. This bit is active high. 0: disabled 1: enabled
[5]	RW	cnt_rd1	Whether to enable the DFX function on internal AXI channel 1 (SATA port 0 RX DMAC) in the read direction. This bit is active high. 0: disabled 1: enabled
[4]	RW	cnt_rd0	Whether to enable the DFX function on internal AXI channel 0 (SATA port 0 TX DMAC) in the read direction. This bit is active high. 0: disabled 1: enabled
[3]	RW	cnt_wr_latency_clr	Clear of the latency debugging register of the current write channel, active high 0: not cleared 1: cleared

[2]	RW	cnt_wr_acc_clr	Clear of the total command number debugging register of the current write channel, active high 0: not cleared 1: cleared
[1]	RW	cnt_rd_latency_clr	Clear of the latency debugging register of the current read channel, active high 0: not cleared 1: cleared
[0]	RW	cnt_rd_acc_clr	Clear of the total command number debugging register of the current read channel, active high 0: not cleared 1: cleared

SATA_AXI_DFX1

SATA_AXI_DFX1 is SATA AXI bus status register 1.

Offset Address	Register Name	Total Reset Value
0x00C0	SATA_AXI_DFX1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cnt_rd_latency_max																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	cnt_rd_latency_max	DFX signals, indicating the maximum latency (in cycle) of the current read channel

SATA_AXI_DFX2

SATA_AXI_DFX2 is SATA AXI bus status register 2.

Offset Address	Register Name	Total Reset Value
0x00C4	SATA_AXI_DFX2	0x0000_001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cnt_rd_latency_avg																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RO	cnt_rd_latency_avg	DFX signals, indicating the average latency (in cycle) of the current read channel

SATA_AXI_DFX3

SATA_AXI_DFX3 is SATA AXI bus to the status register 3.

Offset Address	Register Name	Total Reset Value
0x00C8	SATA_AXI_DFX3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cnt_wr_latency_max																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	cnt_wr_latency_max	DFX signals, indicating the maximum latency (in cycle) of the current write channel

SATA_AXI_DFX4

SATA_AXI_DFX4 is SATA AXI bus status register 4.

Offset Address	Register Name	Total Reset Value
0x00CC	SATA_AXI_DFX4	0x0000_001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cnt_wr_latency_avg																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	cnt_wr_latency_avg	DFX signal, indicating the average latency (in cycle) of the current write channel

SATA_AXI_DFX5

SATA_AXI_DFX5 is SATA AXI bus status register 5.

Offset Address	Register Name	Total Reset Value
0x00D0	SATA_AXI_DFX5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cnt_rd_acc3								cnt_rd_acc2								cnt_rd_acc1								cnt_rd_acc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	cnt_rd_acc3	DFX signal, indicating the total number of current read commands of AXI master port 3 (corresponding to the SATA port 1 RX DMAC)
[23:16]	RO	cnt_rd_acc2	DFX signal, indicating the total number of current read commands of AXI master port 2 (corresponding to the SATA port 1 TX DMAC)
[15:8]	RO	cnt_rd_acc1	DFX signal, indicating the total number of current read commands of AXI master port 1 (corresponding to the SATA port 0 RX DMAC)
[7:0]	RO	cnt_rd_acc0	DFX signal, indicating the total number of current read commands of AXI master port 0 (corresponding to the SATA port 0 TX DMAC)

SATA_AXI_DFX7

SATA_AXI_DFX7 is SATA AXI bus status register 7.

Offset Address	Register Name	Total Reset Value
0x00D8	SATA_AXI_DFX7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cnt_wr_acc3								cnt_wr_acc2								cnt_wr_acc1								cnt_wr_acc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	cnt_wr_acc3	DFX signal, indicating the total number of current write commands of AXI master port 3 (corresponding to the SATA port 1 RX DMAC)
[23:16]	RO	cnt_wr_acc2	DFX signal, indicating the total number of current write commands of AXI master port 2 (corresponding to the SATA port 1 TX DMAC)
[15:8]	RO	cnt_wr_acc1	DFX signal, indicating the total number of current write commands of AXI master port 1 (corresponding to the SATA port 0 RX DMAC)

[7:0]	RO	cnt_wr_acc0	DFX signal, indicating the total number of current write commands of AXI master port 0 (corresponding to the SATA port 0 TX DMAC)

SATA_AXI_DFX9

SATA_AXI_DFX9 is SATA AXI bus status register 9.

Offset Address	Register Name	Total Reset Value
0x00E0	SATA_AXI_DFX9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cnt_rd_otd3								cnt_rd_otd2								cnt_rd_otd1								cnt_rd_otd0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	cnt_rd_otd3	DFX signal, indicating the total number of current read outstanding commands of AXI master port 3 (corresponding to the SATA port 1 RX DMAC)
[23:16]	RO	cnt_rd_otd2	DFX signal, indicating the total number of current read outstanding commands of AXI master port 2 (corresponding to the SATA port 1 TX DMAC)
[15:8]	RO	cnt_rd_otd1	DFX signal, indicating the total number of current read outstanding commands of AXI master port 1 (corresponding to the SATA port 0 RX DMAC)
[7:0]	RO	cnt_rd_otd0	DFX signal, indicating the total number of current read outstanding commands of AXI master port 0 (corresponding to the SATA port 0 TX DMAC)

SATA_AXI_DFX11

SATA_AXI_DFX11 SATA AXI bus to the status register 11.

Offset Address	Register Name	Total Reset Value
0x00E8	SATA_AXI_DFX11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cnt_wr_otd3								cnt_wr_otd2								cnt_wr_otd1								cnt_wr_otd0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	cnt_wr_otd3	DFX signal, indicating the total number of current write outstanding commands of AXI master port 3 (corresponding to the SATA port 1 RX DMAC)

[23:16]	RO	cnt_wr_otd2	DFX signal, indicating the total number of current write outstanding commands of AXI master port 2 (corresponding to the SATA port 1 TX DMAC)
[15:8]	RO	cnt_wr_otd1	DFX signal, indicating the total number of current write outstanding commands of AXI master port 1 (corresponding to the SATA port 0 RX DMAC)
[7:0]	RO	cnt_wr_otd0	DFX signal, indicating the total number of current write outstanding commands of AXI master port 0 (corresponding to the SATA port 0 TX DMAC)

13.6.7.2 SATA Port Configuration Registers

SATA_PORT_CLB

SATA_PORT_CLB is a command list base address register.

Offset Address	Register Name	Total Reset Value
0x000 + *n* x 0x80	SATA_PORT_CLB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_clb																								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	port_clb	Base address for storing the port command list in the memory Resetting the SATA controller through SATA_GHC_GHC[hab_rst] has no effect on this field.
[9:0]	RO	reserved	Reserved

SATA_PORT_FB

SATA_PORT_FB is an RX FIS base address register.

Offset Address	Register Name	Total Reset Value
0x008 + *n* x 0x80	SATA_PORT_FB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_fb																								reserved							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	port_fb	Base address in the memory for storing the frames received through the port Resetting the SATA controller through SATA_GHC_GHC[hab_rst] has no effect on this field.
[7:0]	RO	reserved	Reserved

SATA_PORT_IS

SATA_PORT_IS is a port interrupt status register.

Offset Address	Register Name	Total Reset Value
0x010 + *n* x 0x80	SATA_PORT_IS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	pxis_tfes	reserved	pxis_hbds	pxis_ifs	pxis_infs	reserved	pxis_ofs	pxis_ipms	pxis_prcs	reserved														pxis_pcs	pxis_dps	pxis_ufs	pxis_sdbs	pxis_dss	pxis_pss	pxis_dhrs	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	WC	pxis_tfes	Task file data (TFD) error interrupt status 0: The value of SATA_PORT_TFD bit[0] is not 1. 1: The value of SATA_PORT_TFD bit[0] is 1.
[29]	RO	reserved	Reserved
[28]	WC	pxis_hbds	Internal bus error interrupt 0: The DMAC accesses the memory properly. 1: An error occurs when the DMAC accesses the memory.
[27]	WC	pxis_ifs	Fatal error interrupt status 0: No error occurs during the data frame transfer. 1: An error occurs during the data frame transfer.
[26]	WC	pxis_infs	Non-fatal error interrupt status 0: No error occurs during the non-data frame transfer. 1: An error occurs during the non-data frame transfer.
[25]	RO	reserved	Reserved

[24]	WC	pxis_ofs	Data transfer overflow interrupt status 0: No overflow is detected. 1: During the data frame transfer, if the size of the data memory occupied by commands is smaller than the actual data amount, an interrupt is reported at the end of the data transfer.
[23]	WC	pxis_ipms	PM port number error interrupt status 0: No PM port number error is detected during data reception. 1: A PM port number error is detected during data reception.
[22]	RO	pxis_prcs	PHY status change interrupt status 0: No changes of the phyrdy signal are detected. 1: Changes of the phyrdy signal are detected. This bit directly reflects the value of SATA_PORT_SERR[diag_n].
[21:7]	RO	reserved	Reserved
[6]	RO	pxis_pcs	Port connection change interrupt status 0: No COMINIT signal transmitted from the device is detected. 1: A COMINIT signal transmitted from the device is detected. This bit directly reflects the value of SATA_PORT_SERR[diag.x].
[5]	WC	pxis_dps	Linked list transfer completion interrupt status 0: The transfer of the linked list data is complete when no I bit in the PRD is 1. 1: The transfer of the linked list data is complete when an I bit in the PRD is 1.
[4]	RO	pxis_ufs	Unknown FIS interrupt status 0: No unknown FIS is received. 1: An unknown FIS is received.
[3]	WC	pxis_sdbs	Set device bits FIS interrupt status 0: no effect 1: A set device bits FIS is received and the I bit is 1.
[2]	WC	pxis_dss	DMA setup FIS interrupt status 0: no effect 1: A DMA setup FIS is received and the I bit is 1.
[1]	WC	pxis_pss	PIO setup FIS interrupt status 0: no effect 1: A PIO setup FIS is received and the I bit is 1.
[0]	WC	pxis_dhrs	D2H register FIS interrupt status 0: no effect 1: A D2H register FIS is received and the I bit is 1.

SATA_PORT_IE

SATA_PORT_IE is a port interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x014 + *n* x 0x80	SATA_PORT_IE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	pxie_tfee	reserved	pxie_hbde	pxie_ife	pxie_infe	reserved	pxie_ofe	pxie_ipme	pxie_prce	Reserved															pxie_pce	pxie_dpe	pxie_ufe	pxie_sdbe	pxie_dse	pxie_pse	pxie_dhre
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	pxie_tfee	TFD error interrupt mask 0: masked 1: not masked
[29]	RO	reserved	Reserved
[28]	RW	pxie_hbde	Internal bus error interrupt mask 0: masked 1: not masked
[27]	RW	pxie_ife	Fatal error interrupt mask 0: masked 1: not masked
[26]	RW	pxie_infe	Non-fatal error interrupt mask 0: masked 1: not masked
[25]	RO	reserved	Reserved
[24]	RW	pxie_ofe	Data transfer overflow interrupt mask 0: masked 1: not masked
[23]	RW	pxie_ipme	PM port error interrupt mask 0: masked 1: not masked
[22]	RW	pxie_prce	PHY status change interrupt mask 0: masked 1: not masked
[21:7]	RO	reserved	Reserved

[6]	RW	pxie_pce	Port connection change interrupt mask 0: masked 1: not masked
[5]	RW	pxie_dpe	Linked list transfer completion interrupt mask 0: masked 1: not masked
[4]	RW	pxie_ufe	Unknown FIS interrupt mask 0: masked 1: not masked
[3]	RW	pxie_sdbe	Set device bits FIS interrupt mask 0: masked 1: not masked
[2]	RW	pxie_dse	DMA setup FIS interrupt mask 0: masked 1: not masked
[1]	RW	pxie_pse	PIO setup FIS interrupt mask 0: masked 1: not masked
[0]	RW	pxie_dhre	D2H register FIS interrupt mask 0: masked 1: not masked

SATA_PORT_CMD

SATA_PORT_CMD is a port command and status register.

Offset Address	Register Name	Total Reset Value
0x018 + *n* x 0x80	SATA_PORT_CMD	0x0060_0000

Bit	31 30 29 28	27	26	25	24	23	22	21	20	19 18 17 16	15	14	13	12	11 10 9 8	7 6 5 4	3	2	1	0
Name	cmd_icc	cmd_asp	cmd_alpe	cmd_dlae	cmd_atapi	reserved	fbscp	cmd_esp	reserved	cmd_pma	reserved	cmd_cr	cmd_fr	reserved	cmd_ccs	reserved	cmd_fre	cmd_clo	reserved	cmd_sud	cmd_st

Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:28]	RW	cmd_icc	Port communication control signal 0x0: No operation. It indicates that the next port status request is allowed. 0x1: Request to enable the port to be in the active status. 0x2: Request to enable the port to be in the partial status. 0x6: Request to enable the port to be in the slumber status. Other values: reserved When the software writes any of the preceding values rather than the reserved value, the controller clears the cmd_icc bit after performing related operations. When the software requests the current status of the port, the controller clears the cmd_icc bit directly. If the software requests the port status change from a low-power status to another low-power status, such as from the partial status to the slumber status, it needs to request the status change from the partial status to the active status, and then to the slumber status.
[27]	RW	cmd_asp	Slumber or partial status select for power management 0: proactively enter the partial status. 1: proactively enter the slumber status.
[26]	RW	cmd_alpe	Automatic power management enable 0: disabled 1: enabled If SATA_PORT_CI and SATA_PORT_SACT are cleared, the controller enters the power-management status automatically. To be specific, if cmd_asp is 1, the controller enters the partial status; if cmd_asp is 0, the controller enters the slumber status.
[25]	RW	cmd_dlae	LED drive enable in ATAPI mode 0: The LED pin can be driven when cmd_atapi is 0 and commands are being executed. 1: The LED pin can be driven when commands are being executed.
[24]	RW	cmd_atapi	ATAPI device indicator 0: The current device is not an ATAPI device. 1: The current device is an ATAPI device.
[23]	RO	reserved	Reserved
[22]	RO	fbscp	Whether the port supports FIS-based switching. When SATA_GHC_CAP1[spm] and SATA_GHC_CAP1[FBSS] are set to 1, this bit must be set to 1. 0: not supported 1: supported
[21]	RO	cmd_esp	Fixed at 1, indicating that the external SATA device is supported

[20:18]	RO	reserved	Reserved
[17]	RW	cmd_pma	Port multiplier detection indicator 0: No port multiplier is connected to the port. 1: A port multiplier is connected to the port.
[16]	RO	reserved	Reserved
[15]	RO	cmd_cr	Command list processing indicator 0: No command is being executed. 1: A command is being executed.
[14]	RO	cmd_fr	FIS receive processing indicator 0: No FIS is being received. 1: An FIS is being received.
[13]	RO	reserved	Reserved
[12:8]	RO	cmd_ccs	Slot number of the current command This field is valid when cmd_st is 1 and is cleared when cmd_st is 0.
[7:5]	RO	reserved	Reserved
[4]	RW	cmd_fre	FIS receive enable control 0: forbid to write the received FISs to the system memory 1: enable the received FISs and write them to the system memory The software needs to set the receive FIS base address register SATA_PORT_FB before enabling this bit to receive FISs. When cmd_st is 1, this bit must be set to 1.
[3]	RW	cmd_clo	BSY/DQR clear control. The software can forcibly clear the BSY and DRQ bits through this bit and transmit commands to the device. 0: no effect 1: Clear the BSY and DRQ bits of SATA_PORT_TFD[tfd_sts]. After the BSY and DRQ bits are 0, the cmd_clo bit is automatically cleared. The cmd_clo bit can be written as 1 only before the value of cmd_st is changed from 0 to 1. In addition, the software must write 1 to cmd_st after the cmd_clo bit is cleared.
[2]	RO	reserved	Reserved
[1]	RW	cmd_sud	Spin-up device control 0: When SATA_PORT_SCTL[det] is 0, the controller enters the listen mode. 1: After the system is powered on or the HBA is reset, the controller is enabled to transmit a COMRESET sequence to initialize the hardware device.

[0]	RW	cmd_st	Command list processing enable 0: The controller enters the idle status. 1: The controller processes the commands from slot 0 that are identified as valid slots by SATA_PORT_CI. **NOTE** The cmd_st bit can be set to 1 only after cmd_fre is 1.

SATA_PORT_TFD

SATA_PORT_TFD is a port task file register.

Offset Address	Register Name	Total Reset Value
0x20 + *n* x 0x80	SATA_PORT_TFD	0x0000_007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																tfd_err								tfd_sts							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RO	tfd_err	Task file error The controller updates this field after receiving a D2H register FIS, a PIO setup FIS, or an SDB FIS.
[7:0]	RO	tfd_sts	Task file status bit[7]: BSY bit. It indicates that the device is busy. bit[6:4]: The meaning of this field varies according to commands. bit[3]: DRQ bit. It indicates that there is the data to be transferred in the device. bit[2:1]: The meaning of this field varies according to commands. bit[0]: ERR bit. It indicates that an error occurs during the data transfer. The controller updates this field after receiving a D2H register FIS, a PIO setup FIS, or an SDB FIS.

SATA_PORT_SIG

SATA_PORT_SIG is a port signature register.

Offset Address	Register Name	Total Reset Value
0x24 + *n* x 0x80	SATA_PORT_SIG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Signature																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	signature	LBA address and sector addressing. The allocated addresses are as follows: bit[31:24]: LBA upper-bit address bit[23:16]: LBA middle-bit address bit[15:8]: LBA lower-bit address bit[7:0]: number of sectors The controller updates this register when receiving the first D2H register FIS after the hardware device is reset.

SATA_PORT_SSTS

SATA_PORT_SSTS is a port status register.

Offset Address	Register Name	Total Reset Value
0x028 + *n* x 0x80	SATA_PORT_SSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pxssts_ipm				pxssts_spd				pxssts_det			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RO	pxssts_ipm	Current port status 0x0: No devices exist or no communication is set up. 0x1: active 0x2: partial 0x6: slumber Other values: reserved

[7:4]	RO	pxssts_spd	Port negotiation speed 0x0: No devices exist or no communication is set up. 0x1: Rate 1 is negotiated for communication. 0x2: Rate 2 is negotiated for communication. 0x3: Rate 3 is negotiated for communication. Other values: reserved
[3:0]	RO	pxssts_det	Device detection and PHY status 0x0: No device is detected and no PHY communication is set up. 0x1: A device is detected but no PHY communication is set up. 0x3: A device is detected but the PHY communication is set up. 0x4: The PHY is offline or in the built-in self test (BIST) status. Other values: reserved

SATA_PORT_SCTL

SATA_PORT_SCTL is a port control register.

Offset Address	Register Name	Total Reset Value
0x02C + *n* x 0x80	SATA_PORT_SCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pxsctl_ipm				pxsctl_spd				pxsctl_det			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:8]	RW	pxsctl_ipm	Port power management status control 0x0: no requirements 0x1: forbid to enter the partial status 0x2: forbid to enter the slumber status 0x3: forbid to enter the partial or slumber state Other values: reserved
[7:4]	RW	pxsctl_spd	Port communication speed control 0x0: no requirements 0x1: limit the communication speed to rate 1 0x2: limit the communication speed to rate 2 0x3: limit the communication speed to rate 3 Other values: reserved

[3:0]	RW	pxsctl_det	Device detection and port initialization control 0x0: no device detection or initialization request 0x1: request the port to reset the initialization sequence COMRESET 0x4: force the port to be offline Other values: reserved When pxsctl_det is set to 1, the controller transmits the COMRESET sequence to the device. In this case, to ensure that the device receives the COMRESET sequence, the software must retain the value 1 of pxsctl_det for at least 1 ms.

SATA_PORT_SERR

SATA_PORT_SERR is an error diagnosis status register.

Offset Address	Register Name	Total Reset Value
0x30 + *n* x 0x80	SATA_PORT_SERR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					diag_x	diag_f	reserved	diag_s	diag_h	diag_c	reserved	diag_b	diag_w	diag_i	diag_n	reserved					err_p	reserved	err_t	reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	WC	diag_x	Device detection status 0: No COMINIT signal transmitted from the device is detected. 1: A COMINIT signal transmitted from the device is detected.
[25]	WC	diag_f	Detection status of the unknown FIS 0: No unknown FIS is received. 1: An unknown FIS is received and this bit is set to 1 when the cyclic redundancy check (CRC) is correct.
[24]	RO	reserved	Reserved
[23]	WC	diag_s	Link layer error status 0: No status transition error occurs at the link layer. 1: A status transition error occurs at the link layer.
[22]	WC	diag_h	Handshake error status 0: No R_ERR primitive transmitted from the device is received. 1: One or more R_ERR primitives transmitted from the device are received.

[21]	WC	diag_c	CRC error status 0: No CRC error occurs during FIS receiving. 1: A CRC error occurs during FIS receiving.
[20]	RO	reserved	Reserved
[19]	WC	diag_b	Decoding error status 0: No 8B/10B decoding error is detected. 1: An 8B/10B decoding error is detected.
[18]	WC	diag_w	COMWAKE status 0: No COMWAKE signal transmitted from the device is detected. 1: A COMWAKE signal transmitted from the device is detected.
[17]	WC	diag_i	PHY internal error status 0: No PHY internal error is detected. 1: A PHY internal error is detected.
[16]	WC	diag_n	PhyRdy signal change status 0: The PhyRdy signal is not changed. 1: The PhyRdy signal is changed. This bit is set to 1 when the value of the PhyRdy signal is changed from 1 to 0 or from 0 to 1.
[15:11]	RO	reserved	Reserved
[10]	WC	err_p	SATA protocol incompliance error status 0: All device behaviors comply with the SATA protocol. 1: Some device behaviors do not comply with the SATA protocol.
[9]	RO	reserved	Reserved
[8]	WC	err_t	Data integrity error status 0: No data integrity error is detected. 1: A data integrity error is detected.
[7:0]	RO	reserved	Reserved

SATA_PORT_SACT

SATA_PORT_SACT is an NCQ command identifier control register.

Offset Address	Register Name	Total Reset Value
0x034 + *n* x 0x80	SATA_PORT_SACT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	port_sact							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	port_sact	NCQ command identifier control Each bit of this register maps to a tag ID and an NCQ command in the memory. To be specific, bit[31:0] map to the commands of slot 31–0 and tag 31–0 respectively. The following describes the meaning of each bit by taking bit[3] as an example: 0: The slot 3 command is a non-NCQ command. 1: The slot 3 command is an NCQ command. Before setting SATA_PORT_SACT bit[3] to 1, the software must clear SATA_PORT_CI bit[3]. After the command data transfer, the device transmits an SDB FIS. Then, the controller clears SATA_PORT_SACT bit[3] based on the SActive in the FIS. The software can set SATA_PORT_SACT only when cmd_st is 1. When cmd_st is 0, all bits of SATA_PORT_SACT are cleared.

SATA_PORT_CI

SATA_PORT_CI is a command TX control register.

Offset Address	Register Name	Total Reset Value
0x38 + *n* x 0x80	SATA_PORT_CI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_ci																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	port_ci	Control for the commands to be transmitted Each bit of this register maps to a command in the memory. To be specific, bit[31:0] map to the commands of slot 31–0 respectively. The following describes the meaning of each bit by taking bit[3] as an example: 0: There is no slot 3 command to be transmitted and executed. 1: A slot 3 command is created in the memory. Then the controller can transmit this command. After running this command and receiving a corresponding FIS, the controller clears SATA_PORT_CI bit[3] and the BSY, DRQ, and ERR bits of SATA_PORT_TFD. The bits of SATA_PORT_CI can be set to 1 only when cmd_st is 1 and all bits of SATA_PORT_CI are cleared when cmd_st is 0.

SATA_PORT_SNTF

SATA_PORT_SNTF is an async notification event indicator register.

Offset Address	Register Name	Total Reset Value
0x3C + *n* x 0x80	SATA_PORT_SNTF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pxsntf_pmn															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	WC	pxsntf_pmn	Async notification event status If the controller receives an SDB FIS from the device on the PM port and the N bit of this FIS is 1, the controller sets the bit of this register corresponding to this port number to 1. The following describes the meaning of each bit by taking bit[3] as an example: 0: No async notification event occurs on the device whose PM port number is 3. 1: An async notification event occurs on the device whose PM port number is 3.

SATA_PORT_FBS

SATA_PORT_FBS is an FIS-based switching control register.

Offset Address	Register Name	Total Reset Value
0x40 + *n* x 0x80	SATA_PORT_FBS	0x0000_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												fbs_dwe				fbs_ado				fbs_dev				reserved					fbs_sde	fbs_dec	fbs_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RO	fbs_dwe	A fatal error occurs on the device corresponding to the current PM port. This field is configured by hardware and is valid only when PxFBS.SDE is 1.

[15:12]	RO	fbs_ado	Maximum number of external devices mounted over the PM during the current FIS-based switching. This field is configured by hardware. The number of PM domains corresponding to the created command should be less than the value when a command is created for optimal performance.
[11:8]	RW	fbs_dev	ID of the PM port to which the next command is transmitted. This field is configured by software. Software cannot transmit commands to multiple PM ports. Therefore, when a CI is created, commands cannot be transmitted to multiple PM ports. The same PM port must be used for a CI.
[7:3]	RO	reserved	Reserved
[2]	RO	fbs_sde	When this field is set to 1, a fatal error occurs, and hardware considers that software processes this error first. This field is cleared by setting PxCMD.ST to 0. When PxFBS.DEC is set to 1 or PxCMD.ST is set to 0, the fbs_sde bit needs to be cleared.
[1]	RW	fbs_dec	When software sets this bit to 1, the HBA needs to clear the error trigger conditions and clear the commands of the outstanding corresponding to the device including PxCI and PxSACT of the device. After hardware rectifies the error, the hardware must set this bit to 0. Writing 0 to this bit by using software has no effect. Software can set this bit to 1 only when PxFBS.EN and PxFBS.SDE are 1.
[0]	RW	fbs_en	When this bit is set to 1, a PM is connected, and the HBA needs to enable FIB-based switching to communicate with the PM. When this bit is cleared, FIS-based switching is unavailable. Software can modify this bit only when PxCMD.ST is 0.

SATA_PORT_FIFOTH

SATA_PORT_FIFOTH is an RX FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x044 + *n* x 0x80	SATA_PORT_FIFOTH	0x076D_9F24

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			mem_ctrl		reserved	dmac_rxfifo_th	rxfifo_th_sel / link_rxfifo_th
Reset	0 0 0 0	0 1 1 1	0 1 1 0	1 0 1 1	1 0 0 1	1 1 1 1	0 0 1 0	0 1 0 0

Bits	Access	Name	Description
[31:18]	RW	reserved	Reserved

[17:11]	RW	mem_ctrl	Timing parameter for controlling the memory [13:11]: EMAA in the corresponding memory [14]: EMSA in the corresponding memory [17:15]: EMAB in the corresponding memory
[10:9]	RO	reserved	Reserved
[9]	RW	hold_seagate_bug_en	The test shows that some Seagate hard disks do not comply with the protocol. To be specific, CONTp is transmitted after primitives are transmitted once. This bug can be avoided by setting this bit to 1.
[8:4]	RW	dmac_rxfifo_th	Flow control threshold of the DMAC RX FIFO. During data reception, if the data amount in the DMAC FIFO is above the threshold, the controller starts to control the data flow.
[3]	RW	rxfifo_th_sel	Flow control FIFO select 0: The flow control for the link RX FIFO is valid. 1: The flow control for the DMAC RX FIFO is valid.
[2:0]	RW	link_rxfifo_th	Flow control threshold of the link RX FIFO. During data reception, if the data amount in the DMAC FIFO is above the threshold, the controller starts to control the data flow.

SATA_PORT_PHYCTL1

SATA_PORT_PHYCTL1 is PHY control register 1.

Offset Address	Register Name	Total Reset Value
0x048 + *n* x 0x80	SATA_PORT_PHYCTL1	0x002E_5CB8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				px_tx_invert	px_nearafelb	px_bpr_reset	px_rx_eq					px_tx_amplitude_gen3				px_tx_amplitude_gen2				px_tx_amplitude_gen1								px_rx_invert			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	1	0	1	1	1	0	0	1	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27]	RW	px_tx_invert	Whether polarity reverse is allowed in the TX direction 0: no 1: yes
[26]	RW	px_nearafelb	Loopback mode for the BIST test
[25]	RW	px_bpr_reset	Reset in BIST mode

[24:22]	RW	px_rx_eq	Equalization setting in the RX direction
[21:15]	RW	px_tx_amplitude_gen3	Amplitude of the TX signal in Gen3 mode
[14:8]	RW	px_tx_amplitude_gen2	Amplitude of the TX signal in Gen2 mode
[7:1]	RW	px_tx_amplitude_gen1	Amplitude of the TX signal in Gen1 mode
[0]	RW	px_rx_invert	Whether polarity reverse is allowed in the RX direction 0: no 1: yes

SATA_PORT_PHYCTL2

SATA_PORT_PHYCTL2 is PHY control register 2.

Offset Address	Register Name	Total Reset Value
0x04C + *n* x 0x80	SATA_PORT_PHYCTL2	0x0002_0555

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													px_reset	px_tx_preemph_gen3						px_tx_preemph_gen2				px_tx_preemph_gen1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	px_reset	Lane reset signal of the SerDes, async reset, active high
[17:12]	RW	px_tx_preemph_gen3	TX preemphasis control in Gen3 mode
[11:6]	RW	px_tx_preemph_gen2	TX preemphasis control in Gen2 mode
[5:0]	RW	px_tx_preemph_gen1	TX preemphasis control in Gen1 mode

SATA_PORT_HBA

SATA_PORT_HBA is an HBA test status register.

Offset Address	Register Name	Total Reset Value
0x050 + *n* x 0x80	SATA_PORT_HBA	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				p_curr_st				reserved				ndr_curr_st				cfis_curr_st				reserved	pio_curr_st			reserved	pm_curr_st			err_curr_st			
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RO	p_curr_st	Current status of the HBA_PINIT_STATE state machine
[23:21]	RO	reserved	Reserved
[20:16]	RO	ndr_curr_st	Current status of the HBA_NDR_STATE state machine
[15:12]	RO	cfis_curr_st	Current status of the HBA_CFIS_STATE state machine
[11]	RO	reserved	Reserved
[10:8]	RO	pio_curr_st	Current status of the HBA_PIO_STATE state machine
[7]	RO	reserved	Reserved
[6:4]	RO	pm_curr_st	Current status of the HBA_PM_STATE state machine
[3:0]	RO	err_curr_st	Current status of the HBA_ERR_STATE state machine

SATA_PORT_LINK

SATA_PORT_LINK is a link test status register.

Offset Address	Register Name	Total Reset Value
0x054 + *n* x 0x80	SATA_PORT_LINK	0x0020_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				link_curr_st				reserved	link_df_fifo_full	link_df_fifo_empty		link_df_fifo_count				reserved	link_rx_fifo_full	link_rx_fifo_empty		link_rx_fifo_count				reserved	link_tx_fifo_full	link_tx_fifo_empty		link_tx_fifo_count			
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved

[28:24]	RO	link_curr_st	Current status of the LINK_CTL_STATE state machine
[23]	RO	reserved	Reserved
[22]	RO	link_df_fifo_full	Full flag of the link frequency difference FIFO 0: not full 1: full
[21]	RO	link_df_fifo_empty	Empty flag of the link frequency difference FIFO 0: not empty 1: empty
[20:16]	RO	link_df_fifo_count	Data amount in the link frequency difference FIFO
[15]	RO	reserved	Reserved
[14]	RO	link_rx_fifo_full	Full flag of the link RX FIFO 0: not full 1: full
[13]	RO	link_rx_fifo_empty	Empty flag of the link RX FIFO 0: not empty 1: empty
[12:8]	RO	link_rx_fifo_count	Data amount in the link RX FIFO
[7]	RO	reserved	Reserved
[6]	RO	link_tx_fifo_full	Full flag of the link TX FIFO 0: not full 1: full
[5]	RO	link_tx_fifo_empty	Empty flag of the link TX FIFO 0: not empty 1: empty
[4:0]	RO	link_tx_fifo_count	Data amount in the link TX FIFO

SATA_PORT_DMA1

SATA_PORT_DMA1 is DMAC test status register 1.

Offset Address	Register Name	Total Reset Value
0x058 + *n* x 0x80	SATA_PORT_DMA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				txdmac_cur_state				txdmac_prd_i	tx_entry_dbc_cnt																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RO	txdmac_cur_state	Current status of the SATA_TX_DMAC state machine
[23]	RO	txdmac_prd_i	I bit in the entry of the PRD linked list of SATA_TX_DAMC
[22:0]	RO	tx_entry_dbc_cnt	Down counter in SATA_TX_DMAC. It indicates the number of data bytes in the current entry.

SATA_PORT_DMA2

SATA_PORT_DMA2 is DMAC test status register 2.

Offset Address	Register Name	Total Reset Value
0x05C + *n* x 0x80	SATA_PORT_DMA2	0x0020_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_data_fis_cnt																tx_cmdh_prdtl							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:8]	RO	tx_data_fis_cnt	Down counter in SATA_TX_DMAC. It indicates the number of data FIS bytes during the operation of PIO, legacy DMA, or first party DMA. For the PIO operation, the initial value is equal to the value of transcount in the PIO setup FIS; for the legacy DMA or first party DMA operation, the initial value is 0x2000 (2048 DWORD).
[7:0]	RO	tx_cmdh_prdtl	Down counter in SATA_TX_DMAC. The parameter in the command header indicates the number of entries in the PRDT.

SATA_PORT_DMA3

SATA_PORT_DMA3 is DMAC test status register 3.

Offset Address	Register Name	Total Reset Value
0x060 + *n* x 0x80	SATA_PORT_DMA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_fpdma_tran_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	tx_fpdma_tran_cnt	Down counter in SATA_TX_DMAC. It indicates the number of data FIS bytes during the first party DMA operation.

SATA_PORT_DMA4

SATA_PORT_DMA4 is DMAC test status register 4.

Offset Address	Register Name	Total Reset Value
0x064 + *n* x 0x80	SATA_PORT_DMA4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rxdmac_cur_state				rxdmac_prd_i	rx_entry_dbc_cnt																						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RO	rxdmac_cur_state	Current status of the SATA_RX_DMAC state machine
[23]	RO	rxdmac_prd_i	I bit in the entry of the PRD linked list of SATA_RX_DAMC
[22:0]	RO	rx_entry_dbc_cnt	Down counter in SATA_RX_DMAC. It indicates the number of data bytes in the current entry.

SATA_PORT_DMA5

SATA_PORT_DMA5 is DMAC test status register 5.

Offset Address	Register Name	Total Reset Value
0x068 + *n* x 0x80	SATA_PORT_DMA5	0x0020_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_data_fis_cnt																rx_cmdh_prdtl							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:8]	RO	rx_data_fis_cnt	Down counter in SATA_RX_DMAC. It indicates the number of data FIS bytes during the operation of PIO, legacy DMA, or first party DMA. For the PIO operation, the initial value is equal to the value of transcount in the PIO setup FIS; for the legacy DMA or first party DMA operation, the initial value is 0x2000 (2048 DWORD).
[7:0]	RO	rx_cmdh_prdtl	Down counter in SATA_RX_DMAC. The parameter in the command header indicates the number of entries in the PRDT.

SATA_PORT_DMA6

SATA_PORT_DMA6 is DMAC test status register 6.

Offset Address	Register Name	Total Reset Value
0x6C + *n* x 0x80	SATA_PORT_DMA6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_fpdma_tran_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rx_fpdma_tran_cnt	Down counter in SATA_RX_DMAC. It indicates the number of data FIS bytes during the first party DMA operation. The initial value is equal to the value of transcount in the DMA setup FIS.

SATA_PORT_DMA7

SATA_PORT_DMA7 is DMAC test status register 7.

Offset Address	Register Name	Total Reset Value
0x070 + *n* x 0x80	SATA_PORT_DMA7	0x0005_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										pio_op	fpdma_op	dmac_rx_fifo_full	dmac_rx_fifo_empty	dmac_tx_fifo_full	dmac_tx_fifo_empty	dmac_rx_fifo_cnt								dmac_tx_fifo_cnt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RO	pio_op	PIO operation indicator 0: The current command is not used for the PIO operation. 1: The current command is used for the PIO operation.
[20]	RO	fpdma_op	First party DMA operation indicator 0: The current command is not used for the first party DMA operation. 1: The current command is used for the first party DMA operation.
[19]	RO	dmac_rx_fifo_full	Full status of SATA_DMAC_RX_FIFO 0: not full 1: full
[18]	RO	dmac_rx_fifo_empty	Empty status of SATA_DMAC_RX_FIFO 0: not empty 1: empty
[17]	RO	dmac_tx_fifo_full	Full status of SATA_DMAC_TX_FIFO 0: not full 1: full
[16]	RO	dmac_tx_fifo_empty	Empty status of SATA_DMAC_TX_FIFO 0: not empty 1: empty
[15:8]	RO	dmac_rx_fifo_cnt	Number of data segments in SATA_DMAC_RX_FIFO (in DWORD)
[7:0]	RO	dmac_tx_fifo_cnt	Number of data segments in SATA_DMAC_TX_FIFO (in DWORD)

SATA_PORT_PHYCTL

SATA_PORT_PHYCTL is a PHY control register.

Offset Address	Register Name	Total Reset Value
0x074 + *n* x 0x80	SATA_PORT_PHYCTL	0x0E24_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	test_seq_sel			phy_disable	phy_calibrated	spd_change_ack	dp_rdy	bist_tx_fspd	neg_mode_b	gen2_en	reserved																				port_phy_ctrl_1	port_phy_ctrl_0
Reset	0	0	0	0	1	1	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	test_seq_sel	Test mode. Parameters are set to transmit various test sequences to test eye patterns. 001: The HFTP sequence is transmitted. 010: The MFTP sequence is transmitted. 100: The LFTP sequence is transmitted. 011: The LBP sequence is transmitted.
[28]	RW	phy_disable	PHY enable 0: enabled 1: disabled
[27]	RW	phy_calibrated	Whether to calibrate the PHY 0: not calibrated 1: calibrated
[26]	RW	spd_change_ack	Whether the rate can be switched 0: no 1: yes
[25]	RW	dp_rdy	Whether the PHY is ready to transmit data 0: no 1: yes
[24]	RW	bist_tx_fspd	Whether the clock frequency is forcibly transmitted in BIST mode 0: no 1: yes
[23]	RW	neg_mode_b	Negotiation mode B select 0: not supported 1: supported

[22:21]	RW	gen2_en	Maximum interface rate control signal 00: 1.5 Gbit/s mode 01: 3 Gbit/s mode 10: 6 Gbit/s mode 11: reserved
[20:2]	RO	reserved	Reserved
[1]	RW	port_phy_ctrl_1	Rate mode select. This bit is valid only when the rate mode is controlled by software (port_phy_ctrl_0 is 1). 1: 1.5 Gbit/s mode 0: 3 Gbit/s mode
[0]	RW	port_phy_ctrl_0	Rate control mode 0: hardware automatic negotiation 1: software control

SATA_PORT_PHYSTS

SATA_PORT_PHYSTS is a PHY test status register.

Offset Address	Register Name	Total Reset Value
0x078 + *n* x 0x80	SATA_PORT_PHYSTS	0x0000_1883

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												current_state				spd_change	link_rdy	init_compl	pwr_state	rx_pll_pwron	rx_en	tx_en		mpll_pwron	phy_comwake	phy_cominit	half_rate		phyrdy	los	op_done
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:17]	RO	current_state	Current status of the state machine at the PHY layer
[16]	RO	spd_change	Rate change request
[15]	RO	link_rdy	Sufficient D10.2 is transmitted when this bit is 1.
[14]	RO	init_compl	Non-align primitive is received and initialization is complete when this bit is 1.

[13]	RO	pwr_state	Whether the controller is in low-power (slumber or partial) status 1: yes 0: no
[12]	RO	rx_pll_pwron	PHY RX PLL power-on indicator
[11]	RO	rx_en	RX enable indicator 0x0: disabled 0x1: enabled
[10:8]	RO	tx_en	Required status of the PHY TX 000: idle status 001: low-power slumber status 010: low-power partial status 011: normal working status
[7]	RO	mpll_pwron	MPLL power-on indicator
[6]	RO	phy_comwake	The PHY detects COMWAKE when this bit is 1.
[5]	RO	phy_cominit	The PHY detects COMINIT when this bit is 1.
[4:3]	RO	half_rate	Rate mode of the PHY 0: full-speed mode 1: half-speed mode
[2]	RO	phyrdy	The OOB phase and rate negotiation are complete at the link layer when this bit 1, and data can be normally transmitted currently.
[1]	RO	los	Status of the RX differential line 0: Data is received on the RX differential line that is in normal operating status. 1: The RX differential line is in static idle status.
[0]	RO	op_done	The PHY PLL is powered on when this bit is 1.

SATA_PORT_OUTSTANDING

SATA_PORT_OUTSTANDING is an AXI outstanding control register.

Offset Address	Register Name	Total Reset Value
0x07C + *n* x 0x80	SATA_PORT_OUTSTANDING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						px_wr_otd_ctrl				px_rd_otd_ctrl						px_wr_otd_en	px_rd_otd_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:6]	RW	px_wr_otd_ctrl	Maximum outstanding capability during the write operation performed by the AXI master of each port 1111: outstanding of 16 0111: outstanding of 8 0011: outstanding of 4 0001: outstanding of 2 0000: outstanding of 1 Other values: reserved
[5:2]	RW	px_rd_otd_ctrl	Maximum outstanding capability during the read operation performed by the AXI master of each port 1111: outstanding of 16 0111: outstanding of 8 0011: outstanding of 4 0001: outstanding of 2 0000: outstanding of 1 Other values: reserved
[1]	RW	px_wr_otd_en	Whether to control the maximum outstanding capability during the write operation performed by the AXI master of each port 0: no 1: yes
[0]	RW	px_rd_otd_en	Whether to control the maximum outstanding capability during the read operation performed by the AXI master of each port 0: no 1: yes

13.6.8 Appendix A Format of the SATA Command Linked List

Figure 13-40 shows the structure of the FIS linked list. The linked list refers to spaces that are created in the system memory by software. The base address for the linked list is stored in the PxFB and PxFBU registers in the AHCI register group. The DMAC uses this base address as its destination address and transfers the received frames to different memory spaces.

Figure 13-40 Structure of the linked list

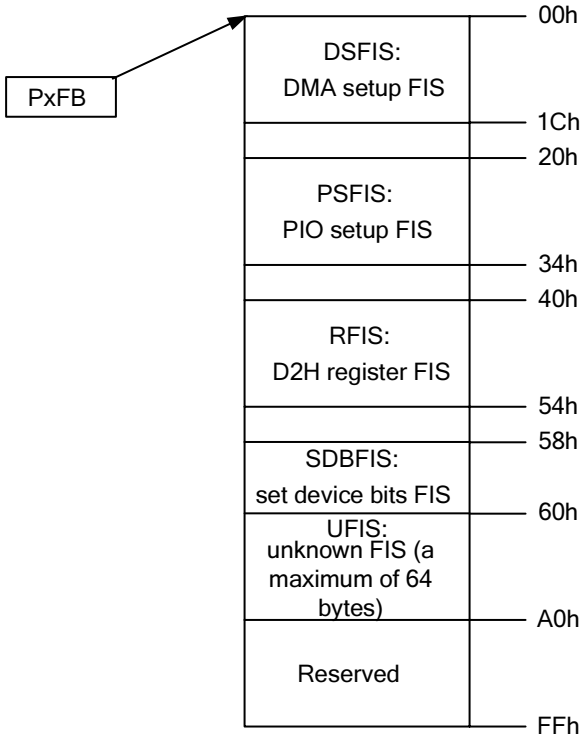
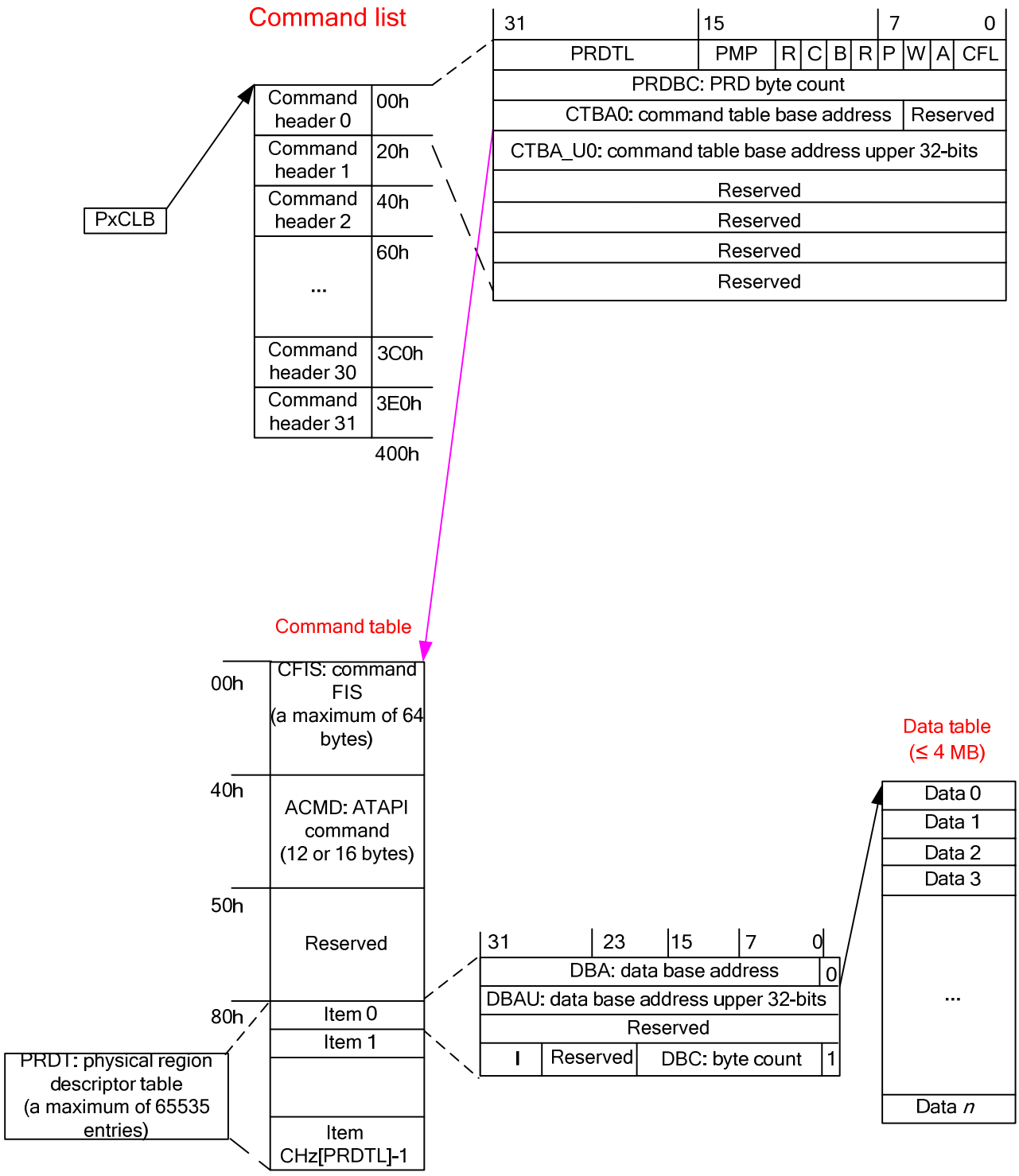


Figure 13-41 shows the structures of a command list and a data list. Such lists refer to the areas that are created in the system memory by software. A command list contains a maximum of 32 commands, and its base address is specified by the PxCLB and PxCLBU registers in the AHCI register group. Each command has a command header in which the CTBA0 part specifies the base address for the command table. The command table contains the commands to be read and the data space linked list to be read and written.

Figure 13-41 Structures of the command list and data list



Each time before a command is executed, the preceding two lists must be created in the memory. For details about the meaning of the lists, see the AHCI1.2 protocol. The CFIS area is used to store the H2D register FISs. For details, see the SATA2.5 protocol. The ACMD area is used to store the commands related to the ATAPI operation. For details, see the protocols about the DVD devices and CD-ROMs provided by the Small Form Factor (SSF) Committee.

13.7 USB 2.0 Host

13.7.1 Overview

The USB 2.0 host controller supports the high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) data transfer modes. It complies with the USB 2.0, open host controller interface (OHCI) V1.0a, and enhanced host controller interface (EHCI) V1.0 protocols. The USB 2.0 host controller has a root hub. As a part of the USB system, the root hub is used to extend the USB port. By using in the controller, the following functions are achieved:

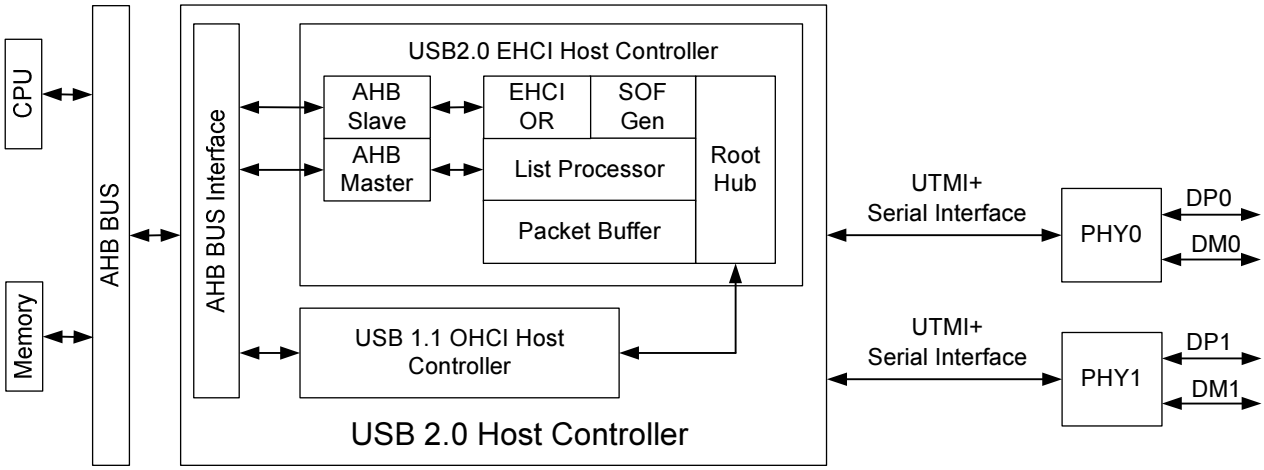
- Controls and processes data transfer.
- Parses data packets and packages data.
- Encodes and decodes the signals transmitted through the USB port.
- Provide interfaces (such as the interrupt vector interface) for the driver.

13.7.2 Function Description

Logic Block Diagram

Figure 13-42 shows the logic block diagram of the USB 2.0 host controller.

Figure 13-42 Logic block diagram of the USB 2.0 host controller



NOTE

- UTMI: USB2.0 transceiver macrocell interface
- EHCI: enhanced host controller interface
- OHCI: open host controller interface

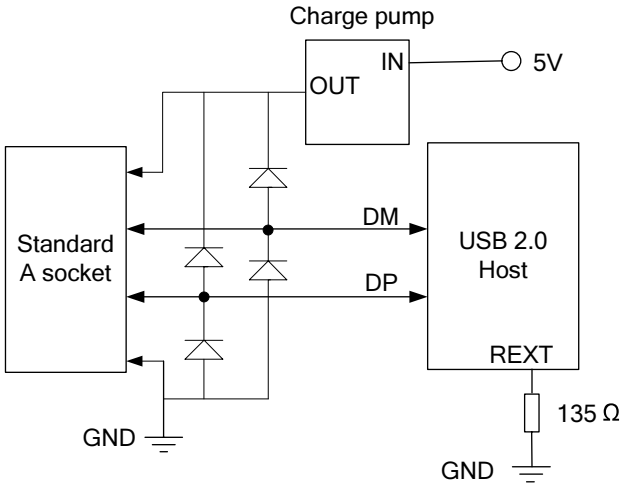
Typical Application

Figure 13-43 shows the reference design of the USB 2.0 host controller.

CAUTION

- The impedance of DP or DM is 45 Ω ±1% and no extra matched resistors are required.
- The REXT resistor is a ±1% resistor.
- If high-speed electro static discharge (ESD) components are used, 1 pF capacitors are recommended.

Figure 13-43 Reference design of the USB 2.0 host controller



Functions

The USB 2.0 host controller has the following features:

- Fully compatible with USB 2.0.
- Complies with OHCI V1.0a and EHCI V1.0 protocols.
- Supports high-speed, full-speed, and low-speed devices.
- Supports low-power solutions.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.
- Supports a maximum of 127 devices by using USB hubs

Working Principle

The USB 2.0 host controller supports the following four standard transfer modes:

- Control transfer

  This mode applies to the data transfer between endpoints 0 of USB host and the USB device. For the USB devices of specific models, other endpoints may be used. The control transfer is bidirectional and the transferred data amount is small. Depending on the device and transfer speed, 8-byte data, 16-byte data, 32-byte data, or 64-byte data can be transferred.

- Bulk transfer

  This mode applies to the data transfer in bulk when there is no limit on the bandwidth and time interval. This mode is the best choice when the transfer speed is very low and many data transfers are delayed. Bulk transfer can be performed after all other types of data transfers are complete. In bulk transfer mode, data is transferred between the USB Host and USB Device without errors by using an error detection and retransmission mechanism.

- Isochronous transfer

  This mode applies to the stream data transfer with strict time requirements and strong error tolerance or the instant data transfer at a constant transfer rate. This mode provides a fixed bandwidth and time interval.

- Interrupt transfer

  This mode applies to the data transfer when the data is scattered, unpredictable, and is of small volume. In this mode, the device is checked whether there is interrupt data to be sent at a fixed interval. The query frequency ranges from 1 ms to 255 ms and it depends on the device endpoint mode. The typical interrupt transfer mode is unidirectional and only input is available for the USB host.

13.7.3 Operating Mode

NOTE

For details about clock and reset registers, see section 3.2.7 "Register Description" in chapter 3 "System."

Pin Polarity Control

The valid polarity of the USB power supply can be specified by configuring the system control register MISC_CTRL20[usb2_host_pwren_pol]. The valid polarity of USB overcurrent protection can be specified by configuring the system control register MISC_CTRL20[usb2_host_ovrcur_pol].

Clock Gating

If the USB 2.0 host controller is not used, its clock can be disabled to reduce power consumption.

To disable the clock, perform the following steps:

Step 1 Write 1 to PERI_CRG28[usb2phy_port1_treq], PERI_CRG28[usb2phy_port0_treq], PERI_CRG28[usb2_ctrl_utmi1_req], PERI_CRG28[usb2_ahb_srst_req] and PERI_CRG28[usb2_ctrl_utmi0_req] respectively to reset the USB controller and PHY.

Step 2 Set PERI_CRG28[usb2_cken] to 0 to disable the clocks of the USB 2.0 PHY and controller.

----End

To enable the clock, perform the following steps:

Step 1 Set PERI_CRG28[usb2_cken] to 1 to enable the clocks of the USB 2.0 host controller.

Step 2 Deassert the reset on the USB controller and PHY. For details, see "Reset Deassert"

----End

Reset Deassert

By default, the USB controller and PHY are reset after power-on. To deassert reset, perform the following steps:

Step 1 Delay at least 10 μs.

Step 2 Write 0 to PERI_CRG28[usb2phy_port1_treq] and PERI_CRG28[usb2phy_port0_treq] to deassert the soft reset on USB PHY port 1 and port 0 respectively.

Step 3 Write 0 to PERI_CRG28[usb2phy_req] to deassert the global reset on the USB PHY.

Step 4 After a delay of 250 μs, write 0 to PERI_CRG28[usb2_ctrl_utmi1_req] and PERI_CRG28[usb2_ctrl_utmi1_req] to deassert the soft reset on port 1 and port 0 of the USB controller respectively, and write 0 to PERI_CRG28[usb2_ctrl_hub_req] to deassert the soft reset on the USB controller.

Step 5 Write 0 to PERI_CRG28[usb2_ahb_srst_req] to deassert the soft reset on the USB bus.

----End

Separately Resetting Ports During the Working Process

To reset port0 separately during the working process, perform the following steps:

Step 1 Write 1 to PERI_CRG28[usb2_ctrl_utmi0_req] to soft-reset port0 of the USB controller.

Step 2 Write 1 to PERI_CRG28[usb2phy_port0_treq] to soft-reset port0 of the USB PHY.

Step 3 After 200 μs delay, write 0 to PERI_CRG28[usb2phy_port0_treq] to deassert the reset on port0 of the USB PHY.

Step 4 Write 0 to PERI_CRG28[usb2_ctrl_utmi0_req] to deassert the reset on port0 of the USB controller.

---End

To reset port1 separately during the working process, perform the following steps:

Step 5 Write 1 to PERI_CRG28[usb2_ctrl_utmi1_req] to soft-reset port0 of the USB controller.

Step 6 Write 1 to PERI_CRG28[usb2phy_port1_treq] to soft-reset port0 of the USB PHY.

Step 7 After 200 μs delay, write 0 to PERI_CRG28[usb2_ctrl_utmi1_req] to deassert the reset on port0 of the USB PHY.

Step 8 Write 0 to PERI_CRG28[usb2phy_port1_treq] to deassert the reset on port0 of the USB controller.

----End

Variables in the Offset Addresses for USB 2.0 Registers

Table 13-14 describes the value ranges and meanings of the variables in the offset addresses of registers.

Table 13-14 Variables in the offset addresses for USB 2.0 registers

Variable	Value Range	Description
FIFO_num	0–14	Number of FIFOs
n	0–15	Endpoint *n*

13.7.4 Register Summary

Table 13-15 describes USB 2.0 registers.

Table 13-15 Summary of USB 2.0 registers (base address: 0x1004_0000)

Offset Address	Register	Description	Page
0x90	INTNREG00	Micro-frame length configuration register	13-158
0x94	INSNREG01	PBUF OUT/IN register	13-159
0x98	INSNREG02	PBUF depth register	13-159
0x9C	INSNREG03	Interrupt memory transfer enable register	13-160
0xA0	INTNREG04	Debug register	13-160
0xA4	INTNREG05	Control and status register	13-161
0xA8	INTNREG06	AHB error status register	13-162
0xAC	INTNREG07	AHB error address register	13-162

NOTE

The base address of the EHCI register is 0x1004_0000 and the base address of the OHCI register is 0x1003_0000. The base address of Table 13-15 is that of the EHCI register.

13.7.5 Register Description

INTNREG00

INTNREG00 is a micro-frame length configuration register.

Offset Address	Register Name	Total Reset Value
0x90	INTNREG00	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved					val			en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved

[13:1]	RW	val	Value of the micro-frame counter. This register is used only for emulation. In normal mode, the micro-frame length is 125 μs defined by the protocol. During emulation, you can change the micro-frame length by configuring this register as required to reduce the emulation time.
[0]	RW	en	Register enable 0: disabled 1: enabled

INSNREG01

INTNREG01 is a PBUF out/in configuration register.

Offset Address	Register Name	Total Reset Value
0x94	INSNREG01	0x0020_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	out_threshold																in_threshold															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	out_threshold	TX threshold. If the data amount in the PBUF is above the TX threshold, data starts to be transmitted. The depth is measured by 32 bits.
[15:0]	RW	in_threshold	RX threshold. If the data amount in the PBUF is above the RX threshold, data is read from the PBUF. The depth is measured by 32 bits.

INSNREG02

INSNREG02 is a PBUF depth configuration register.

Offset Address	Register Name	Total Reset Value
0x98	INSNREG02	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pbuf_depth											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	pbuf_depth	PBUF depth. The depth is measured by 32 bits.

INSNREG03

INSNREG03 is an interrupt memory transfer enable register.

Offset Address	Register Name	Total Reset Value
0x9C	INSNREG03	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	dis	ctrl	val			fetch	offset								brk_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	dis	256 MHz clock check enable 0: disabled 1: enabled
[13]	RW	ctrl	Line state ignore during TESTSE0 NAK
[12:10]	RW	val	tx-tx turnaround delay addition
[9]	RW	fetch	Periodic frame list RX
[8:1]	RW	offset	Available time offset
[0]	RO	brk_en	Interrupt memory transfer enable 0: disabled 1: enabled

INTNREG04

INTNREG04 is a debug register.

Offset Address	Register Name	Total Reset Value
0xA0	INTNREG04	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										auto_en	nak_reldfix_en	reserved	scaledwn_enum_time		hccparam_en	hcsparam_en

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	auto_en	Automatic feature enable 0: enabled. The suspend signal is valid when the run/stop bit is reset by software, but the hchalted bit is not set. 1: disabled. The port is not suspended when software clears the run/stop bit. The default value is 0.
[4]	RW	nak_reldfix_en	NAK reload enable 0: enabled 1: disabled
[3]	RO	reserved	Reserved
[2]	RW	scaledwn_enum_time	Port enumeration time scale down enable 0: disabled 1: enabled
[1]	RW	hccparam_en	HCCPARAMS register write enable 0: disabled 1: enabled
[0]	RW	hcsparam_en	HCSPARAMS register write enable 0: disabled 1: enabled

INTNREG05

INTNREG05 is a control and status register. It is used to read or write to the PHY.

Offset Address	Register Name	Total Reset Value
0xA4	INTNREG05	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														vbusy		vport			vcontrol_loadm	vcontrol				vstatus							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved

[17]	RO	vbusy	The value 1 indicates that the hardware is writing data. This bit is cleared only when the process ends.
[16:13]	RW	vport	Port ID. It cannot exceed the supported number of ports.
[12]	RW	vcontrol_loadm	Load enable 0: enabled 1: disabled
[11:8]	RW	vcontrol	Port control signal
[7:0]	RO	vstatus	Port status signal

INTNREG06

INTNREG06 is an AHB error status register.

Offset Address	Register Name	Total Reset Value
0xA8	INTNREG06	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_capture	reserved																			hbusrt_err				num_beat_err				num_beat_ok			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	err_capture	AHB error
[30:12]	RO	reserved	Reserved
[11:9]	RO	hbusrt_err	hbrust value during a control transfer when an AHB error occurs
[8:4]	RO	num_beat_err	Number of beats during a burst transfer when an AHB error occurs. The maximum number of beats is 16. 0x00–0x10: valid 0x11–0x1F: reserved
[3:0]	RO	num_beat_ok	Number of completed beats during a burst transfer when an AHB error occurs

INTNREG07

INTNREG07 is an AHB error address register.

Offset Address	Register Name	Total Reset Value
0xAC	INTNREG07	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_addr	Address during a control transfer when an AHB error occurs

Contents

A Ordering Information

Figure A-1 shows the Hi3521A mark.

Figure A-1 Hi3521A mark

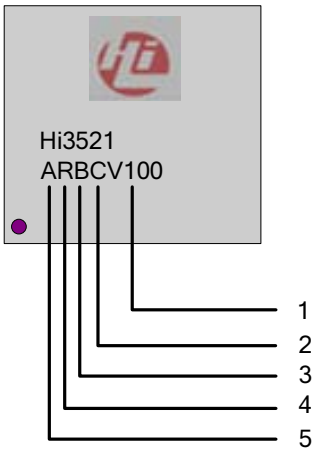


Figure A-2 shows the Hi3520D V300 mark.

Figure A-2 Hi3520D V300 mark

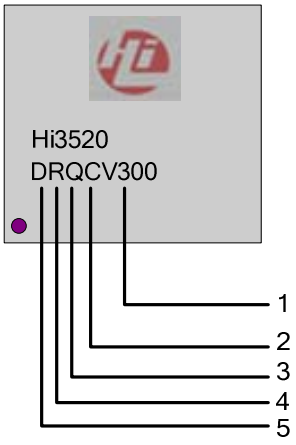


Table A-1 describes the Hi3521A and Hi3520D V300 marks.

Table A-1 Meaning of Hi3521A and Hi3520D V300 marks

No.	Item	Description
1	Version number	It indicates the chip version number.
2	Temperature flag	The letter C stands for commercial. It indicates that the chip is for commercial use.
3	Package flag	The letter B indicates the ball grid array (BGA) package. The letter Q stands for quad flat package (QFP)
4	Environmental protection flag	The letter R stands for restriction of the use of certain hazardous substances (RoHS).
5	Product differentiation flag	It is the last character of a chip name for differentiating one chip from another one.